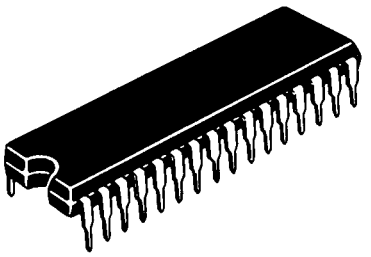
AKM628128 Series

131072-Word × 8-Bit High Speed CMOS Static RAM

The AKM628128 is a CMOS static RAM organized 128-kword × 8-bit. It realizes higher density, higher performance and low power consumption by employing 0.8 μm Hi-CMOS process technology.

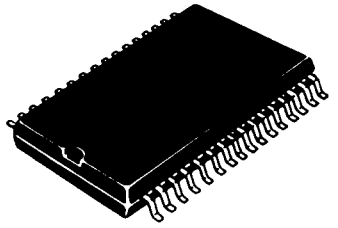
It offers low power standby power dissipation; therefore, it is suitable for battery back-up systems. The device, packaged in a 525 mil SOP (460-mil body SOP) or a 600-mil plastic DIP, or a 8 × 20mm TSOP with thickness of 1.2 mm is available for high density mounting. TSOP package is suitable for cards, and reverse type TSOP is also provided.

AKM628128P Series



(DP-32)

AKM628128FP Series



(FP-32D)

Features

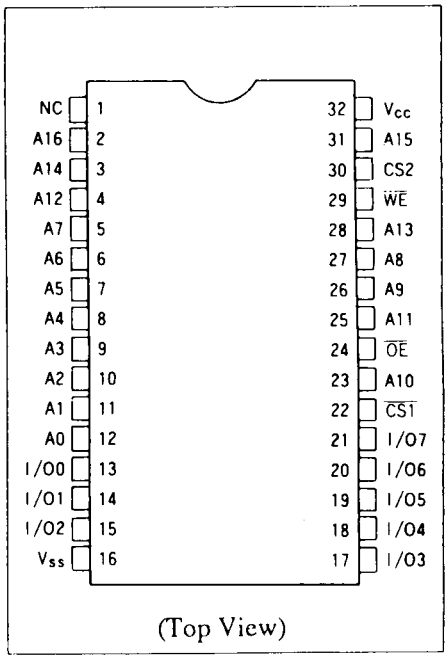
- High speed: Fast access time 70/85/100/120 ns (max.)
- Low power
  - Standby: 10 μW (typ) (L-version)
  - Operation: 75 mW (typ)
- Single 5 V supply
- Completely static memory
  - No clock or timing strobe required
- Equal access and cycle times
- Common data input and output: Three state output
- Directly TTL compatible: All inputs and outputs
- Capability of battery back up operation (L-version)
  - 2 chip selection for battery back up

■ ORDERING INFORMATION

Type No.	Access Time	Package
AKM628128P-7 AKM628128P-8 AKM628128P-10 AKM628128P-12	70ns 85ns 100ns 120ns	600-mil 32-pin plastic DIP (DP-32)
AKM628128LP-7 AKM628128LP-8 AKM628128LP-10 AKM628128LP-12	70ns 85ns 100ns 120ns	
AKM628128LP-7SL AKM628128LP-8SL AKM628128LP-10SL AKM628128LP-12SL	70ns 85ns 100ns 120ns	
AKM628128FP-7 AKM628128FP-8 AKM628128FP-10 AKM628128FP-12	70ns 85ns 100ns 120ns	525-mil 32-pin plastic SOP (FP-32D)
AKM628128LFP-7 AKM628128LFP-8 AKM628128LFP-10 AKM628128LFP-12	70ns 85ns 100ns 120ns	
AKM628128LFP-7SL AKM628128LFP-8SL AKM628128LFP-10SL AKM628128LFP-12SL	70ns 85ns 100ns 120ns	

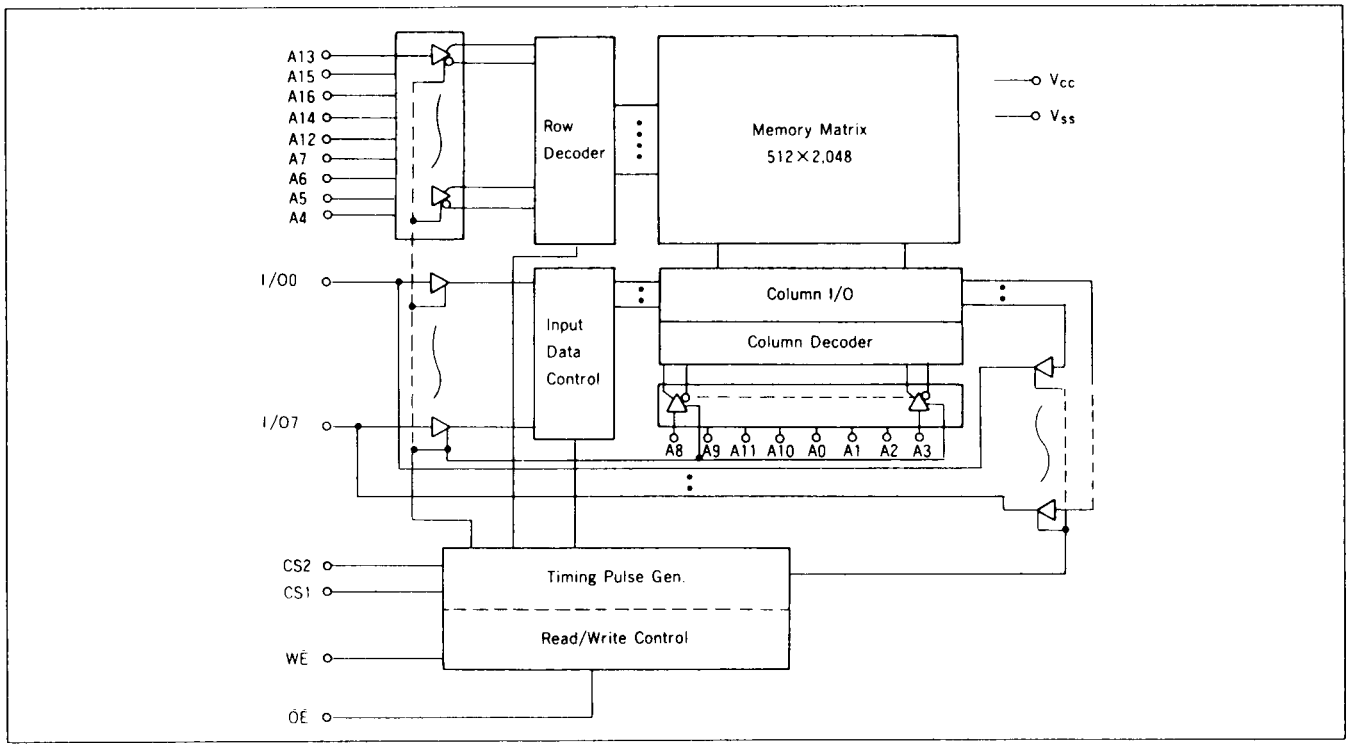
Type No.	Access Time	Package
AKM628128T-7 AKM628128T-8 AKM628128T-10 AKM628128T-12	70ns 85ns 100ns 120ns	8mm × 20mm 32-pin TSOP (normal type) (TFP-32D)
AKM628128LT-7 AKM628128LT-8 AKM628128LT-10 AKM628128LT-12	70ns 85ns 100ns 120ns	
AKM628128LT-7L AKM628128LT-8L AKM628128LT-10L AKM628128LT-12L	70ns 85ns 100ns 120ns	
AKM628128R-7 AKM628128R-8 AKM628128R-10 AKM628128R-12	70ns 85ns 100ns 120ns	8mm × 20mm 32-pin TSOP (reverse type) (TFP-32DR)
AKM628128LR-7 AKM628128LR-8 AKM628128LR-10 AKM628128LR-12	70ns 85ns 100ns 120ns	
AKM628128LR-7L AKM628128LR-8L AKM628128LR-10L AKM628128LR-12L	70ns 85ns 100ns 120ns	

■ PIN CONFIGURATION



(Top View)

Block Diagram



Function Table

$\overline{WE}$	$\overline{CS1}$	CS2	$\overline{OE}$	Mode	Vcc Current	Dout Pin	Ref. Cycle
×	H	×	×	Not selected	I_{SB}, I_{SB1}	High-Z	
×	×	L	×		I_{SB}, I_{SB1}	High-Z	
H	L	H	H	Output disable	Icc	High-Z	
H	L	H	L	Read	Icc	Dout	Read cycle
L	L	H	H	Write	Icc	Din	Write cycle (1)
L	L	H	L		Icc	Din	Write cycle (2)

Note: × : H or L

Absolute Maximum Ratings

Item	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_T	−0.5*1 to +7.0	V
Power dissipation	P_T	1.0	W
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	−55 to +125	°C
Storage temperature under bias	Tbias	−10 to +85	°C

Note: *1. −3.0 V for pulse half-width ≤ 30 ns

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Item	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{CC}	4.5	5.0	5.5	V	
	V_{SS}	0	0	0	V	
Input high (logic 1) voltage	V_{IH}	2.2	—	6.0	V	
Input low (logic 0) voltage	V_{IL}	−0.3*1	—	0.8	V	

Note: *1. −3.0 V for pulse half-width ≤ 30 ns

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V)

Item	Symbol	Min	Typ*1	Max	Unit	Test Conditions
Input leakage current	$\|I_{LI}\|$	—	—	2	µA	Vin = Vss to Vcc
Output leakage current	$\|I_{LO}\|$	—	—	2	µA	$\overline{CS1}$ = V_{IH} or CS2 = V_{IL} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL}, $V_{I/O}$= Vss to Vcc
Operating power supply current: DC	I_{CC}	—	15	35	mA	$\overline{CS1}$= V_{IL}, CS2 = V_{IH}, others = V_{IH}/V_{IL} $I_{I/O}$= 0 mA
Operating power supply current	I_{CC1}	—	45	70	mA	Min cycle, duty = 100%, $\overline{CS1}$ = V_{IL}, CS2 = V_{IH}, others = V_{IH}/V_{IL} $I_{I/O}$ = 0 mA
	I_{CC2}	—	15	30	mA	Cycle time = 1 µs, duty = 100%, $I_{I/O}$ = 0 mA $\overline{CS1}$ ≤ 0.2 V, CS2 ≥Vcc − 0.2 V V_{IH} ≥ Vcc − 0.2V, V_{IL} ≤ 0.2V
Standby power supply current: DC	I_{SB}	—	1	3	mA	$\overline{CS1}$ = V_{IH}, CS2 = V_{IH} or CS2 = V_{IL}
Standby power supply current (1): DC	I_{SB1}	—	0.02	2	mA	Vin ≥ 0 V $\overline{CS1}$ ≥ Vcc − 0.2 V, CS2 ≥ Vcc − 0.2 V or 0 V ≤ CS2 ≤ 0.2 V
		—	2*2	100*2	µA	
			2*3	50*3	µA	
Output low voltage	V_{OL}	—	—	0.4	V	I_{OL} = 2.1 mA
Output high voltage	V_{OH}	2.4	—	—	V	I_{OH} = −1.0 mA

Notes: *1. Typical values are at V_{CC} = 5.0 V, Ta = +25°C and specified loading.
*2. This characteristics is guaranteed only for L-version.
*3. This characteristics is guaranteed only for L-L/L-SL version.

Capacitance (Ta = 25°C, f = 1.0 MHz)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Input capacitance	Cin	—	—	8	pF	Vin = 0 V
Input/output capacitance	$C_{I/O}$	—	—	10	pF	$V_{I/O}$ = 0 V

Note: This parameter is sampled and not 100% tested.

AC Characteristics (Ta = 0 to +70°C, Vcc = 5 V ± 10%, unless otherwise noted)

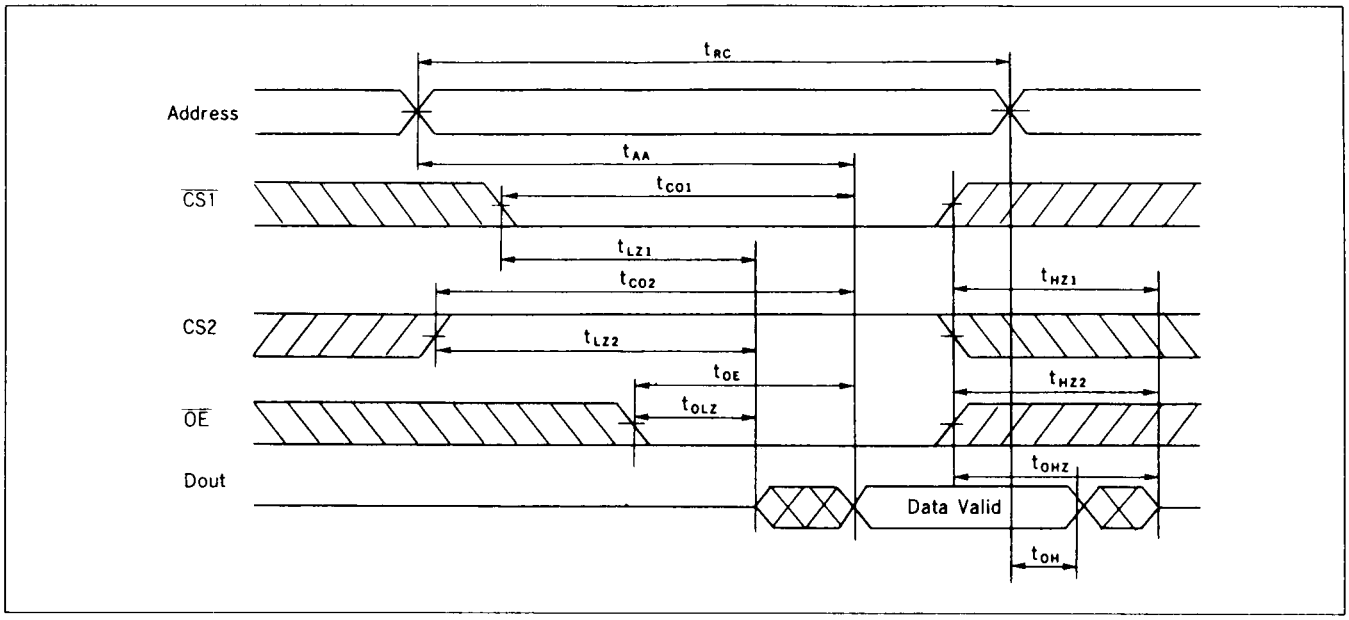
Test Conditions

- Input pulse levels: 0.8 V to 2.4 V
- Input rise and fall times : 5 ns
- Input and output timing reference levels: 1.5 V
- Output load: 1 TTL Gate and CL (100pF) (Including scope & jig)

Read Cycle

Item	Symbol	AKM628128-7		AKM628128-8		AKM628128-10		AKM628128-12		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Read cycle time	t_{RC}	70	—	85	—	100	—	120	—	ns	
Address access time	t_{AA}	—	70	—	85	—	100	—	120	ns	
Chip selection ($\overline{CS1}$) to output valid	t_{CO1}	—	70	—	85	—	100	—	120	ns	
Chip selection (CS2) to output valid	t_{CO2}	—	70	—	85	—	100	—	120	ns	
Output enable ($\overline{OE}$) to output valid	t_{OE}	—	35	—	45	—	50	—	60	ns	
Chip selection ($\overline{CS1}$) to output in low-Z	t_{LZ1}	10	—	10	—	10	—	10	—	ns	*1, *2, *3
Chip selection (CS2) to output in low-Z	t_{LZ2}	10	—	10	—	10	—	10	—	ns	*1, *2, *3
Output enable ($\overline{OE}$) to output in low-Z	t_{OLZ}	5	—	5	—	5	—	5	—	ns	*1, *2, *3
Chip deselection ($\overline{CS1}$) to output in high-Z	t_{HZ1}	0	25	0	30	0	35	0	45	ns	*1, *2, *3
Chip deselection (CS2) to output in high-Z	t_{HZ2}	0	25	0	30	0	35	0	45	ns	*1, *2, *3
Output disable ($\overline{OE}$) to output in high-Z	t_{OHZ}	0	25	0	30	0	35	0	45	ns	*1, *2, *3
Output hold from address change	t_{OH}	10	—	10	—	10	—	10	—	ns	

Read Timing Waveform*4

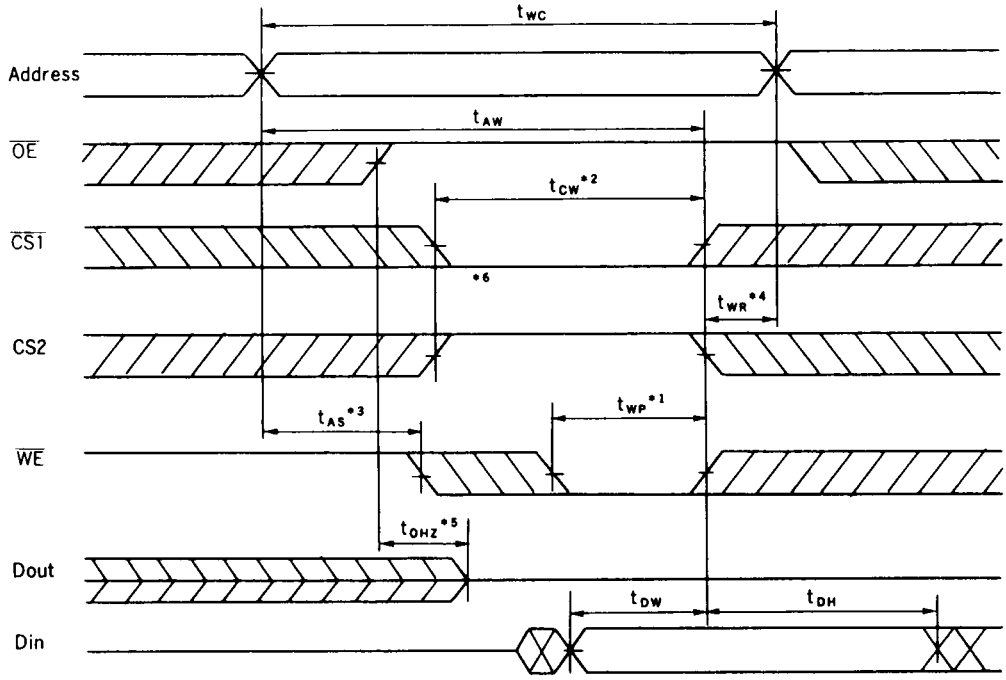


Notes: *1. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
*2. At any given temperature and voltage condition, tHZ max is less than tLZ min both for a given device and from device to device.
*3. This parameter is sampled and not 100% tested.
*4. $\overline{WE}$ is high for read cycle.

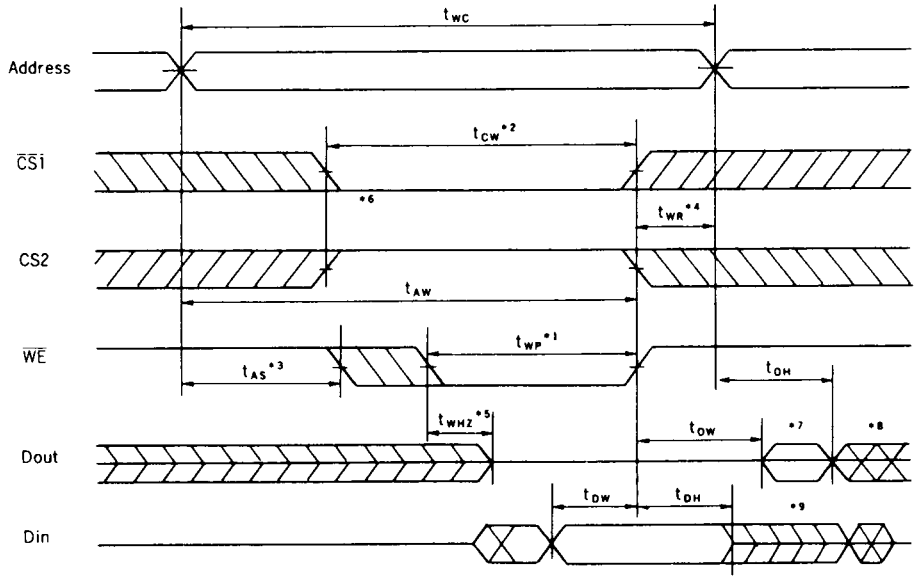
Write Cycle

Item	Symbol	AKM628128-7		AKM628128-8		AKM628128-10		AKM628128-12		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Write cycle time	tWC	70	—	85	—	100	—	120	—	ns	
Chip selection to end of write	tCW	60	—	75	—	90	—	100	—	ns	
Address setup time	tAS	0	—	0	—	0	—	0	—	ns	
Address valid to end of write	tAW	60	—	75	—	90	—	100	—	ns	
Write pulse width	tWP	55	—	65	—	75	—	85	—	ns	
Write recovery time	tWR	5	—	5	—	5	—	10	—	ns	
		10	—	10	—	10	—	15	—	ns	*11
Write to output in high-Z	tWHZ	0	25	0	30	0	35	0	40	ns	*10
Data to write time overlap	tDW	30	—	35	—	40	—	45	—	ns	
Write hold from write time	tDH	0	—	0	—	0	—	0	—	ns	
Output active from end of write	tOW	5	—	5	—	5	—	5	—	ns	*10

Write Timing Waveform (1) ($\overline{OE}$ Clock)



Write Timing Waveform (2) ($\overline{OE}$ Low Fix)



Notes: *1. A write occurs during the overlap of a low $\overline{CS1}$, a high CS2 and a low $\overline{WE}$. A write begins at the latest transition among $\overline{CS1}$ going low, CS2 going high and $\overline{WE}$ going low. A write ends at the earliest transition among $\overline{CS1}$ going high, CS2 going low and $\overline{WE}$ going high. t_{WP} is measured from the beginning of write to the end of write.

*2. t_{CW} is measured from the later of $\overline{CS1}$ going low or CS2 going high to the end of write.

*3. t_{AS} is measured from the address valid to the beginning of write.

*4. t_{WR} is measured from the earliest of $\overline{CS1}$ or $\overline{WE}$ going high or CS2 going low to the end of write cycle.

*5. During this period, I/O pins are in the output state; therefore, the input signals of the opposite phase to the outputs must not be applied.

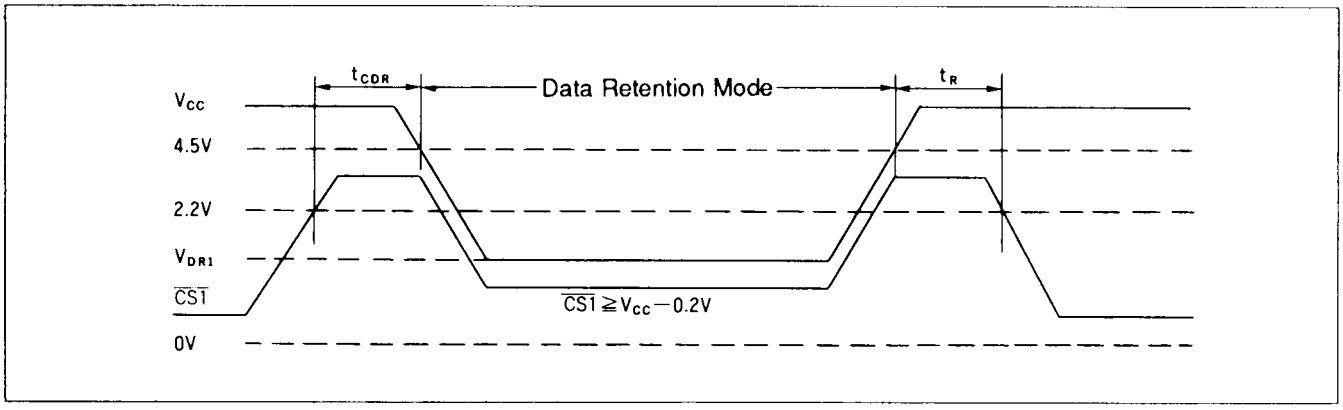
*6. If $\overline{CS1}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain in high impedance state.
*7. Dout is the same phase of the latest written data in this write cycle.
*8. Dout is the read data of next address.
*9. If $\overline{CS1}$ is low and CS2 is high during this period, I/O pins are in the output state. Therefore, the input signals of the opposite phase to the outputs must not be applied to them.
*10. This parameter is sampled and not 100% tested.
*11. This value is measured from CS2 going low to the end of write cycle.

Low Vcc Data Retention Characteristics (Ta = 0 to +70°C)

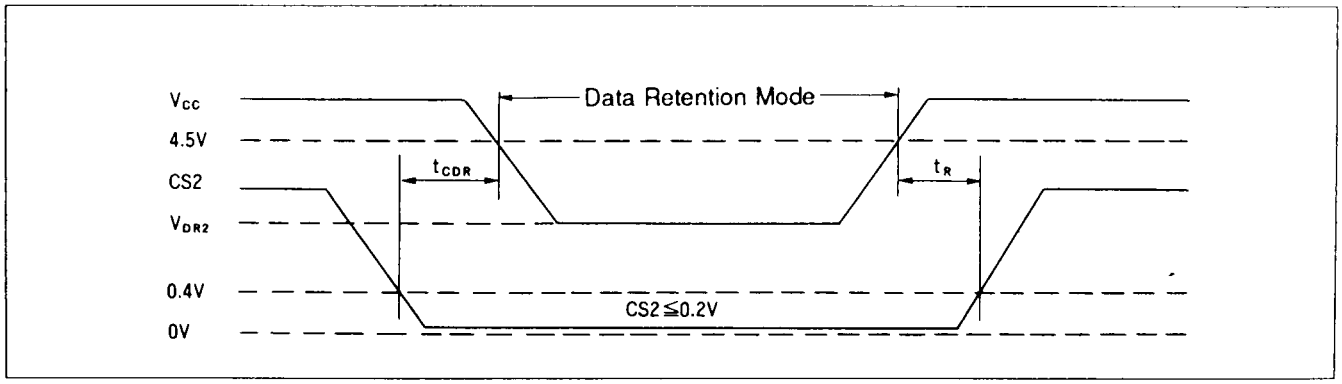
(This characteristics is guaranteed only for L-version.)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions*2
Vcc for data retention	V_{DR}	2.0	—	—	V	$\overline{CS1} \geq Vcc - 0.2$ V, CS2 ≥ Vcc – 0.2 V or 0 V ≤ CS2 ≤ 0.2 V Vin ≥ 0 V
Data retention current	I_{CCDR}	—	1	50*1	µA	Vcc = 3.0 V, Vin ≥ 0 V $\overline{CS1} \geq Vcc - 0.2$ V, CS2 ≥ Vcc – 0.2 V or 0 V ≤ CS2 ≤ 0.2 V
		—	1	30*2		
		—	1	15*3		
Chip deselect to data retention time	t_{CDR}	0	—	—	ns	See Retention Waveform
Operation recovery time	t_R	5	—	—	ms	

Low Vcc Data Retention Timing Waveform (1) ($\overline{CS1}$ Controlled)



Low Vcc Data Retention Timing Waveform (2) (CS2 Controlled)



Notes: *1. 20 µA max at Ta=0 to 40°C, *2. 6 µA max at Ta=0 to 40°C, *3. 3 µA max at Ta=0 to 40°C.
*4. CS2 controls address buffer, $\overline{WE}$ buffer, $\overline{CS1}$ buffer and $\overline{OE}$ buffer and Din buffer. If CS2 controls data retention mode, Vin levels (address, $\overline{WE}$, $\overline{OE}$, $\overline{CS1}$, I/O) can be in the high imepdance state. If $\overline{CS1}$ controls data retention mode, CS2 must be CS2 ≧ Vcc – 0.2 V or 0 V ≦ CS2 ≦ 0.2 V. The other input levels (address, $\overline{WE}$, $\overline{OE}$, I/O) can be in the high impedance state.