National Semiconductor

MM54HC251/MM74HC251
8-Channel TRI-STATE® Multiplexer

General Description

This 8-channel digital multiplexer with TRI-STATE outputs utilizes advanced silicon-gate CMOS technology. Along with the high noise immunity and low power consumption of standard CMOS integrated circuits, it possesses the ability to drive 10 LS-TTL loads. The large output drive capability and TRI-STATE feature make this part ideally suited for interfacing with bus lines in a bus oriented system.

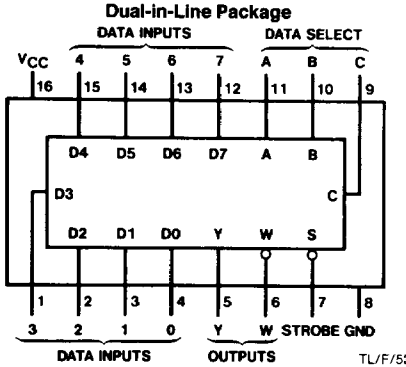
This multiplexer features both true (Y) and complement (W) outputs as well as a STROBE input. The STROBE must be at a low logic level to enable this device. When the STROBE input is high, both outputs are in the high impedance state. When enabled, address information on the data select inputs determines which data input is routed to the Y and W outputs. The 54HC/74HC logic family is speed, function, as well as pinout compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay
  Data select to Y: 26 ns
- Wide supply range: 2–6V
- Low power supply quiescent current: 80 μA maximum (74HC)
- TRI-STATE outputs for interface to bus oriented systems

Connection and Logic Diagrams

Dual-in-Line Package



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Top View

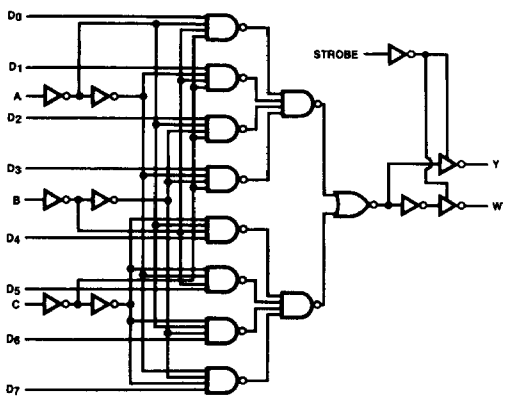
Order Number MM54HC251* or MM74HC251*

*Please look into Section 8, Appendix D for availability of various package types.

Truth Table

Inputs				Outputs	
Select			Strobe		
C	B	A	S	Y	W
X	X	X	H	Z	Z
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

H = high logic level, L = logic level
X = irrelevant, Z = high impedance (off)
D0, D1 . . . D7 = the level of the respective D input



TL/F/5328–2

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D)	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC} = 2.0V		1000	ns
V_{CC} = 4.5V		500	ns
V_{CC} = 6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage**		2.0V		0.5	0.5	0.5	V
			4.5V		1.35	1.35	1.35	V
			6.0V		1.8	1.8	1.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum TRI-STATE Leakage Current	Strobe = V_{CC} V_{OUT} = V_{CC} or GND	6.0V		±0.5	±5	±10	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

**V_{IL} limits are currently tested at 20% of V_{CC}. The above V_{IL} specification (30% of V_{CC}) will be implemented no later than Q1, CY'89.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay A, B or C to Y		26	35	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, A, B or C to W		27	35	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Any D to Y		22	29	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Any D to W		24	32	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time, W Output	$R_L=1$ kΩ $C_L=50$ pF	19	27	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time, Y Output	$R_L=1$ kΩ $C_L=50$ pF	19	26	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time W Output	$R_L=1$ kΩ $C_L=5$ pF	26	40	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time Y Output	$R_L=1$ kΩ $C_L=5$ pF	27	35	ns

AC Electrical Characteristics $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to 85°C	54HC $T_A=-55$ to 125°C	Units
				Typ	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay A, B or C to Y		2.0V 4.5V 6.0V	90 31 26	205 41 35	256 51 44	300 60 51	ns ns ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, A, B or C to W		2.0V 4.5V 6.0V	95 32 27	205 41 35	256 51 44	300 60 51	ns ns ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, any D to Y		2.0V 4.5V 6.0V	70 27 23	195 39 33	244 49 41	283 57 48	ns ns ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, any D to W		2.0V 4.5V 6.0V	75 29 25	185 37 32	231 46 40	268 54 46	ns ns ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time W Output	$R_L=1$ kΩ	2.0V 4.5V 6.0V	45 21 18	150 30 26	188 38 33	218 44 38	ns ns ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time Y Output	$R_L=1$ kΩ	2.0V 4.5V 6.0V	45 21 18	145 29 25	181 36 31	210 42 36	ns ns ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time W Output	$R_L=1$ kΩ	2.0V 4.5V 6.0V	60 29 25	220 44 37	275 55 46	319 64 54	ns ns ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time Y Output	$R_L=1$ kΩ	2.0V 4.5V 6.0V	60 30 26	195 39 33	244 49 41	283 57 48	ns ns ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time		2.0V 4.5V 6.0V	30 8 7	75 15 13	95 19 16	110 22 19	ns ns ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per package)		110				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\,V_{CC}^2\,f+I_{CC}\,V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\,V_{CC}\,f+I_{CC}$.