FAIRCHILD SEMICONDUCTOR™

PRELIMINARY
January 1998

FM27C010
1,048,576-Bit (128K x 8) High Speed CMOS EPROM

General Description

The FM27C010 is a High Performance 128K x 8 UV Erasable EPROM. It is manufactured using an advanced CMOS process technology enabling it to operate at speeds as fast as 25 ns Address Access Time (t_{ACC}). It was designed utilizing Fairchild's Alternate Metal Virtual Ground (AMG) cell. This innovative memory architecture results in a very high performance EPROM.

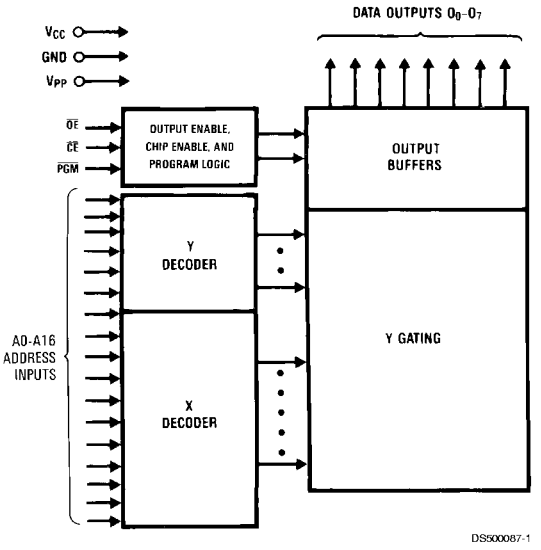
This product, with its high speed capability and high storage capacity is particularly appropriate for use with today's fast DSP processors and high-clock-rate microprocessors. In most mcases the SPU can operate without wait states. The FM27C010 is also designed for use in modem applications. It is an ideal memory for the newest modem chip sets.

The FM27C010 is available in the 600 Mil DIP, the surface mount PLCC and TSOP. Its standard JEDEC EPROM pinouts provide for an easy upgrade for current users of the NM27C010.

Features

- Fast Access Time
  - — t_{ACC} = 25 ns
  - — t_{CE} = 25 ns
- Immune to Latch-Up
  - — Up to 200 mA
- Available in Popular Packages
  - — CERDIP, PDIP, PLCC, TSOP

Block Diagram



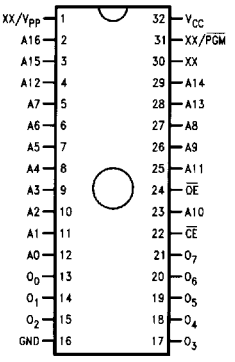
Product Selection Guide

Parameter	27C010-25	27C010-35	27C010-45	27C010-55
Address Access Time (Max)	25 ns	35 ns	45 ns	55 ns
Chip Select Time (Max)	25 ns	35 ns	45 ns	55 ns
Output Enable Time (Max)	12 ns	15 ns	20 ns	25 ns

Connection Diagram

27C040	27C020	27C512	27C256
XX/V_{PP}	XX/V_{PP}		
A16	A16		
A15	A15	A15	V_{PP}
A12	A12	A12	A12
A7	A7	A7	A7
A6	A6	A6	A6
A5	A5	A5	A5
A4	A4	A4	A4
A3	A3	A3	A3
A2	A2	A2	A2
A1	A1	A1	A1
A0	A0	A0	A0
O_0	O_0	O_0	O_0
O_1	O_1	O_1	O_1
O_2	O_2	O_2	O_2
GND	GND	GND	GND

DIP
FM27C010



27C256	27C512	27C020	27C040
		V_{CC}	V_{CC}
		XX/$\overline{PGM}$	A18
V_{CC}	V_{CC}	A17	A17
A14	A14	A14	A14
A13	A13	A13	A13
A8	A8	A8	A8
A9	A9	A9	A9
A11	A11	A11	A11
$\overline{OE}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$
A10	A10	A10	A10
$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}/\overline{PGM}$
O_7	O_7	O_7	O_7
O_6	O_6	O_6	O_6
O_5	O_5	O_5	O_5
O_4	O_4	O_4	O_4
O_3	O_3	O_3	O_3

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Note: Compatible EPROM pin configurations are shown in the blocks adjacent to the FM27C010 pins.

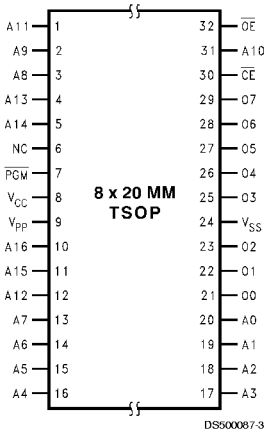
Commercial Temp. Range (0˚C to +70˚C) V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
FM27C010 Q, V, T 25	25
FM27C010 Q, V, T 35	35
FM27C010 Q, V, T 45	45
FM27C010 Q, V, T 55	55

Extended Temp. Range (–40˚C to +85˚C) V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
FM27C010 QE, VE, TE 45	45
FM27C010 QE, VE, TE 55	55

TSOP Pin Configuration



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Package Types: FM27C010 N, Q, V, T

N = Plastic DIP package

Q = Quartz-Windowed Ceramic DIP package

V = PLCC package

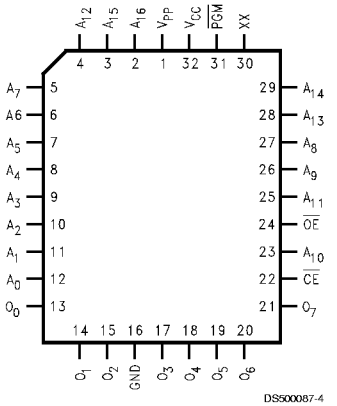
T = TSOP package

• All packages conform to the JEDEC standard.

Pin Names

Symbol	Description
A0–A16	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
O0–O7	Outputs
$\overline{PGM}$	Program
XX	Don't Care (during Read)

PLCC Pin Configuration



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Top View

Absolute Maximum Ratings (Note 1)

Storage Temperature	−65°C to +125°C
All Input Voltages except A9 with Respect to Ground	−0.6V to +7V
V_{PP} and A_9 with Respect to Ground	−0.6V to +14V
V_{CC} Supply Voltage with Respect to Ground	− 0.6V to +7V
ESD Protection	> 2000V
All Output Voltages with Respect to Ground	V_{CC} + 1.0V to GND − 0.6V

Operating Range

Range	Temperature	V_{CC}	Tolerance
Commercial	0°C to +70°C	+5V	±10%
Industrial	−40°C to +85°C	+5V	±10%

Read Operation

DC Electrical Characteristics

(V_{CC} = 5.0 V ± 0.5 V)

Symbol	Parameter	Test Conditions		Min	Max	Units
V_{IL}	Input Low Voltage			−0.3	0.8	V
V_{IH}	Input High Voltage			2.0	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 12 mA			0.45	V
V_{OH}	Output High Voltage	I_{OH} = −4 mA		2.4		V
I_{SB}	V_{CC}Standby Quiescent Current (CMOS)	$\overline{CE} \geq V_{CC}$ − 0.3 V All Pins ≥ V_{CC} − 0.3 V or ≤ 0.3 V (All Inputs Fixed, No Switching)	Comm'l		100	µA
			Industrial		150	µA
I_{CCSB0}	V_{CC} Standby Current (CMOS)	$\overline{CE} \geq V_{CC}$ − 0.3 V All Pins ≥ V_{CC} − 0.3 V or ≤ 0.3 V (Toggling) f ≤ 10 MHz	Comm'l		10	mA
			Industrial		15	mA
I_{CCSB1}	V_{CC} Standby Current (TTL)	$\overline{CE} \geq V_{IH}$ All Pins = V_{IH} or V_{IL} (Toggling) f ≤ 10 MHz	Comm'l		20	mA
			Industrial		25	mA
I_{CC1}	V_{CC} Active Current	$\overline{CE}$ = V_{IL} f ≤ 10 MHz I_{OUT} = 0 mA (Open Outputs)	Comm'l		25	mA
			Industrial		30	mA
I_{PP1}	V_{PP} Current During Read	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, V_{PP} = V_{CC}			10	µA
I_{LI}	Input Leakage Current	0 V < V_{IN} < 5.5V		−10	10	µA
I_{LO}	Output Leakage Current	0 V < V_{OUT} < 5.5V		−10	10	µA

Note 1: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: I_{CC1} is tested with $\overline{OE}$ = V_{IH} to simulate open outputs.

Note 3: The FM27C010 device employs high speed output drivers, which can produce transient voltages at the device ground pin when discharging load capacitances through parasitic inductance between device ground and system ground. These transient voltages can result in significant reductions in measured input relay margins, particularly V_{IL}. Special care should be taken to minimize the inductance of the current path from device ground to system ground (by use of a ground place or grid) and to eliminate ground loops, especially where multiple FM27C010 devices are used in a synchronous design.

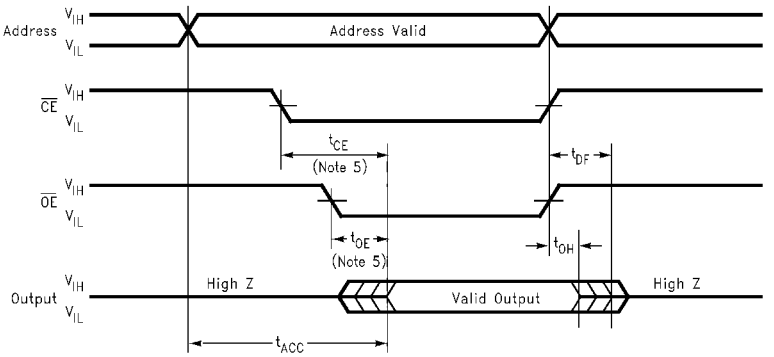
AC Read Characteristics

V_{CC} = 5.0 V ± 0.5 V, V_{PP} = V_{CC}

Symbol	Parameter	-25		-35		-45		-55		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay		25		35		45		55	ns
t_{CE}	Chip Enable to Output Delay		25		35		45		55	ns
t_{OE}	Output Enable to Output Delay		12		15		20		25	ns
t_{DF}	Output Disable to Output Float (Note 4)		12		15		20		25	ns
t_{OH}	Output Hold	0		0		0		0		ns

Note 4: This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is not longer driven - see timing diagram.

AC Waveforms (Note 5)



Note 5: $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE}.

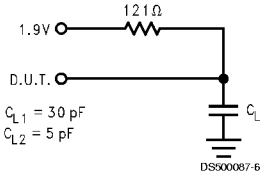
Capacitance (Note 6)

T_A = +25˚C, f = 1 MHz

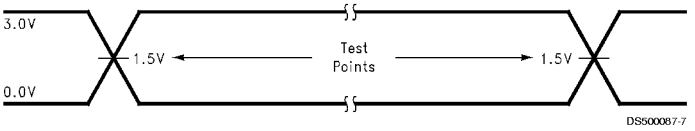
Symbol	Parameter	Conditions	Typ (Note 6)	Max	Units
C_{IN}	Input Capacitance	V_{IN} = 0V	4	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF
C_{VPP}	V_{PP} Capacitance	V_{PP} = oV	18	25	pF

Note 6: Typical values are for T_A = 25˚C and nominal supply voltages.

Test Load (High Impedance Test Systems)



AC Testing Input/Output Waveform



AC testing inputs are driven at 3.0 V for a logic "1" and 0.0 V for a logic "0." Timing measurements are made at 1.5 V for input and output transitions in both directions.

Note 7: Provide adequate decoupling capacitance as close as possible to this device to achieve the published AC and DC parameters. A 0.1 microfarad capacitor in parallel with a 0.01 microfarad capacitor connected between V_{CC} and ground is recommended. Inadequate decoupling may result in access time degradation or other transient performance failures.

DC Programming Characteristics (Note 8), (Note 9), and (Note 10)

(T_A = 25˚C ± 5˚C, V_{CC} = 6.25 ± 0.25 V, V_{PP} = 12.75 ± 0.25V)

Symbol	Parameter	Min	Max	Units
I_{LI}	Input Capacitance	−10	10	µA
I_{PP}	Output Capacitance		60	mA
I_{CC}	V_{PP} Capacitance		50	mA
V_{OL}	Output Low Voltage During Verify (I_{OL} = 12 mA)		0.45	V
V_{OH}	Output High Voltage During Verify (I_{OH} = −4 mA)	2.4		V

Note 8: V_{CC} must be applied coincidentally or before V_{PP} and removed coincidentally or after V_{PP}.

Note 9: V_{PP} must not be greater than 13 volts including overshoot. During $\overline{CE}$ = $\overline{PGM}$ = V_{IL}, V_{PP} must not be switched from 5 volts to 12.75 volts or vice-versa.

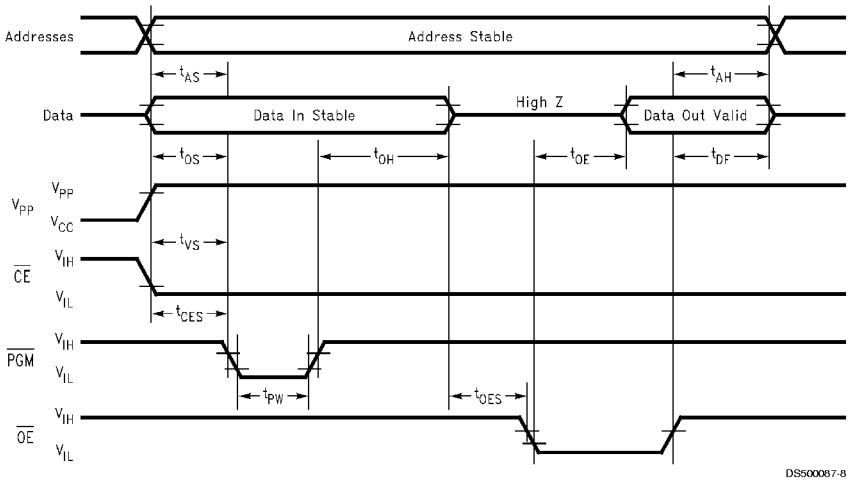
Note 10: During power up the $\overline{PGM}$ pin must be brought high (≥ V_{IH}) either coincident with or before power is applied to V_{PP}.

AC Programming Characteristics

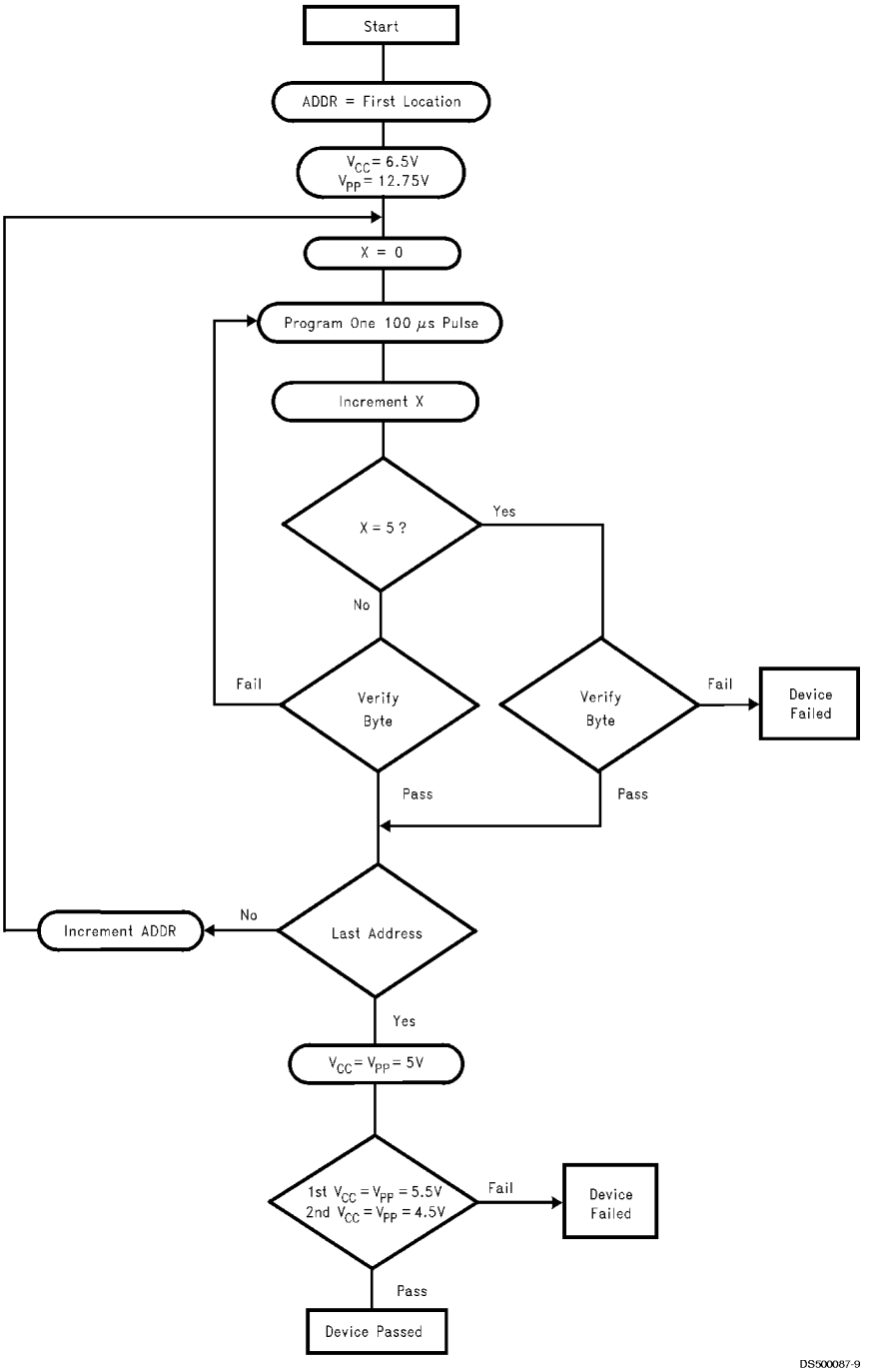
(T_A = 25˚C ± 5˚C, V_{CC} = 6.25 ± 0.25 V, V_{PP} = 12.75 ± 0.25V)

Symbol	Parameter	Min	Typ	Max	Units
t_{AS}	Address Setup Time	2			µs
t_{OES}	Output Enable Setup Time	2			µs
t_{OS}	Data Setup Time	2			µs
t_{AH}	Address Hold Time	0			µs
t_{OH}	Data Hold Time	2			µs
t_{DF}	Chip Disable to Output Float Delay	0		55	ns
t_{OE}	Data Valid from Output Enable			55	ns
t_{VS}/t_{CES}	V_{PP} Setup Time/$\overline{CE}$ Setup Time	2			µs
t_{PW}	$\overline{PGM}$ Pulse Width	0.1		1	ms

Programming Waveform



Fast Programming Algorithm



Note: Turbo Programming Algorithm will be available in Quarter 1, 1998 - Please check with Factory.

Mode Selection

The modes of operation of FM27C010 listed below. A single 5V power supply is required in the read mode. All inputs are TTL levels except for V_{PP} and A_9 for device signature.

TABLE 1. Modes Selection

Pins / Mode	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	A_9	A_0	V_{PP}	V_{CC}	Outputs
Read	V_{IL}	V_{IL}	X (Note 11)	X	X	X	5.0 V	D_{OUT}
Output Disable	X	V_{IH}	X	X	X	X	5.0 V	High Z
Standby	V_{IH}	X	X	X	X	X	5.0 V	High Z
Program	V_{IL}	V_{IH}	V_{IL}	X	X	V_{PP} (Note 12)	6.25 V	D_{IN}
Program Verify	V_{IL}	V_{IL}	V_{IH}	X	X	V_{PP} (Note 12)	6.25 V	D_{OUT}
Program Inhibit	V_{IH}	X	X	X	X	V_{PP} (Note 12)	5.0 V	High Z
Manufacturer Signature (Note 13)	V_{IL}	V_{IL}	X	V_{IH} (Note 12)	V_{IL}	X	5.0 V	23 H
Device Signature (Note 13)	V_{IL}	V_{IL}	X	V_{IH} (Note 12)	V_{IH}	X	5.0 V	F8 H

Note 11: X can be V_{IL} or V_{IH}.

Note 12: $V_{IH} = V_{PP} = 12.75 \pm 0.25$ V.

Note 13: A1 - A8, A10 - A14 = V_{IL}.

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