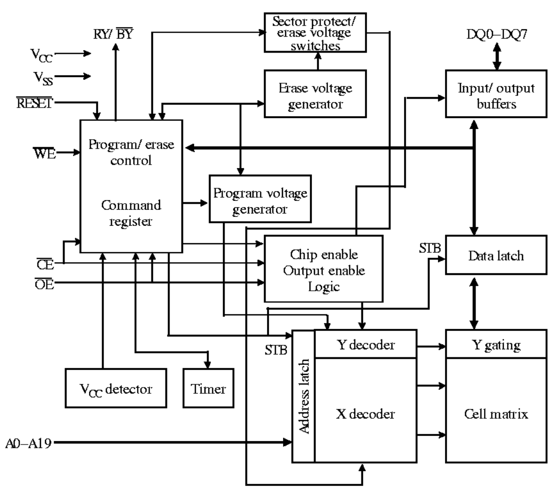
3V 1M×8 CMOS Flash EEPROM

Features

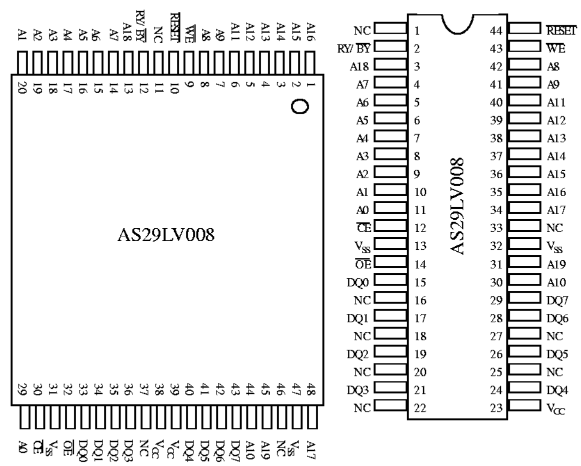
- Organization: 1M×8
- Sector architecture
  - One 16K; two 8K; one 32K; and fifteen 64K byte sectors
  - Boot code sector architecture—T (top) or B (bottom)
  - Erase any combination of sectors or full chip
- Single 2.7-3.6V power supply for read/ write operations
- Sector protection
- High speed 80/ 100/ 120/ 150 ns address access time
- Automated on-chip programming algorithm
  - Automatically programs/ verifies data at specified address
- Automated on-chip erase algorithm
  - Automatically preprograms/ erases chip or specified sectors
- 10,000 write/ erase cycle endurance
- Hardware $\overline{\text{RESET}}$ pin
  - Resets internal state machine to read mode
- Low power consumption
  - 10 mA typical read current
  - 30 mA typical program current
  - 1 µA typical standby current
  - 1 µA typical automatic sleep mode current
- JEDEC standard software, packages and pinouts
  - 40-pin TSOP
  - 44-pin SO
- Detection of program/ erase cycle completion
  - DQ7 $\overline{\text{DATA}}$ polling
  - DQ6 toggle bit
  - DQ2 toggle bit
  - RY/ $\overline{\text{BY}}$ output
- Erase suspend/ resume
  - Supports reading data from or programming data to a sector not being erased
- Low V_{CC} write lock-out below 1.5V

Logic block diagram



Pin arrangement

40-pin TSOP 44-pin SO



Selection guide

		29LV008-80	29LV008-100	29LV008-120	29LV008-150	Unit
Maximum access time	t_{AA}	80	100	120	150	ns
Maximum chip enable access time	t_{CE}	80	100	120	150	ns
Maximum output enable access time	t_{OE}	30	40	50	50	ns

Functional description

The AS29LV008 is an 8 megabit, 3.0 volt only Flash memory organized as 1 Megabyte of 8 bits each. For flexible erase and program capability, the 8 megabits of data is divided into nineteen sectors: one 16K, two 8K, one 32K, and fifteen 64k byte sectors. The data appears on DQ0–DQ7. The AS29LV008 is offered in JEDEC standard 40-pin TSOP and 44-pin SO packages. This device is designed to be programmed and erased in-system with a single 3.0V V_{CC} supply. The device can also be reprogrammed in standard EPROM programmers.

The AS29LV008 offers access times of 80/100/120/150 ns, allowing 0-wait state operation of high speed microprocessors. To eliminate bus contention the device has separate chip enable ($\overline{CE}$), write enable ($\overline{WE}$), and output enable ($\overline{OE}$) controls.

The AS29LV008 is fully compatible with the JEDEC single power supply Flash standard. Write commands to the command register using standard microprocessor write timings. An internal state-machine uses register contents to control the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the programming and erase operations. Read data from the device in the same manner as other Flash or EPROM devices. Use the program command sequence to invoke the automated on-chip programming algorithm that automatically times the program pulse widths and verifies proper cell margin. Use the erase command sequence to invoke the automated on-chip erase algorithm that preprograms the sector if it is not already programmed before executing the erase operation, times the erase pulse widths, and verifies proper cell margin.

Boot sector architecture enables the system to boot from either the top (AS29LV008T) or the bottom (AS29LV008B) sector. Sector erase architecture allows specified sectors of memory to be erased and reprogrammed without altering data in other sectors. A sector typically erases and verifies within 1.5 seconds. Hardware sector protection disables both program and erase operations in all or any combination of the nineteen sectors. The device provides true background erase with Erase Suspend, which puts erase operations on hold to either read data from or program data to a sector that is not being erased. The chip erase command will automatically erase all unprotected sectors.

A factory shipped AS29LV008 is fully erased (all bits = 1). The programming operation sets bits to 0. Data is programmed into the array one byte at a time in any sequence and across sector boundaries. A sector must be erased to change bits from 0 to 1. Erase returns all bytes in a sector to the erased state (all bits = 1). Each sector is erased individually with no effect on other sectors.

The device features single 3.0V power supply operation for read, write, and erase functions. Internally generated and regulated voltages are provided for the program and erase operations. A low V_{CC} detector automatically inhibits write operations during power transtitions. The RY/$\overline{BY}$ pin, $\overline{DATA}$ polling of DQ7, or toggle bit (DQ6) may be used to detect end of program or erase operations. The device automatically resets to the read mode after program/erase operations are completed. DQ2 indicates which sectors are being erased.

The AS29LV008 resists accidental erasure or spurious programming signals resulting from power transitions. Control register architecture permits alteration of memory contents only after successful completion of specific command sequences. During power up, the device is set to read mode with all program/erase commands disabled when V_{CC} is less than V_{LKO} (lockout voltage). The command registers are not affected by noise pulses of less than 5 ns on $\overline{OE}$, $\overline{CE}$, or $\overline{WE}$. To initiate write commands, $\overline{CE}$ and $\overline{WE}$ must be logical zero and $\overline{OE}$ a logical one.

When the device's hardware $\overline{RESET}$ pin is driven low, any program/erase operation in progress will be terminated and the internal state machine will be reset to read mode. If the $\overline{RESET}$ pin is tied to the system reset circuitry and a system reset occurs during an automated on-chip program/erase algorithm, data in address locations being operated on will become corrupted and require rewriting. Resetting the device enables the system's microprocessor to read boot-up firmware from the Flash memory.

The AS29LV008 uses Fowler-Nordheim tunnelling to electrically erase all bits within a sector simultaneously. Bytes are programmed one at a time using EPROM programming mechanism of hot electron injection.

Operating modes

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	A0	A1	A6	A9	$\overline{RESET}$	DQ
ID read MFR code	L	L	H	L	L	L	V_{ID}	H	Code
ID read device code	L	L	H	H	L	L	V_{ID}	H	Code
Read	L	L	H	A0	A1	A6	A9	H	D_{OUT}
Standby	H	X	X	X	X	X	X	H	High Z
Output disable	L	H	H	X	X	X	X	H	High Z
Write	L	H	L	A0	A1	A6	A9	H	D_{IN}
Enable sector protect	L	V_{ID}	Pulse/ L	L	H	L	V_{ID}	H	X
Sector unprotect	L	V_{ID}	Pulse/ L	L	H	H	V_{ID}	H	X
Temporary sector unprotect	X	X	X	X	X	X	X	V_{ID}	X
Verify sector protect†	L	L	H	L	H	L	V_{ID}	H	Code
Hardware Reset	X	X	X	X	X	X	X	L	High Z

L = Low (<V_{IL}) = logic 0; H = High (>V_{IH}) = logic 1; V_{ID} = 10.0 ± 1.0V; X = don't care.

†Verification of sector protect during A9 = V_{ID}.

Mode definitions

Item	Description
ID MFR code, device code	Selected by A9 = V_{ID}(11.5–12.5V), $\overline{CE}$ = $\overline{OE}$ = A1 = A6 = L, enabling outputs. When A0 is low (V_{IL}) the output data = 52h, a unique Mfr. code for Alliance Semiconductor Flash products. When A0 is high (V_{IH}), D_{OUT} represents the device code for the AS29LV008.
Read mode	Selected with $\overline{CE}$ = $\overline{OE}$ = L, $\overline{WE}$ = H. Data is valid in t_{ACC} time after addresses are stable, t_{CE} after $\overline{CE}$ is low and t_{OE} after $\overline{OE}$ is low.
Standby	Selected with $\overline{CE}$ = H. Part is powered down, and I_{CC} reduced to <1.0 µA when $\overline{CE}$ = V_{CC} ± 0.3V = $\overline{RESET}$. If activated during an automated on-chip algorithm, the device completes the operation before entering standby.
Output disable	Part remains powered up; but outputs disabled with $\overline{OE}$ pulled high.
Write	Selected with $\overline{CE}$ = $\overline{WE}$ = L, $\overline{OE}$ = H. Accomplish all Flash erasure and programming through the command register. Contents of command register serve as inputs to the internal state machine. Address latching occurs on the falling edge of $\overline{WE}$ or $\overline{CE}$, whichever occurs later. Data latching occurs on the rising edge $\overline{WE}$ or $\overline{CE}$, whichever occurs first. Filters on $\overline{WE}$ prevent spurious noise events from appearing as write commands.
Enable sector protect	Hardware protection circuitry implemented with external programming equipment causes the device to disable program and erase operations for specified sectors.
Sector unprotect	Disables sector protection for all sectors using external programming equipment. All sectors must be protected prior to sector unprotection.
Verify sector protect	Verifies write protection for sector. Sectors are protected from program/ erase operations on commercial programming equipment. Determine if sector protection exists in a system by writing the ID read command sequence and reading location XXX02h, where address bits A13–19 select the defined sector addresses. A logical 1 on DQ0 indicates a protected sector; a logical 0 indicates an unprotected sector.
Temporary sector unprotect	Temporarily disables sector protection for in-system data changes to protected sectors. Apply +12V to $\overline{RESET}$ to activate temporary sector unprotect mode. During temporary sector unprotect mode, program protected sectors by selecting the appropriate sector address. All protected sectors revert to protected state on removal of +12V from $\overline{RESET}$.

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Item	Description
$\overline{RESET}$	Resets the interal state machine to read mode. If device is programming or erasing when $\overline{RESET}$ = L, data may be corrupted.
Deep power down	Hold $\overline{RESET}$ low to enter deep power down mode (<1 µA). Recovery time to start of first read cycle is 50ns.
Automatic sleep mode	Enabled automatically when addresses remain stable for 300ns. Typical current draw is 1 µA. Existing data is available to the system during this mode. If an address is changed, automatic sleep mode is disabled and new data is returned within standard access times.

Flexible sector architecture

	Bottom boot sector architecture (AS29LV008B)		Top boot sector architecture (AS29LV008T)	
Sector	×8	Size (Kbytes)	×8	Size (Kbytes)
0	00000h–03FFFh	16	00000h–0FFFFh	64
1	04000h–05FFFh	8	10000h–1FFFFh	64
2	06000h–07FFFh	8	20000h–2FFFFh	64
3	08000h–0FFFFh	32	30000h–3FFFFh	64
4	10000h–1FFFFh	64	40000h–4FFFFh	64
5	20000h–2FFFFh	64	50000h–5FFFFh	64
6	30000h–3FFFFh	64	60000h–6FFFFh	64
7	40000h–4FFFFh	64	70000h–7FFFFh	64
8	50000h–5FFFFh	64	80000h–8FFFFh	64
9	60000h–6FFFFh	64	90000h–9FFFFh	64
10	70000h–7FFFFh	64	A0000h–AFFFFh	64
11	80000h–8FFFFh	64	B0000h–BFFFFh	64
12	90000h–9FFFFh	64	C0000h–CFFFFh	64
13	A0000h–AFFFFh	64	D0000h–DFFFFh	64
14	B0000h–BFFFFh	64	E0000h–EFFFFh	64
15	C0000h–CFFFFh	64	F0000h–F7FFFh	32
16	D0000h–DFFFFh	64	F8000h–F9FFFh	8
17	E0000h–EFFFFh	64	FA000h–FBFFFh	8
18	F0000h–FFFFFh	64	FC000h–FFFFFh	16

The address range is A19–A0.

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ID Sector address table

Sector	Bottom boot sector address (AS29LV008B) A19	A18	A17	A16	A15	A14	A13	Top boot sector address (AS29LV008T) A19	A18	A17	A16	A15	A14	A13
0	0	0	0	0	0	0	X	0	0	0	0	X	X	X
1	0	0	0	0	0	1	0	0	0	0	1	X	X	X
2	0	0	0	0	0	1	1	0	0	1	0	X	X	X
3	0	0	0	0	1	X	X	0	0	1	1	X	X	X
4	0	0	0	1	X	X	X	0	1	0	0	X	X	X
5	0	0	1	0	X	X	X	0	1	0	1	X	X	X
6	0	0	1	1	X	X	X	0	1	1	0	X	X	X
7	0	1	0	0	X	X	X	0	1	1	1	X	X	X
8	0	1	0	1	X	X	X	1	0	0	0	X	X	X
9	0	1	1	0	X	X	X	1	0	0	1	X	X	X
10	0	1	1	1	X	X	X	1	0	1	0	X	X	X
11	1	0	0	0	X	X	X	1	0	1	1	X	X	X
12	1	0	0	1	X	X	X	1	1	0	0	X	X	X
13	1	0	1	0	X	X	X	1	1	0	1	X	X	X
14	1	0	1	1	X	X	X	1	1	1	0	X	X	X
15	1	1	0	0	X	X	X	1	1	1	1	0	X	X
16	1	1	0	1	X	X	X	1	1	1	1	1	0	0
17	1	1	1	0	X	X	X	1	1	1	1	1	0	1
18	1	1	1	1	X	X	X	1	1	1	1	1	1	X

READ codes

Mode		A19–A13	A6	A1	A0	Code
MFR code (Alliance Semiconductor)		X	L	L	L	52h
Device code	×8 T boot	X	L	L	H	3Eh
	×8 B boot	X	L	L	H	37h
Sector protection		Sector address	L	H	L	01h protected 00h unprotected

Key: L=Low (<V_{IL}); H = High (>V_{IH}); X=Don't care

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Command format

Command sequence	Required bus write cycles	1st bus cycle Address	1st bus cycle Data	2nd bus cycle Address	2nd bus cycle Data	3rd bus cycle Address	3rd bus cycle Data	4th bus cycle Address	4th bus cycle Data	5th bus cycle Address	5th bus cycle Data	6th bus cycle Address	6th bus cycle Data
Reset/ Read	1	XXXh	F0h	Read Address	Read Data								
Reset/ Read	3	555h	AAh	2AAh	55h	555h	F0h	Read Address	Read Data				
Autoselect ID Read	3	555h	AAh	2AAh	55h	555h	90h	01h Device code	3Eh (T) 37h (B)				
								00h MFR code	52h				
								XXX02h Sector protection	01 = protected 00 = unprotected				
Program	4	555h	AAh	2AAh	55h	555h	A0h	Program Address	Program Data				
Chip Erase	6	555h	AAh	2AAh	55h	555h	80h	555h	AAh	2AAh	55h	555h	10h
Sector Erase	6	555h	AAh	2AAh	55h	555h	80h	555h	AAh	2AAh	55h	Sector Address	30h
Sector Erase Suspend	1	XXXh	B0h										
Sector Erase Resume	1	XXXh	30h										

1 Bus operations defined in "Mode definitions," on page 3.

2 Reading from and programming to non-erasing sectors allowed in Erase Suspend mode.

3 Address bits A19–A11 = X = Don't Care for all address commands except Program Address and Sector Address.

Command definitions

Item	Description
Reset/ Read	Initiate read or reset operations by writing the Read/ Reset command sequence into the command register. This allows the microprocessor to retrieve data from the memory. Device remains in read mode until command register contents are altered. Device automatically powers up in read/ reset state. This feature allows only reads, therefore ensuring no spurious memory content alterations during power up.
ID Read	AS29LV008 provides manufacturer and device codes in two ways. External PROM programmers typically access the device codes by driving +10V on A9. AS29LV008 also contains an ID Read command to read the device code with only +3V, since multiplexing +10V on address lines is generally undesirable. Initiate device ID read by writing the ID Read command sequence into the command register. Follow with a read sequence from address XXX00h to return MFR code. Follow ID Read command sequence with a read sequence from address XXX01h to return device code. To verify write protect status on sectors, read address XXX02h. Sector addresses A19–A13 produce a 1 on DQ0 for protected sector and a 0 for unprotected sector. Exit from ID read mode with Read/ Reset command sequence.
Hardware Reset	Holding $\overline{RESET}$ low for 500 ns resets the device, terminating any operation in progress; data handled in the operation is corrupted. The internal state machine resets 10 µs after $\overline{RESET}$ is driven low. RY/ $\overline{BY}$ remains low until internal state machine resets. After $\overline{RESET}$ is set high, there is a delay of 50 ns for the device to permit read operations.

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Item	Description
Byte programming	Programming the AS29LV008 is a four bus cycle operation performed on a byte-by-byte basis. Two unlock write cycles precede the Program Setup command and program data write cycle. Upon execution of the program command, no additional CPU controls or timings are necessary. Addresses are latched on the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever is last; data is latched on the rising edge of $\overline{CE}$ or $\overline{WE}$, whichever is first. The AS29LV008's automated on-chip program algorithm provides adequate internally-generated programming pulses and verifies the programmed cell margin. Check programming status by sampling data on the RY/$\overline{BY}$ pin, or either the $\overline{DATA}$ polling (DQ7) or toggle bit (DQ6) at the program address location. The programming operation is complete if DQ7 returns equivalent data, if DQ6 = no toggle, or if RY/$\overline{BY}$ pin = high. The AS29LV008 ignores commands written during programming. A hardware reset occurring during programming may corrupt the data at the programmed location. AS29LV008 allows programming in any sequence, across any sector boundary. Changing data from 0 to 1 requires an erase operation. Attempting to program data 0 to 1 results in either DQ5 = 1 (exceeded programming time limits); reading this data after a read/reset operation returns a 0. When programming time limit is exceeded, DQ5 reads high, and DQ6 continues to toggle. In this state, a Reset command returns the device to read mode.
Chip Erase	Chip erase requires six bus cycles: two unlock write cycles; a setup command, two additional unlock write cycles; and finally the Chip Erase command. Chip erase does not require logical 0s to be written prior to erasure. When the automated on-chip erase algorithm is invoked with the Chip Erase command sequence, AS29LV008 automatically programs and verifies the entire memory array for an all-zero pattern prior to erase. The 29LV008 returns to read mode upon completion of chip erase unless DQ5 is set high as a result of exceeding time limit.
Sector Erase	Sector erase requires six bus cycles: two unlock write cycles, a setup command, two additional unlock write cycles, and finally the Sector Erase command. Identify the sector to be erased by addressing any location in the sector. The address is latched on the falling edge of $\overline{WE}$; the command, 30h is latched on the rising edge of $\overline{WE}$. The sector erase operation begins after a sector erase time-out. To erase multiple sectors, write the Sector Erase command to each of the addresses of sectors to erase after following the six bus cycle operation above. Timing between writes of additional sectors must be less than the erase time-out period, or the AS29LV008 ignores the command and erasure begins. During the time-out period any falling edge of $\overline{WE}$ resets the time-out. Any command (other than Sector Erase or Erase Suspend) during time-out period resets the AS29LV008 to read mode, and the device ignores the sector erase command string. Erase such ignored sectors by restarting the Sector Erase command on the ignored sectors. The entire array need not be written with 0s prior to erasure. AS29LV008 writes 0s to the entire sector prior to electrical erase; writing of 0s affects only selected sectors, leaving non-selected sectors unaffected. AS29LV008 requires no CPU control or timing signals during sector erase operations. Automatic sector erase begins after sector erase time-out from the last rising edge of $\overline{WE}$ from the sector erase command stream and ends when the $\overline{DATA}$ polling (DQ7) is logical 1. $\overline{DATA}$ polling address must be performed on addresses that fall within the sectors being erased. AS29LV008 returns to read mode after sector erase unless DQ5 is set high by exceeding the time limit.

Item	Description
Erase Suspend	Erase Suspend allows interruption of sector erase operations to read data from or program data to a sector not being erased. Erase suspend applies only during sector erase operations, including the time-out period. Writing an Erase Suspend command during sector erase time-out results in immediate termination of the time-out period and suspension of erase operation. AS29LV008 ignores any commands during erase suspend other than Read/ Reset, Program or Erase Resume commands. Writing the Erase Resume Command continues erase operations. Addresses are Don't Care when writing Erase Suspend or Erase Resume commands. AS29LV008 takes less than 10ns to suspend erase operations after receiving Erase Suspend command. To determine completion of erase suspend, either check DQ6 after selecting an address of a sector not being erased, or poll RY/ $\overline{\text{BY}}$. Check DQ2 in conjunction with DQ6 to determine if a sector is being erased. AS29LV008 ignores redundant writes of Erase Suspend. While in erase-suspend mode, AS29LV008 allows reading data (erase-suspend-read mode) from or programming data (erase-suspend-program mode) to any sector not undergoing sector erase; these operations are treated as standard read or standard programming mode. AS29LV008 defaults to erase-suspend-read mode while an erase operation has been suspended. Write the Resume command 30h to continue operation of sector erase. AS29LV008 ignores redundant writes of the Resume command. AS29LV008 permits multiple suspend/ resume operations during sector erase.
Sector Protect	When attempting to write to a protected sector, $\overline{\text{DATA}}$ polling and Toggle Bit 1 (DQ6) are activated for about <1 µs. When attempting to erase a protected sector, $\overline{\text{DATA}}$ polling and Toggle Bit 1 (DQ6) are activated for about <5 µs. In both cases, the device returns to read mode without altering the specified sectors.
Ready/ Busy	RY/ $\overline{\text{BY}}$ indicates whether an automated on-chip algorithm is in progress (RY/ $\overline{\text{BY}}$ = low) or completed (RY/ $\overline{\text{BY}}$ = high). The device does not accept Program/ Erase commands when RY/ $\overline{\text{BY}}$ = low. RY/ $\overline{\text{BY}}$= high when device is in erase suspend mode. RY/ $\overline{\text{BY}}$ = high when device exceeds time limit, indicating that a program or erase operation has failed. RY/ $\overline{\text{BY}}$ is an open drain output, enabling multiple RY/ $\overline{\text{BY}}$ pins to be tied in parallel with a pull up resistor to V_{CC}.

Status operations

$\overline{\text{DATA}}$ polling (DQ7)	Only active during automated on-chip algorithms or sector erase time outs. DQ7 reflects complement of data last written when read during the automated on-chip program algorithm (0 during erase algorithm); reflects true data when read after completion of an automated on-chip program algorithm (1 after completion of erase agorithm).
Toggle bit 1 (DQ6)	Active during automated on-chip algorithms or sector erase time outs. DQ6 toggles when $\overline{\text{CE}}$ or $\overline{\text{OE}}$ toggles, or an Erase Resume command is invoked. DQ6 is valid after the rising edge of the fourth pulse of $\overline{\text{WE}}$ during programming; after the rising edge of the sixth $\overline{\text{WE}}$ pulse during chip erase; after the last rising edge of the sector erase $\overline{\text{WE}}$ pulse for sector erase. For protected sectors, DQ6 toggles for <1 µs during program mode writes, and <5 µs during erase (if all selected sectors are protected).
Exceeding time limit (DQ5)	Indicates unsuccessful completion of program/ erase operation (DQ5 = 1). $\overline{\text{DATA}}$ polling remains active. If DQ5 = 1 during chip erase, all or some sectors are defective; during byte programming or sector erase, the sector is defective (in this case, reset the device and execute a program or erase command sequence to continue working with functional sectors). Attempting to program 0 to 1 will set DQ5 = 1.

Sector erase timer (DQ3)	Checks whether sector erase timer window is open. If DQ3 = 1, erase is in progress; no commands will be accepted. If DQ3 = 0, the device will accept sector erase commands. Check DQ3 before and after each Sector Erase command to verify that the command was accepted.
Toggle bit 2 (DQ2)	During sector erase, DQ2 toggles with $\overline{OE}$ or $\overline{CE}$ only during an attempt to read a sector being erased. During chip erase, DQ2 toggles with $\overline{OE}$ or $\overline{CE}$ for all addresses. If DQ5 = 1, DQ2 toggles only at sector addresses where failure occurred, and will not toggle at other sector addresses. Use DQ2 in conjunction with DQ6 to determine whether device is in auto erase or erase suspend mode.

Write operation status

	Status	DQ7	DQ6	DQ5	DQ3	DQ2	RY/$\overline{BY}$
Standard mode	Auto programming	$\overline{DQ7}$	Toggle	0	N/A	No toggle	0
	Program/erase in auto erase	0	Toggle	0	1	Toggle†	0
Erase suspend mode	Read erasing sector	1	No toggle	0	N/A	Toggle	1
	Read non-erasing sector	Data	Data	Data	Data	Data	1
	Program in erase suspend	$\overline{DQ7}$	Toggle	0	N/A	Toggle†	0
Exceeded time limits	Auto programming	$\overline{DQ7}$	Toggle	1	N/A	No toggle	1
	Program/erase in auto erase	0	Toggle	1	N/A	Toggle†	1
	Program in erase suspend (non-erase suspended sector)	$\overline{DQ7}$	Toggle	1	N/A	No toggle	1

DQ2 toggles when an erase-suspended sector is read repeatedly.

DQ6 toggles when any address is read repeatedly.

DQ2 = 1 if byte address being programmed is read during erase-suspend program mode.

†DQ2 toggles when the read address applied points to a sector which is undergoing erase, suspended erase, or a failure to erase.

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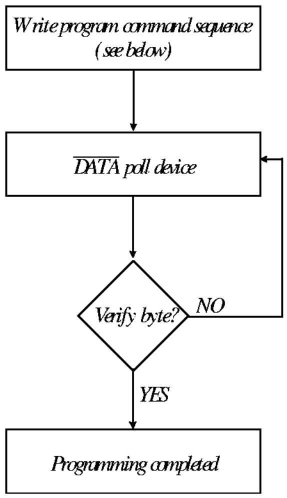
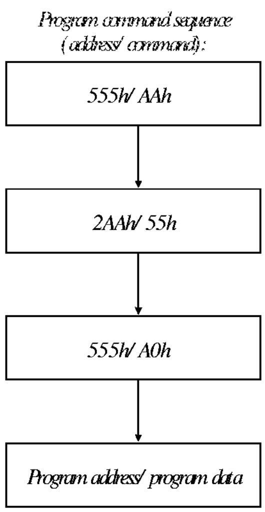
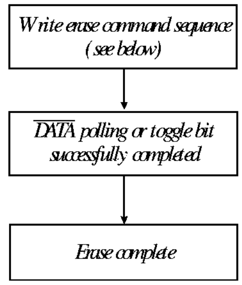
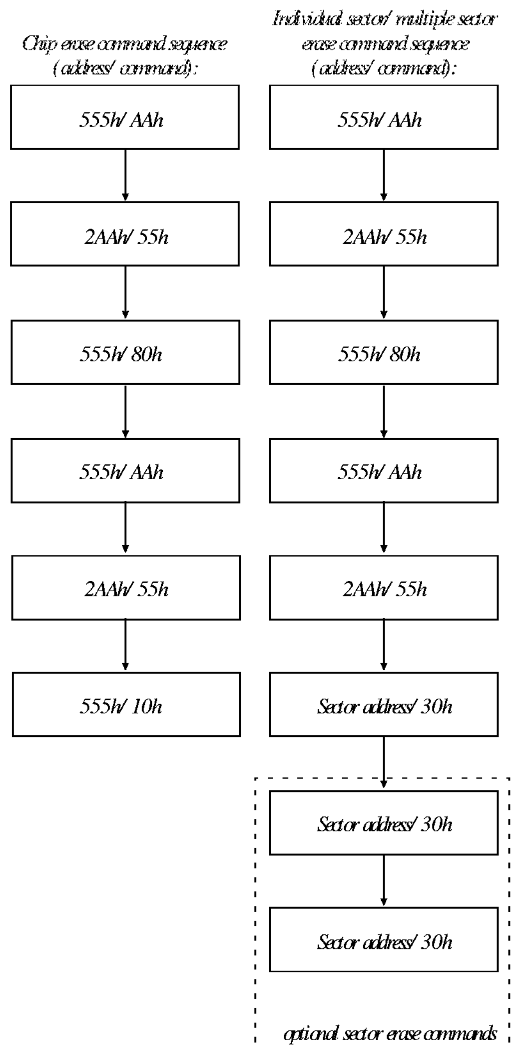
Automated on-chip programming algorithm





Automated on-chip erase algorithm





† The system software should check the status of DQ3 prior to and following each subsequent sector erase command to ensure command completion. The device may not have accepted the command if DQ3 is high on second status check.

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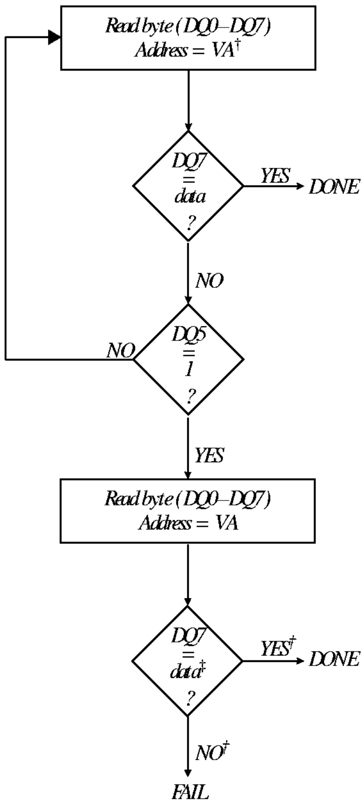
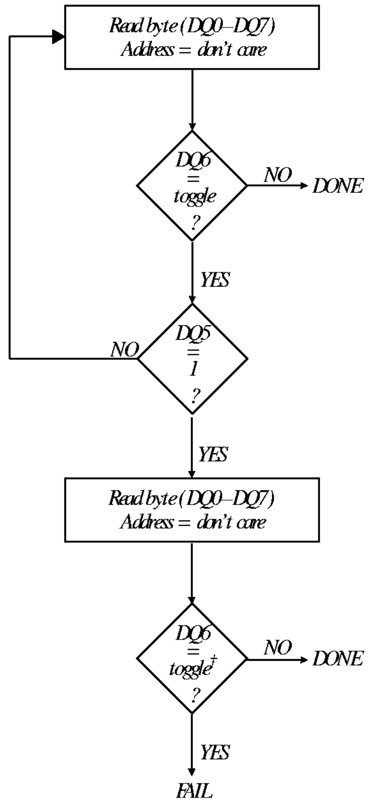
DATA polling algorithm



† VA = Byte address for programming. VA = any of the sector addresses within the sector being erased during Sector Erase. VA = valid address equals any non-protected sector group address during Chip Erase.

‡ DQ7 rechecked even if DQ5 = 1 because DQ5 and DQ7 may not change simultaneously.

Toggle bit algorithm



†DQ6 rechecked even if DQ5 = 1 because DQ6 may stop toggling when DQ5 changes to 1.

DC electrical characteristics

V_{CC} = 2.7–3.6V

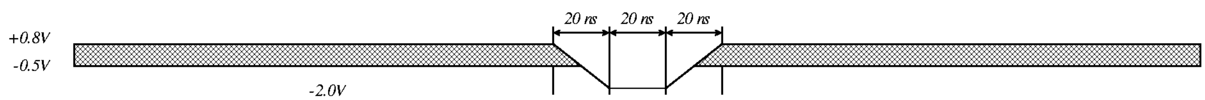
Parameter	Symbol	Test conditions	Min	Max	Unit
Input load current	I_{LI}	$V_{IN} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC\,MAX}$	-	±1	µA
A9 Input load current	I_{LIT}	$V_{CC} = V_{CC\,MAX}$, A9 = 10V		35	µA
Output leakage current	I_{LO}	$V_{OUT} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC\,MAX}$	-	±1	µA
Active current, read @ 6MHz[1]	I_{CC}	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$	-	20	mA
Active current, program/ erase[2]	I_{CC2}	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$	-	35	mA
Standby current	I_{SB3}	$V_{CC} = V_{CCMAX}$, $\overline{CE} = V_{CC} \pm 0.3V$, $\overline{RESET} = V_{CC} \pm 0.3V$	-	5	µA
Deep power down current[3]	I_{SB4}	$\overline{RESET} = V_{SS} \pm 0.3V$	-	5	µA
Input low voltage	V_{IL}		-0.5	0.8	V
Input high voltage	V_{IH}		$0.7 \times V_{CC}$	$V_{CC} + 0.3$	V
Output low voltage	V_{OL}	I_{OL} = 4.0 mA, $V_{CC} = V_{CC\,MIN}$	-	0.45	V
Output high voltage	V_{OH}	I_{OH} = -2.0 mA, $V_{CC} = V_{CC\,MIN}$	$0.85 \times V_{CC}$	-	V
Low V_{CC} lock out voltage	V_{LKO}		1.5	-	V
Input HV select voltage	V_{ID}		9	11	V

1 The I_{CC} current listed includes both the DC operating current and the frequency dependent component (@ 6 MHz). The frequency component typically is less than 2 mA/ MHz with $\overline{OE}$ at V_{IH}.
2 I_{CC} active while program or erase operations are in progress.
3 Automatic sleep mode enables the deep power down mode when addresses are stable for 300 ns. Typical sleep mode current is 1 µA.

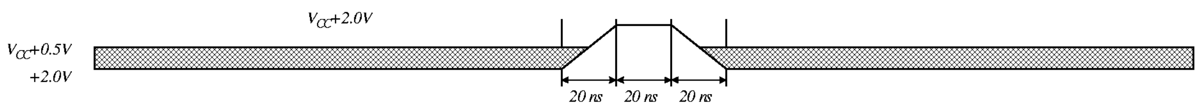
Key to switching waveforms

Rising input Falling input Undefined output/ don't care

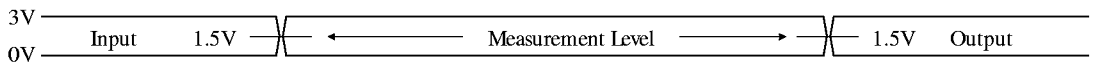
Maximum negative overshoot waveform



Maximum positive overshoot waveform



Input waveform and measurement levels

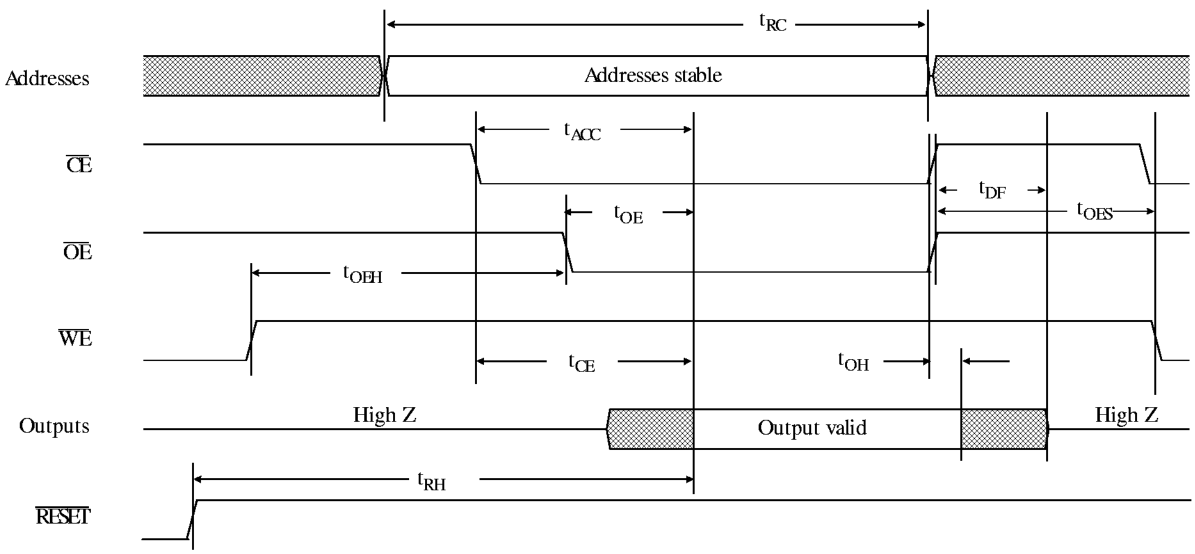


FLASH

AC parameters — read cycle

JEDEC Symbol	Std Symbol	Parameter	-80 Min	-80 Max	-100 Min	-100 Max	-120 Min	-120 Max	-150 Min	-150 Max	Unit
t_{AVAV}	t_{RC}	Read cycle time	80	-	100	-	120	-	150	-	ns
t_{AVQV}	t_{ACC}	Address to output delay	-	80	-	100	-	120	-	150	ns
t_{ELQV}	t_{CE}	Chip enable to output	-	80	-	100	-	120	-	150	ns
t_{GLQV}	t_{OE}	Output enable to output	-	30	-	40	-	50	-	50	ns
	t_{OES}	Output enable setup time	0	-	0	-	0	-	0	-	ns
t_{EHQZ}	t_{DF}	Chip enable to output High Z	-	20	-	30	-	30	-	35	ns
t_{GHQZ}	t_{DF}	Output enable to output High Z	-	20	-	30	-	30	-	35	ns
t_{AXQX}	t_{OH}	Output hold time from addresses, first occurrence of $\overline{CE}$ or $\overline{OE}$	0	-	0	-	0	-	0	-	ns
	t_{OEH}	Output enable hold time: Read	10	-	10	-	10	-	10	-	ns
		Output enable hold time: Toggle and data polling	10	-	10	-	10	-	10	-	ns
t_{PHQV}	t_{RH}	$\overline{RESET}$ high to output delay	-	50	-	50	-	50	-	50	ns
	t_{READY}	$\overline{RESET}$ pin low to read mode	-	10	-	10	-	10	-	10	µs
	t_{RP}	$\overline{RESET}$ pulse	500	-	500	-	500	-	500	-	ns

Read waveform



FLASH

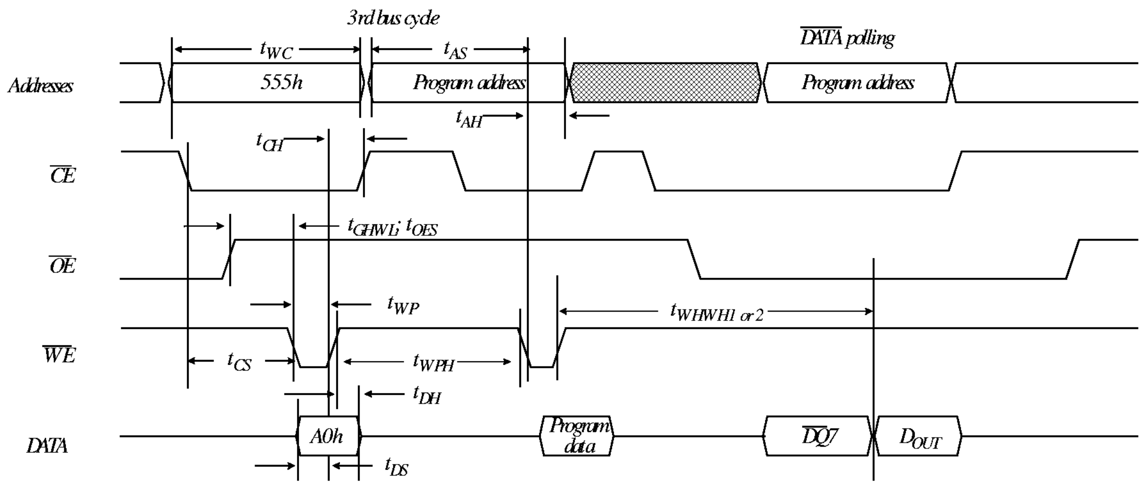
AC parameters — write cycle 1

$\overline{WE}$ controlled

JEDEC Symbol	Std Symbol	Parameter	-80 Min	-80 Max	-100 Min	-100 Max	-120 Min	-120 Max	-150 Min	-150 Max	Unit
t_{AVAV}	t_{WC}	Write cycle time	80	-	100	-	120	-	150	-	ns
t_{AVWL}	t_{AS}	Address setup time	0	-	0	-	0	-	0	-	ns
t_{WLAX}	t_{AH}	Address hold time	45	-	50	-	50	-	50	-	ns
t_{DVWH}	t_{DS}	Data setup time	30	-	50	-	50	-	50	-	ns
t_{WHDX}	t_{DH}	Data hold time	0	-	0	-	0	-	0	-	ns
t_{GHWL}	t_{GHWL}	Read recover time before write	0	-	0	-	0	-	0	-	ns
t_{ELWL}	t_{CS}	$\overline{CE}$ setup time	0	-	0	-	0	-	0	-	ns
t_{WHEH}	t_{CH}	$\overline{CE}$ hold time	0	-	0	-	0	-	0	-	ns
t_{WLWH}	t_{WP}	Write pulse width	40	-	50	-	50	-	50	-	ns
t_{WHWL}	t_{WPH}	Write pulse width high	20	-	20	-	20	-	20	-	ns
t_{WHWH1}	t_{WHWH1}	Programming time	10	-	10	-	10	-	10	-	µs
t_{WHWH2}	t_{WHWH2}	Erase time	0.5	-	0.5	-	0.5	-	0.5	-	sec

Write waveform 1

$\overline{WE}$ controlled



FLASH

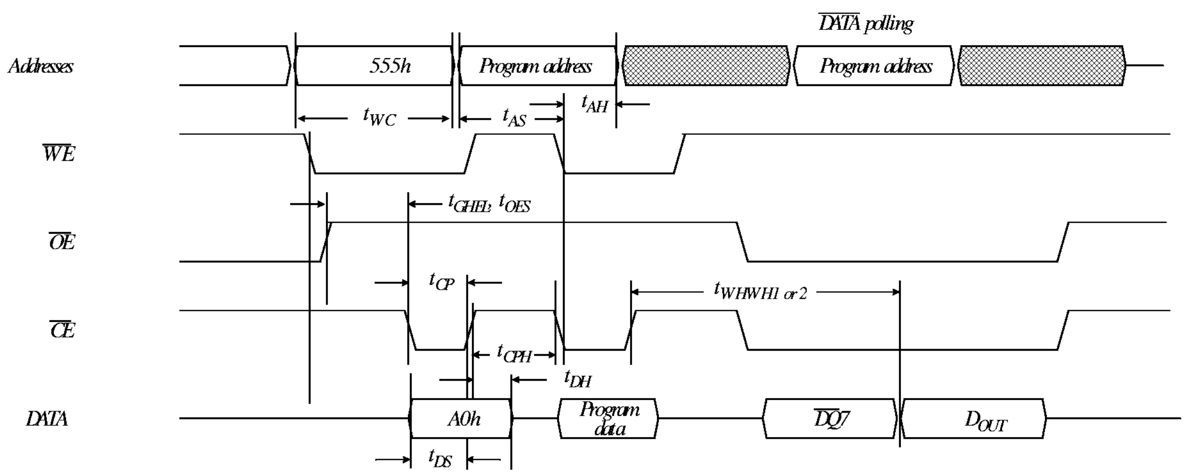
AC parameters — write cycle 2

$\overline{CE}$ controlled

JEDEC Symbol	Std Symbol	Parameter	-80 Min	-80 Max	-100 Min	-100 Max	-120 Min	-120 Max	-150 Min	-150 Max	Unit
t_{AVAV}	t_{WC}	Write cycle time	80	-	100	-	120	-	150	-	ns
t_{AVEL}	t_{AS}	Address setup time	0	-	0	-	0	-	0	-	ns
t_{ELAX}	t_{AH}	Address hold time	45	-	50	-	50	-	50	-	ns
t_{DVEH}	t_{DS}	Data setup time	30	-	50	-	50	-	50	-	ns
t_{EHDX}	t_{DH}	Data hold time	0	-	0	-	0	-	0	-	ns
t_{GHEL}	t_{GHEL}	Read recover time before write	0	-	0	-	0	-	0	-	ns
t_{WLEL}	t_{WS}	$\overline{WE}$ setup time	0	-	0	-	0	-	0	-	ns
t_{EHWH}	t_{WH}	$\overline{WE}$ hold time	0	-	0	-	0	-	0	-	ns
t_{ELEH}	t_{CP}	$\overline{CE}$ pulse width	40	-	50	-	50	-	50	-	ns
t_{EHEL}	t_{CPH}	$\overline{CE}$ pulse width high	20	-	20	-	20	-	20	-	ns
t_{WHWH1}	t_{WHWH1}	Programming time	10	-	10	-	10	-	10	-	µs
t_{WHWH2}	t_{WHWH2}	Erase time	0.5	-	0.5	-	0.5	-	0.5	-	sec

Write waveform 2

$\overline{CE}$ controlled

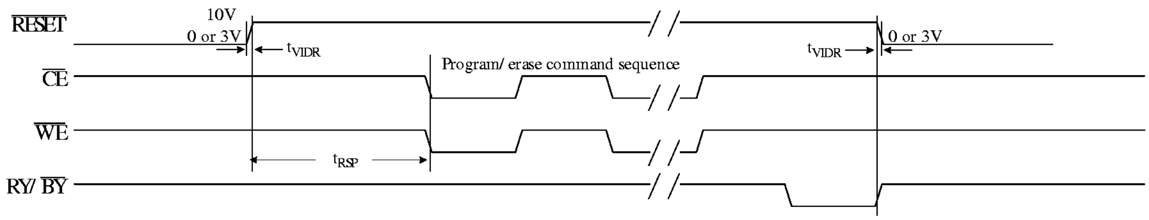


FLASH

AC parameters — temporary sector unprotect

JEDEC Symbol	Std Symbol	Parameter	-80 Min	-80 Max	-100 Min	-100 Max	-120 Min	-120 Max	-150 Min	-150 Max	Unit
	t_{VIDR}	V_{ID} rise and fall time	500	-	500	-	500	-	500	-	ns
	t_{RSP}	$\overline{RESET}$ setup time for temporary sector unprotect	4	-	4	-	4	-	4	-	µs

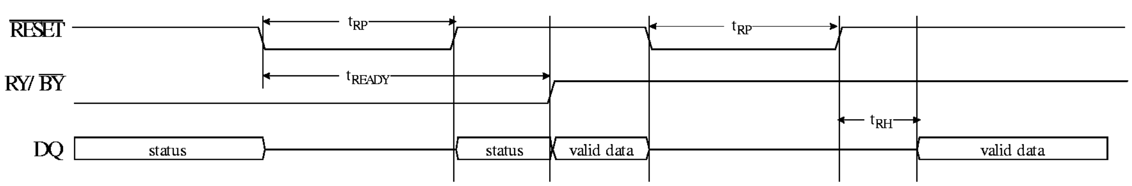
Temporary sector unprotect waveform



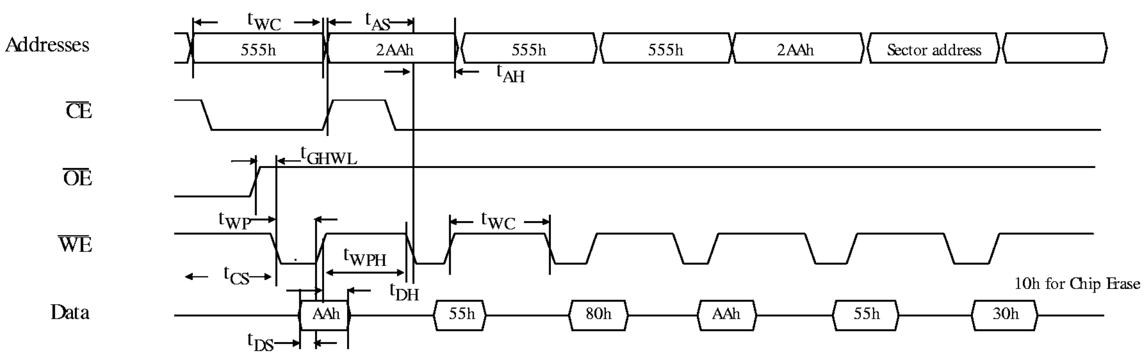
AC parameters — $\overline{RESET}$

JEDEC Symbol	Std Symbol	Parameter	-80 Min	-80 Max	-100 Min	-100 Max	-120 Min	-120 Max	-150 Min	-150 Max	Unit
	t_{RP}	$\overline{RESET}$ pulse	500	-	500	-	500	-	500	-	ns
	t_{RH}	$\overline{RESET}$ High time before Read	-	50	-	50	-	50	-	50	ns
	t_{READY}	$\overline{RESET}$ Low to Read mode	-	10	-	10	-	10	-	10	µs

$\overline{RESET}$ waveform

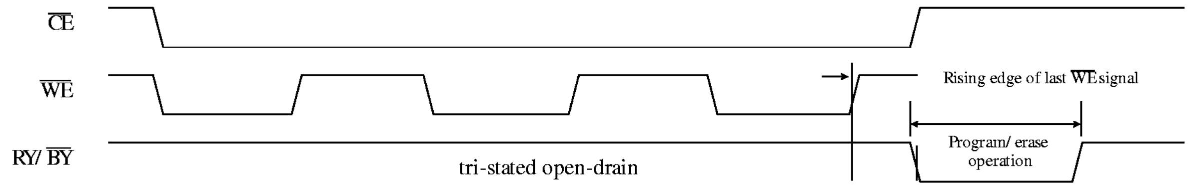


Erase waveform

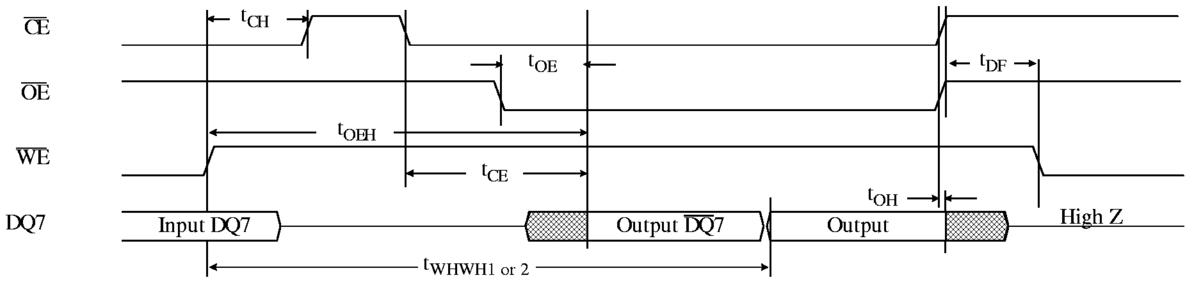


FLASH

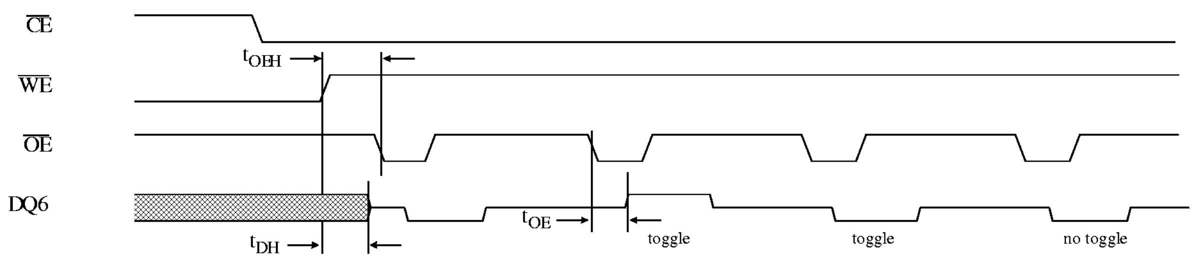
RY/$\overline{BY}$ waveform



$\overline{DATA}$ polling waveform



Toggle bit waveform



Erase and programming performance

Parameter		Limits Min	Typical	Max	Unit
Sector erase and verify-1 time (excludes 00h programming prior to erase)		-	1.0	-	sec
Programming time	Byte	-	10	-	µs
Chip programming time		-	7.2	-	sec
Erase/ program cycles		-	-	10,000	cycles

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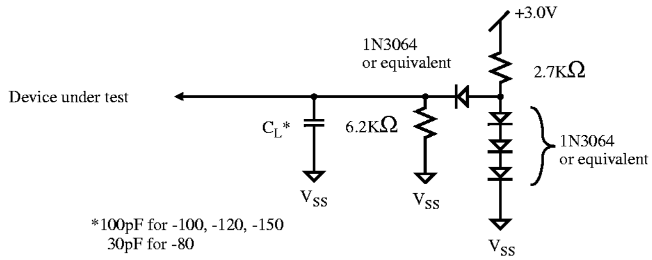
Latchup tolerance

Parameter	Min	Max	Unit
Input voltage with respect to V_{SS} on A9, $\overline{OE}$, and $\overline{RESET}$ pin	-1.0	+12.0	V
Input voltage with respect to V_{SS} on all DQ, address and control pins	-0.5	V_{CC}+0.5	V
Current	-100	+100	mA

Includes all pins except V_{CC}. Test conditions: V_{CC} = 3.0V, one pin at a time.

AC test conditions



*100pF for -100, -120, -150
30pF for -80

Recommended operating conditions

Parameter	Symbol	Min	Max	Unit
Supply voltage	V_{CC}	+2.7	+3.6	V
	V_{SS}	0	0	V
Input voltage	V_{IH}	1.9	V_{CC}+ 0.3	V
	V_{IL}	–0.5	0.8	V

Absolute maximum ratings

Parameter	Symbol	Min	Max	Unit
Input voltage (Input or DQ pin)	V_{IN}	–0.5	V_{CC}+ 0.5	V
Input voltage (A9 pin, $\overline{OE}$, $\overline{RESET}$)	V_{IN}	–0.5	+12.5	V
Power supply voltage	V_{CC}	-0.5	+4.0	V
Operating temperature	T_{OPR}	–55	+125	°C
Storage temperature (plastic)	T_{STG}	–65	+150	°C
Short circuit output current	I_{OUT}	-	150	mA

Stresses greater than those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

FLASH

TSOP pin capacitance

Symbol	Parameter	Test setup	Typ	Max	Unit
C_{IN}	Input capacitance	$V_{IN} = 0$	6	7.5	pF
C_{OUT}	Output capacitance	$V_{OUT} = 0$	8.5	12	pF
C_{IN2}	Control pin capacitance	$V_{IN} = 0$	8	10	pF

SO pin capacitance

Symbol	Parameter	Test setup	Typ	Max	Unit
C_{IN}	Input capacitance	$V_{IN} = 0$	6	7.5	pF
C_{OUT}	Output capacitance	$V_{OUT} = 0$	8.5	12	pF
C_{IN2}	Control pin capacitance	$V_{IN} = 0$	8	10	pF

Data retention

Parameter	Temp.(°C)	Min	Unit
Minimum pattern data retention time	150°	10	years
	125°	20	years

AS29LV008 ordering codes

Package \ Access Time	80 ns (commercial/ industrial)	100 ns (commercial/ industrial)	120 ns (commercial/ industrial)	150 ns (commercial/ industrial)
TSOP, 10×20 mm, 40-pin	AS29LV008-80TC AS29LV008-80TI	AS29LV008-100TC AS29LV008-100TI	AS29LV008-120TC AS29LV008-120TI	AS29LV008-150TC AS29LV008-150TI
SO, 600 mil wide, 44-pin	AS29LV008-80SC AS29LV008-80SI	AS29LV008-100SC AS29LV008-100SI	AS29LV008-120SC AS29LV008-120SI	AS29LV008-150SC AS29LV008-150SI

AS29LV008 part numbering system

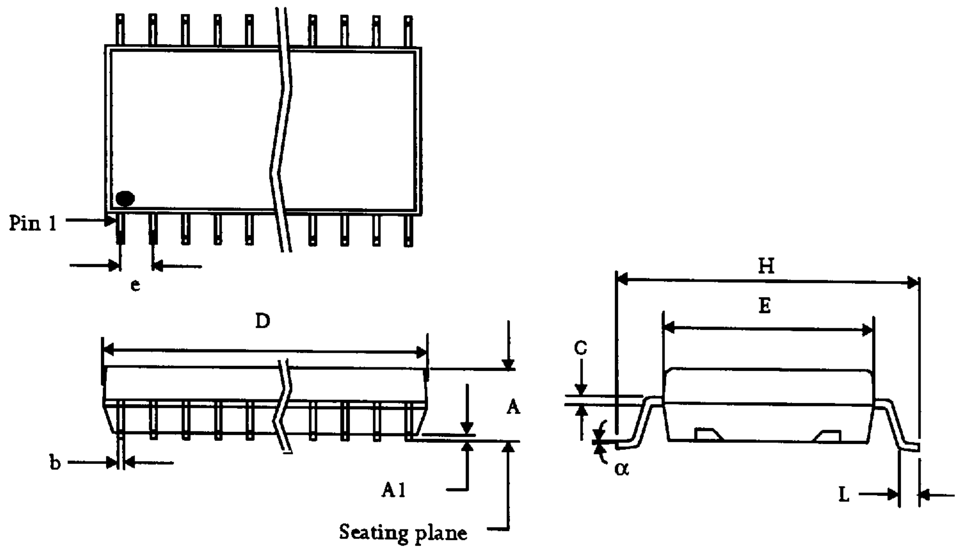
AS29	X	008	–XXX	X	X
Flash EEPROM prefix	F = 5V LV = 3V LL = 2.5V	Device number	Address access time	Package: S= SO T= TSOP	Temperature range: C = Commercial: 0°C to 70°C I = Industrial: -40°C to 85°C

FLASH

Plastic small outline gull wing IC (SOIC)

	28-pin 330 mil	
	Min	Max
A	-	0.112
A1	0.004	-
b	0.014	0.020
C	0.008	0.014
D	-	0.733
e	0.050 nominal	
E	0.326	0.336
H	0.453	0.477
L	0.028	0.044
α	0°	10°

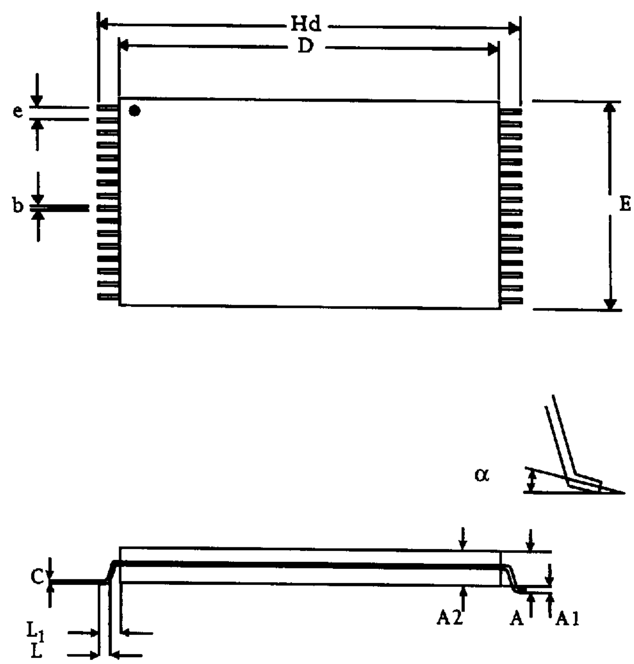
Dimensions in inches

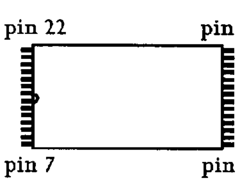


Thin small outline package (TSOP-I)

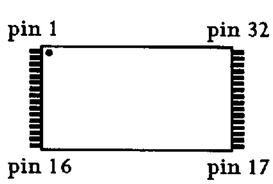
	28-pin 8×13.4		32-pin 8×20		40-pin 10×20	
	Min	Max	Min	Max	Min	Max
A	-	1.20	-	1.20	-	1.20
A1	0.05	0.15	0.05	0.15	0.05	0.15
A2	0.90	1.05	0.90	1.05	0.95	1.05
b	0.17	0.27	0.17	0.23	0.17	0.27
C	0.10	-	0.10	-	0.10	0.20
D	11.70	11.90	18.20	18.60	18.30	18.50
e	0.55 nominal		0.50 nominal		0.50 nominal	
E	8.0 nominal		7.80	8.20	9.90	10.10
Hd	13.20	13.60	19.80	20.20	19.80	20.20
L	0.30	0.70	0.40	0.60	0.50	0.70
α	0°	5°	1°	5°	0°	5°

Dimensions in millimeters





28-pin



32-pin