FAIRCHILD SEMICONDUCTOR™

March 1998

74F646 • 74F646B • 74F648
Octal Transceiver/Register with 3-STATE Outputs

General Description

These devices consist of bus transceiver circuits with 3-STATE, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes to a high logic level. Control $\overline{G}$ and direction pins are provided to control the transceiver function. In the transceiver mode, data present at the high impedance port may be stored in either the A or the B register or in both. The select controls can multiplex stored and real-time (transparent mode) data. The direction control determines which bus will receive data when the enable control $\overline{G}$ is Active LOW. In the isolation mode (control $\overline{G}$ HIGH), A data may be stored in the B register and/or B data may be stored in the A register.

Features

- Independent registers for A and B buses
- Multiplexed real-time and stored data
- 'F648 has inverting data paths
- 'F646/'F646B have non-inverting data paths
- 'F646B is a faster version of the 'F646
- 3-STATE outputs
- 300 mil slim DIP
- Guaranteed 4000V minimum ESD protection

Ordering Code:

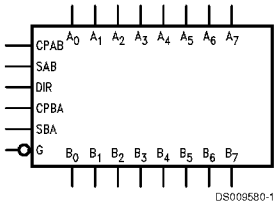
Commercial	Military	Package Number	Package Description
74F646SPC		N24C	24-Lead (0.300" Wide) Molded Dual-In-Line
	54F646DM (Note 2)	J24F	24-Lead (0.300"Wide) Ceramic Dual-In-Line
74F646SC (Note 1)		M24B	24-Lead (0.300" Wide) Molded Small Outline, JEDEC
74F646MSA (Note 1)		MSA24	24-Lead Molded Shrink Small Outline, EIAJ, Type II
	54F646FM (Note 2)	W24C	24-Lead Cerpack
	54F646LM (Note 2)	E28A	28-Lead Ceramic Leadless Chip Carrier, Type C
74F646BSPC		N24C	24-Lead (0.300" Wide) Molded Dual-In-Line
74F646BSC (Note 1)		M24B	24-Lead (0.300" Wide) Molded Small Outline, JEDEC
74F648SPC		N24C	24-Lead (0.300" Wide) Molded Dual-In-Line
	54F648SDM (Note 2)	J24F	24-Lead (0.300" Wide) Ceramic Dual-In-Line
74F648SC (Note 1)		M24B	24-Lead (0.300" Wide) Molded Small Outline, JEDEC
	54F648FM (Note 2)	W24C	24-Lead Cerpack
	54F648LM (Note 2)	E28A	24-Lead Ceramic Leadless Chip Carrier, Type C

Note 1: Devices also available in 13" reel. Use suffix = SCX.

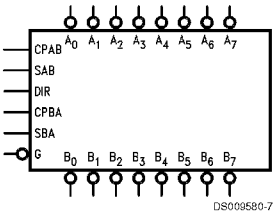
Note 2: Military grade device with environmental and burn-in processing. Use suffix = DMQB, FMQB and LMQB.

Logic Symbols

'F646/'F646B

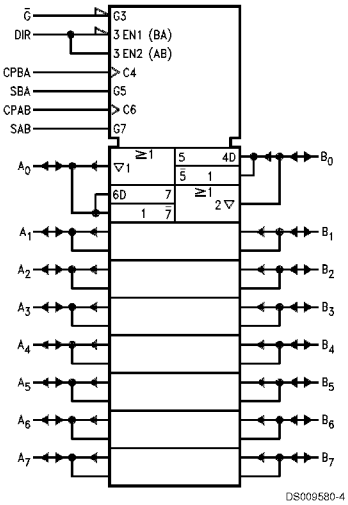


'F648

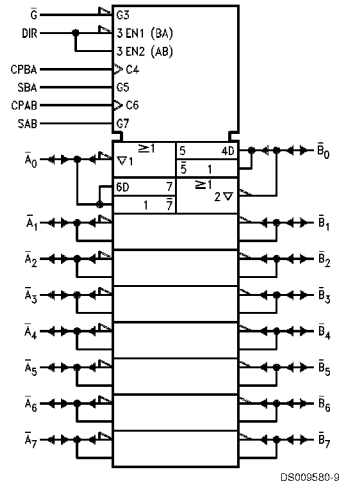


Logic Symbols (Continued)

IEEE/IEC
'F646/'F646B

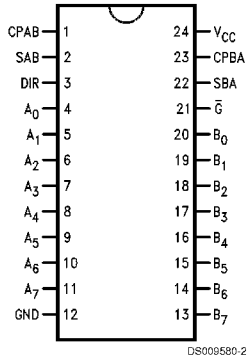


IEEE/IEC
'F648

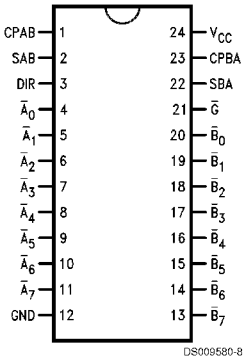


Connection Diagrams

Pin Assignment
for DIP, SOIC and Flatpak
'F646/'F646B

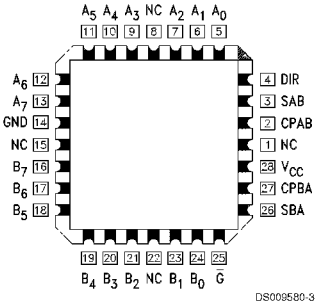


Pin Assignment
for DIP, SOIC and Flatpak
'F648



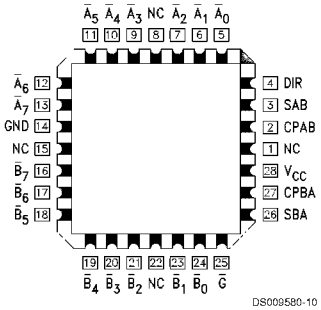
Connection Diagrams (Continued)

Pin Assignment for LCC 'F646/'F646B



DS009580-3

Pin Assignment for LCC 'F648



DS009580-10

Unit Loading/Fan Out

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
A_0–A_7	Data Register A Inputs/ 3-STATE Outputs	3.5/1.083 600/106.6 (80)	70 µA/–650 µA –12 mA/64 mA (48 mA)
B_0–B_7	Data Register B Inputs/ 3-STATE Outputs	3.5/1.083 600/106.6 (80)	70 µA/–650 µA –12 mA/64 mA (48 mA)
CPAB, CPBA	Clock Pulse Inputs	1.0/1.0	20 µA/–0.6 mA
SAB, SBA	Select Inputs	1.0/1.0	20 µA/–0.6 mA
$\overline{G}$	Output Enable Input	1.0/1.0	20 µA/–0.6 mA
DIR	Direction Control Input	1.0/1.0	20 µA/–0.6 mA

Function Table

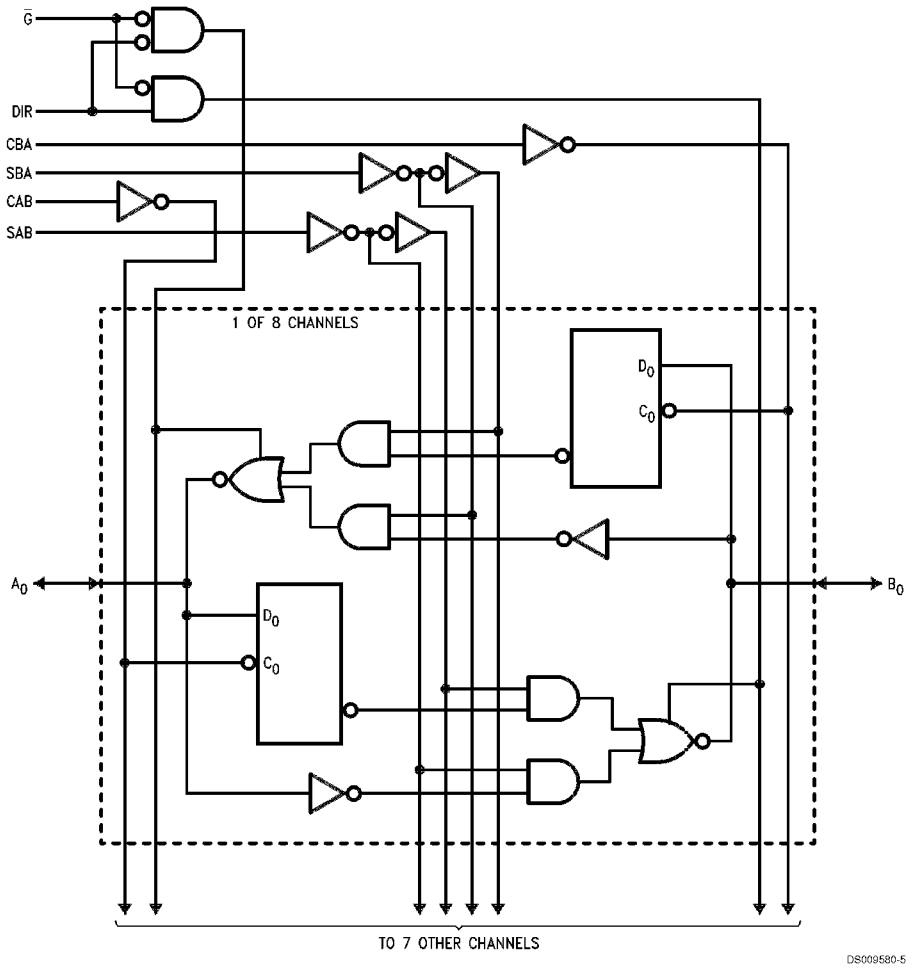
Inputs						Data I/O (Note 3)		Function
$\overline{G}$	DIR	CPAB	CPBA	SAB	SBA	A_0–A_7	B_0–B_7	
H	X	H or L	H or L	X	X			Isolation
H	X	↗	X	X	X	Input	Input	Clock A_n Data into A Register
H	X	X	↗	X	X			Clock B_n Data into B Register
L	H	X	X	L	X			A_n to B_n—Real Time (Transparent Mode)
L	H	↗	X	L	X	Input	Output	Clock A_n Data into A Register
L	H	H or L	X	H	X			A Register to B_n (Stored Mode)
L	H	↗	X	H	X			Clock A_n Data into A Register and Output to B_n
L	L	X	X	X	L			B_n to A_n—Real Time (Transparent Mode)
L	L	X	↗	X	L	Output	Input	Clock B_n Data into B Register
L	L	X	H or L	X	H			B Register to A_n (Stored Mode)
L	L	X	↗	X	H			Clock B_n Data into B Register and Output to A_n

H = HIGH Voltage Level
L = LOW Voltage Level
X = Irrelevant
↗ = LOW-to-HIGH Transition

Note 3: The data output functions may be enabled or disabled by various signals at the $\overline{G}$ and DIR Inputs. Data input functions are always enabled; i.e., data at the bus pins will be stored on every LOW-to-HIGH transition of the clock inputs.

Logic Diagrams

'F646/'F646B

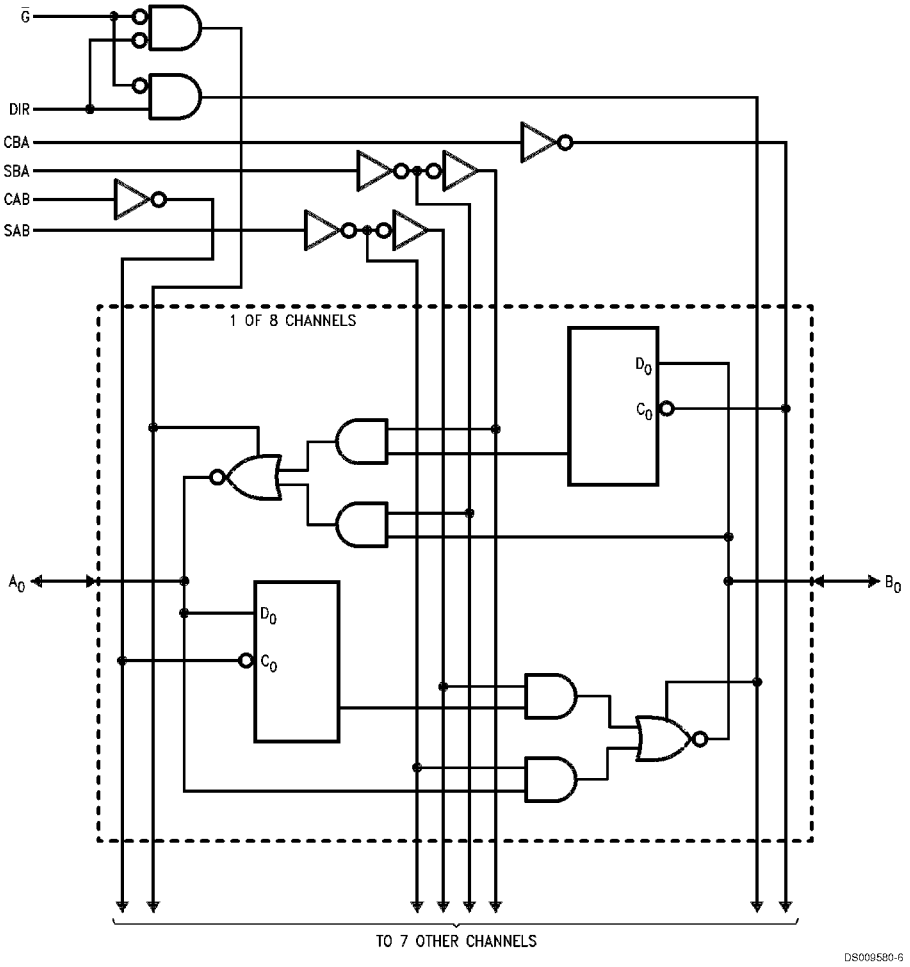


DS009580-5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Logic Diagrams (Continued)

'F648



DS009580-6

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 4)

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +175°C
Plastic	−55°C to +150°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 5)	−0.5V to +7.0V
Input Current (Note 5)	−30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V_{CC} = 0V)	
Standard Output	−0.5V to V_{CC}
3-STATE Output	−0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I_{OL} (mA)
ESD Last Passing Voltage (Min)	4000V

Recommended Operating Conditions

Free Air Ambient Temperature	
Military	−55°C to +125°C
Commercial	0°C to +70°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

Note 4: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 5: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics

Symbol	Parameter		54F/74F Min	54F/74F Typ	54F/74F Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal
V_{IL}	Input LOW Voltage				0.8	V		Recognized as a LOW Signal
V_{CD}	Input Clamp Diode Voltage				−1.2	V	Min	I_{IN} = −18 mA (Non I/O Pins)
V_{OH}	Output HIGH Voltage	54F 10% V_{CC}	2.0			V	Min	I_{OH} = −12 mA (A_n, B_n)
		74F 10% V_{CC}	2.0					I_{OH} = −15 mA (A_n, B_n)
V_{OL}	Output LOW Voltage	54F 10% V_{CC}			0.55	V	Min	I_{OL} = 48 mA (A_n, B_n)
		74F 10% V_{CC}			0.55			I_{OL} = 64 mA (A_n, B_n)
I_{IH}	Input HIGH Current	54F			20.0	µA	Max	V_{IN} = 2.7V (Non I/O Pins)
		74F			5.0			
I_{BVI}	Input HIGH Current Breakdown Test	54F			100	µA	Max	V_{IN} = 7.0V (Non I/O Pins)
		74F			7.0			
I_{BVIT}	Input HIGH Current Breakdown (I/O)	54F			1.0	mA	Max	V_{IN} = 5.5V (A_n, B_n)
		74F			0.5			
I_{CEX}	Output HIGH Leakage Current	54F			250	µA	Max	V_{OUT} = V_{CC}
		74F			50			
V_{ID}	Input Leakage Test	74F	4.75			V	0.0	I_{ID} = 1.9 µA All Other Pins Grounded
I_{OD}	Output Leakage Circuit Current	74F			3.75	µA	0.0	V_{IOD} = 150 mV All Other Pins Grounded
I_{IL}	Input LOW Current				−0.6	mA	Max	V_{IN} = 0.5V (Non I/O Pins)
I_{IH} + I_{OZH}	Output Leakage Current				70	µA	Max	V_{OUT} = 2.7V (A_n, B_n)
I_{IL} + I_{OZL}	Output Leakage Current				−650	µA	Max	V_{OUT} = 0.5V (A_n, B_n)
I_{OS}	Output Short-Circuit Current		−100		−225	mA	Max	V_{OUT} = 0V
I_{ZZ}	Bus Drainage Test				500	µA	0.0V	V_{OUT} = 5.25V
I_{CCH}	Power Supply Current				135	mA	Max	V_O = HIGH
I_{CCL}	Power Supply Current				150	mA	Max	V_O = LOW
I_{CCZ}	Power Supply Current				150	mA	Max	V_O = HIGH Z

'F646/'F648
AC Electrical Characteristics

Symbol	Parameter	74F $T_A = +25^\circ C$ $V_{CC} = +5.0V$ $C_L = 50$ pF		54F T_A, V_{CC} = Mil $C_L = 50$ pF		74F T_A, V_{CC} = Com $C_L = 50$ pF		Units
		Min	Max	Min	Max	Min	Max	
f_{max}	Maximum Clock Frequency	90		75		90		MHz
t_{PLH}	Propagation Delay	2.0	7.0	2.0	8.5	2.0	8.0	ns
t_{PHL}	Clock to Bus	2.0	8.0	2.0	9.5	2.0	9.0	
t_{PLH}	Propagation Delay	1.0	7.0	1.0	8.0	1.0	7.5	ns
t_{PHL}	Bus to Bus ('F646)	1.0	6.5	1.0	8.0	1.0	7.0	
t_{PLH}	Propagation Delay	2.0	8.5	1.0	10.0	2.0	9.0	ns
t_{PHL}	Bus to Bus ('F648)	1.0	7.5	1.0	9.0	1.0	8.0	
t_{PLH}	Propagation Delay	2.0	8.5	2.0	11.0	2.0	9.5	ns
t_{PHL}	SBA or SAB to A or B	2.0	8.0	2.0	10.0	2.0	9.0	
t_{PZH}	Enable Time	2.0	8.5	2.0	10.0	2.0	9.0	ns
t_{PZL}	$\overline{OE}$ to A or B	2.0	12.0	2.0	13.5	2.0	12.5	
t_{PHZ}	Disable Time	1.0	7.5	1.0	9.0	1.0	8.5	ns
t_{PLZ}	$\overline{OE}$ to A or B	2.0	9.0	2.0	11.0	2.0	9.5	
t_{PZH}	Enable Time	2.0	14.0	2.0	16.0	2.0	15.0	ns
t_{PZL}	DIR to A or B	2.0	13.0	2.0	15.0	2.0	14.0	
t_{PHZ}	Disable Time	1.0	9.0	1.0	10.0	1.0	9.5	ns
t_{PLZ}	DIR to A or B	2.0	11.0	2.0	12.0	2.0	11.5	

'F646/'F648
AC Operating Requirements

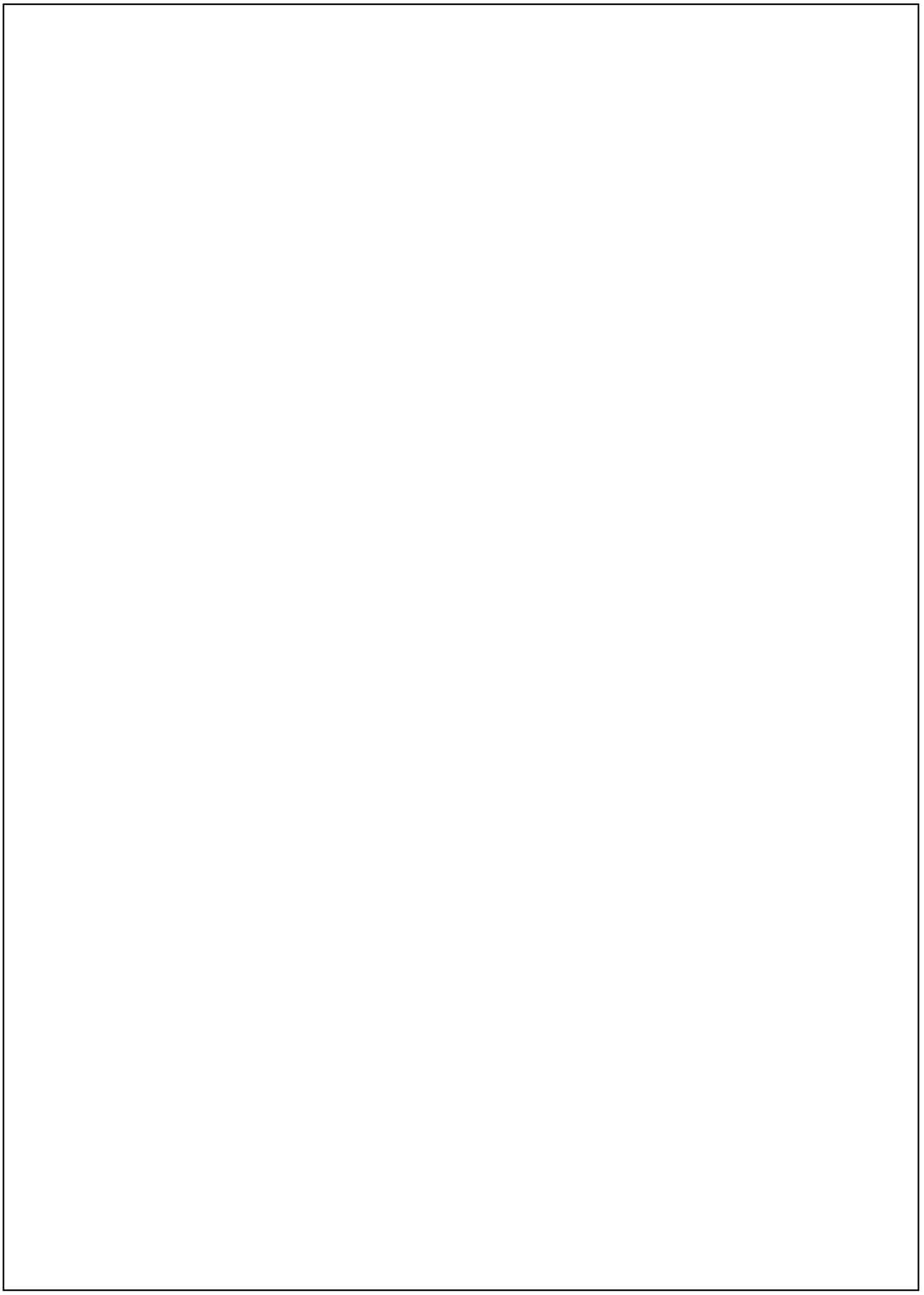
Symbol	Parameter	74F $T_A = +25^\circ C$ $V_{CC} = +5.0V$		54F T_A, V_{CC} = Mil		74F T_A, V_{CC} = Com		Units
		Min	Max	Min	Max	Min	Max	
$t_s(H)$	Setup Time, HIGH or LOW	5.0		5.0		5.0		ns
$t_s(L)$	Bus to Clock	5.0		5.0		5.0		
$t_h(H)$	Hold Time, HIGH or LOW	2.0		2.5		2.0		ns
$t_h(L)$	Bus to Clock	2.0		2.5		2.0		
$t_w(H)$	Clock Pulse Width	5.0		5.0		5.0		ns
$t_w(L)$	HIGH or LOW	5.0		5.0		5.0		

'F646B
AC Electrical Characteristics

Symbol	Parameter	74F T_A = +25°C V_{CC} = +5.0V C_L = 50 pF		54F T_A, V_{CC} = Mil C_L = 50 pF		74F T_A, V_{CC} = Com C_L = 50 pF		Units
		Min	Max	Min	Max	Min	Max	
f_{max}	Maximum Clock Frequency	165				150		MHz
t_{PLH}	Propagation Delay	2.5	7.0			2.5	8.0	ns
t_{PHL}	Clock to Bus	3.0	7.5			3.0	8.0	
t_{PLH}	Propagation Delay	2.0	6.0			2.0	7.0	ns
t_{PHL}	Bus to Bus	2.0	6.0			2.0	7.0	
t_{PLH}	Propagation Delay	2.5	7.5			2.5	8.5	ns
t_{PHL}	SBA or SAB to A or B	2.5	7.5			2.5	8.5	
t_{PZH}	Enable Time	2.5	6.5			2.5	8.0	ns
t_{PZL}	$\overline{OE}$ to A or B	2.5	9.0			2.5	10.0	
t_{PHZ}	Disable Time	1.5	6.5			1.5	7.5	ns
t_{PLZ}	$\overline{OE}$ to A or B	2.0	7.0			2.0	8.5	
t_{PZH}	Enable Time	2.0	7.0			2.0	8.5	ns
t_{PZL}	DIR to A or B	3.0	9.5			3.0	10.0	
t_{PHZ}	Disable Time	1.5	7.5			1.5	8.5	ns
t_{PLZ}	DIR to A or B	2.5	8.5			2.5	9.5	

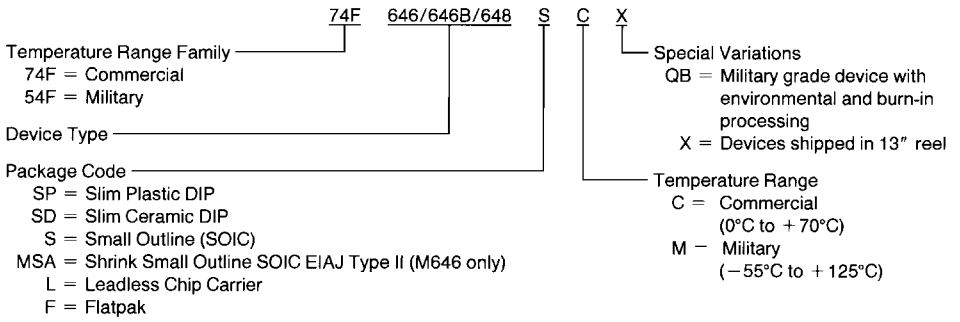
'F646B
AC Operating Requirements

Symbol	Parameter	74F T_A = +25°C V_{CC} = +5.0V		54F T_A, V_{CC} = Mil		74F T_A, V_{CC} = Com		Units
		Min	Max	Min	Max	Min	Max	
t_s(H)	Setup Time, HIGH or LOW	5.0				4.0		ns
t_s(L)	Bus to Clock	5.0				4.0		
t_h(H)	Hold Time, HIGH or LOW	1.5				1.5		ns
t_h(L)	Bus to Clock	1.5				1.5		
t_w(H)	Clock Pulse Width	5.0				5.0		ns
t_w(L)	HIGH or LOW	5.0				5.0		



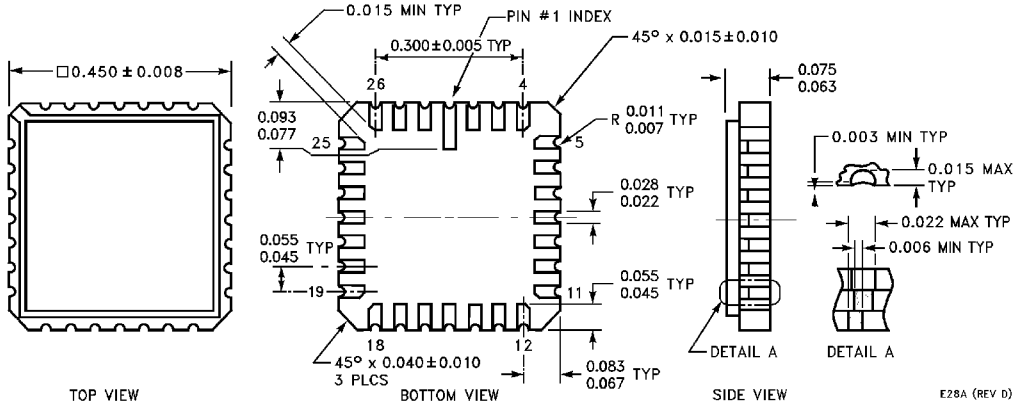
Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:



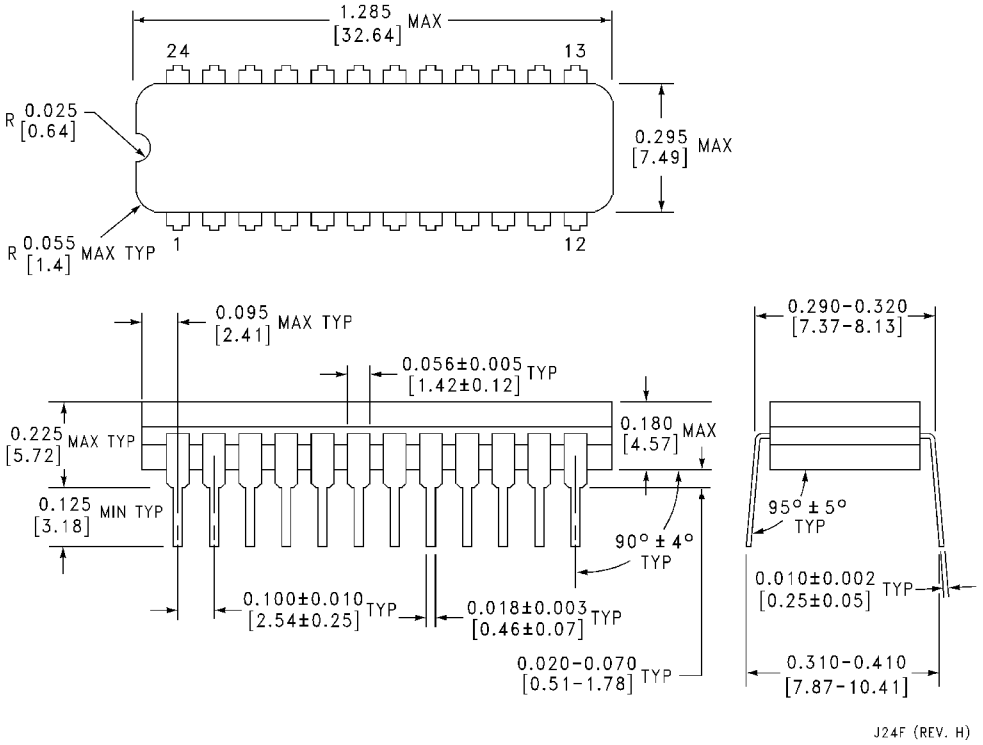
DS009580-12

Physical Dimensions inches (millimeters) unless otherwise noted



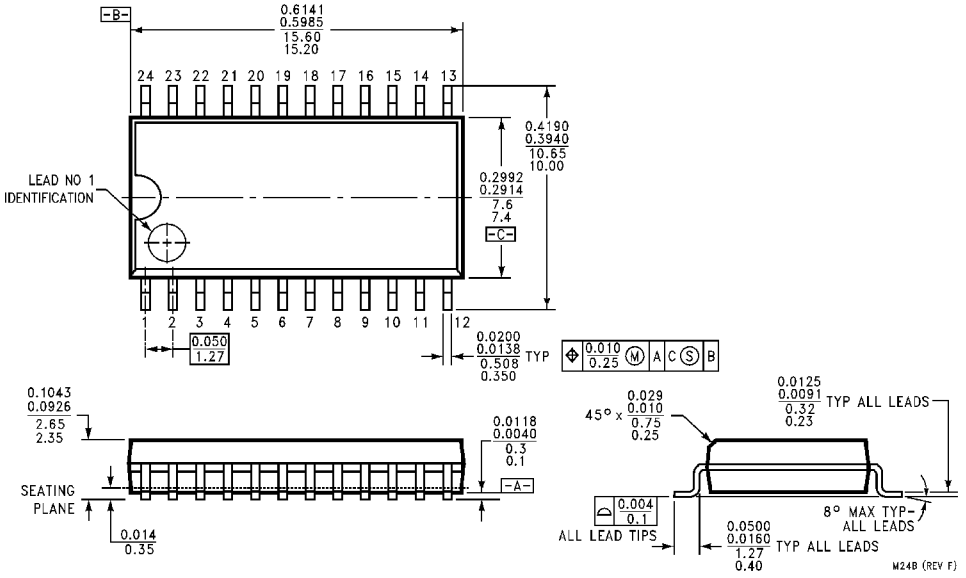
28-Lead Ceramic Leadless Chip Carrier, Type C
Package Number E28A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

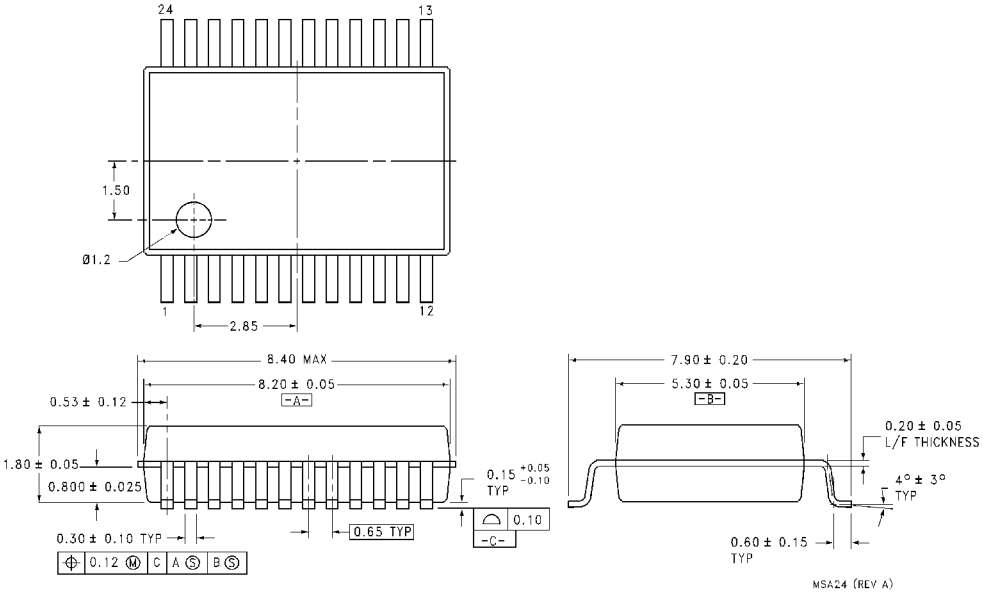


24-Lead (0.300" Wide) Ceramic Dual-In-Line Package (SD)
Package Number J24F

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

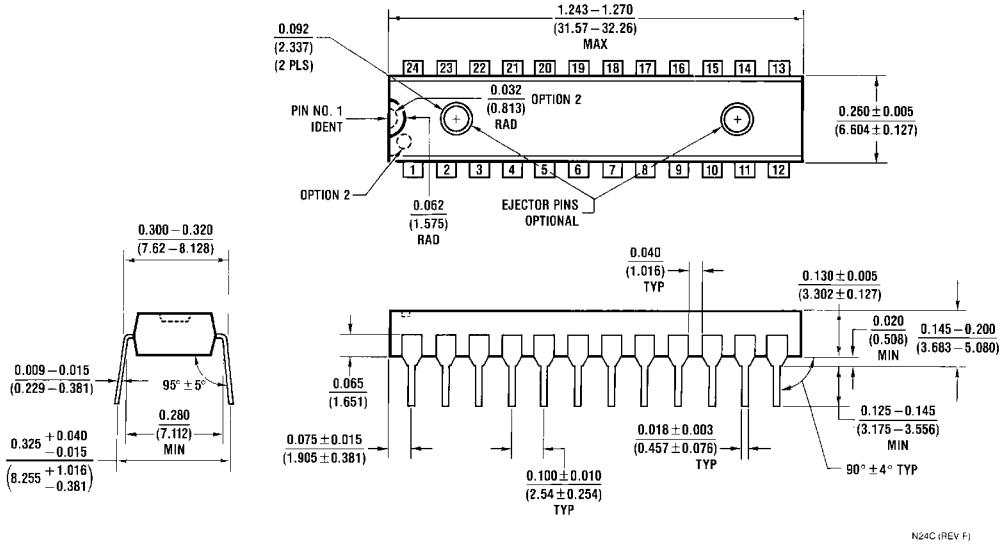


24-Lead (0.300" Wide) Molded Small Outline Package, JEDEC (S)
Package Number M24B

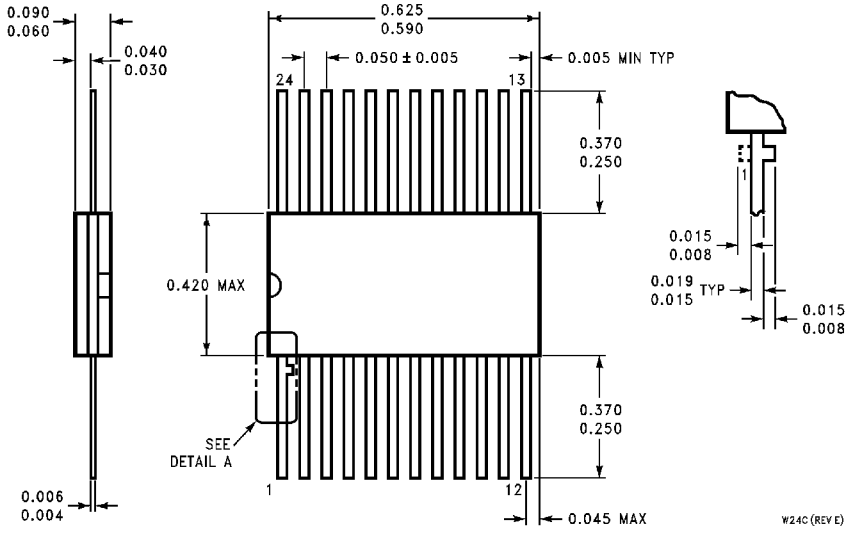


24-Lead Molded Shrink Small Outline Package, EIAJ, Type II
Package Number MSA24

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



24-Lead (0.300" Wide) Molded Dual-In-Line Package (SP)
Package Number N24C



24-Lead Cerpack
Package Number W24C

LIFE SUPPORT POLICY

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1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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