

TC74HC373AP/AF/AFW

TC74HC533AP/AF

OCTAL D-TYPE LATCH WITH 3-STATE OUTPUT
 TC74HC373AP/AF NON-INVERTING
 TC74HC533AP/AF INVERTING

The TC74HC373A and TC74HC533A are high speed CMOS OCTAL LATCH with 3-STATE OUTPUT fabricated with silicon gate C²MOS technology.

They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

These 8-bit D-type latches are controlled by a latch enable input (LE) and a output enable input (\overline{OE}).

When the \overline{OE} input is high, the eight outputs are in a high impedance state.

The TC74HC373A has non-inverting outputs, and TC74HC533A has inverting outputs.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

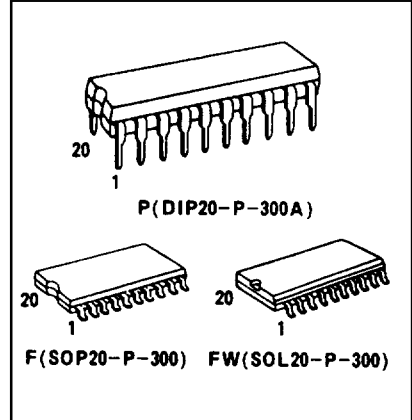
FEATURES:

- High Speed $t_{pd}=11ns$ (typ.) at $V_{CC}=5V$
- Low Power Dissipation $I_{CC}=4\mu A$ (Max.) at $T_a=25^\circ C$
- High Noise Immunity $V_{NIH}=V_{NIL}=28\% V_{CC}$ (Min.)
- Output Drive Capability 15 LSTTL Loads
- Symmetrical Output Impedance ... $|I_{OH}|=I_{OL}=6mA$ (Min.)
- Balanced Propagation Delays $t_{pLH}\approx t_{pHL}$
- Wide Operating Voltage Range ... $V_{CC}(opr)=2V\sim 6V$
- Pin and Function Compatible with 74LS373/533

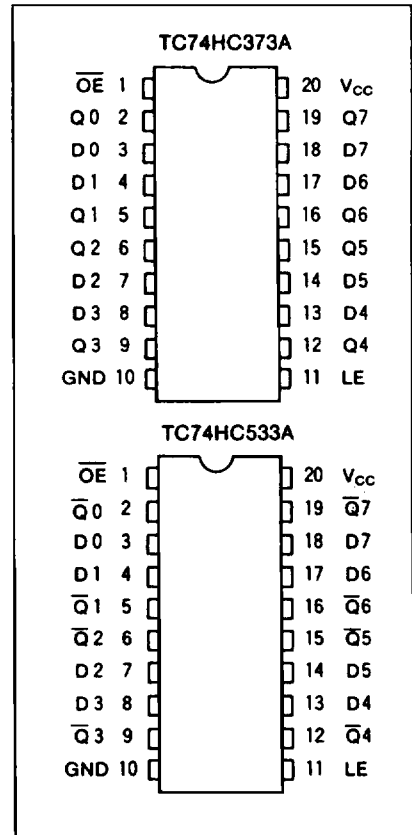
TRUTH TABLE

INPUTS			OUTPUTS	
\overline{OE}	LE	D	Q(HC373A)	\overline{Q} (HC533A)
H	X	X	Z	Z
L	L	X	Q_n	\overline{Q}_n
L	H	L	L	H
L	H	H	H	L

X : Don't Care
 Z : High Impedance
 Q_n (\overline{Q}_n) : Q (\overline{Q}) outputs are latched at the time when the LE input is taken to a low logic level.



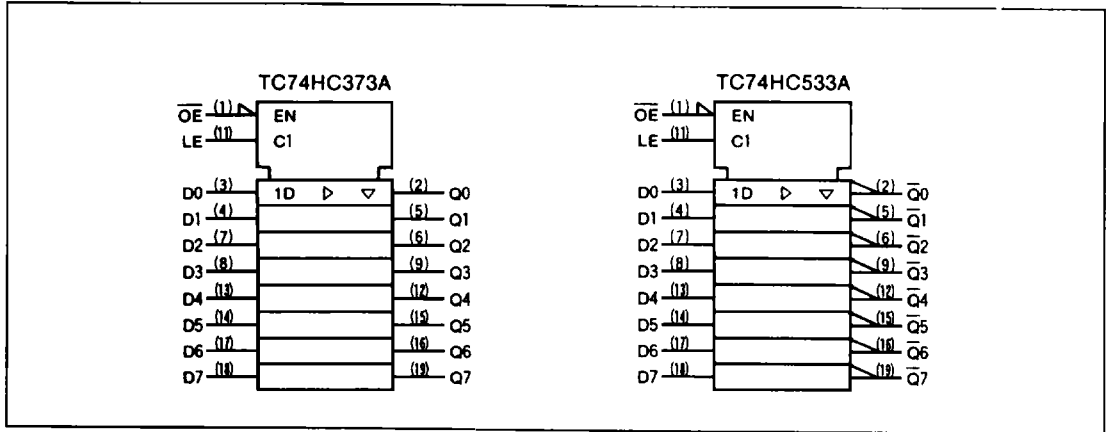
PIN ASSIGNMENT



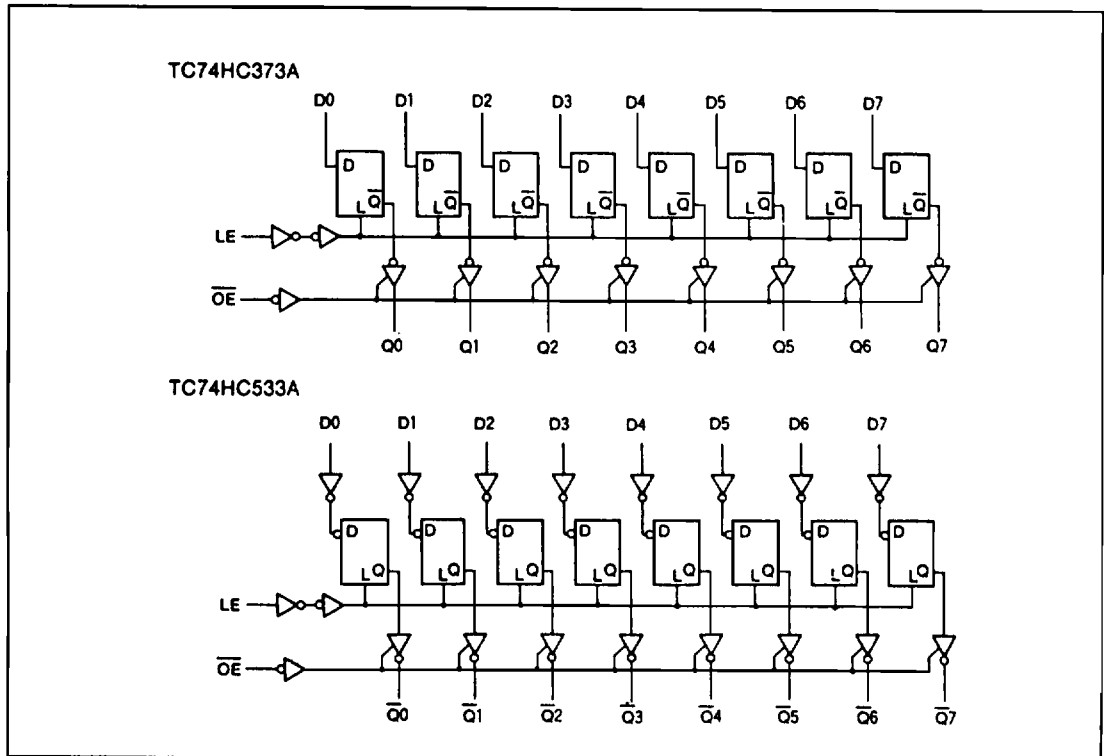
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IEC LOGIC SYMBOL



SYSTEM DIAGRAM



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ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ~ 7	V
DC Input Voltage	V_{IN}	-0.5 ~ $V_{CC}+0.5$	V
DC Output Voltage	V_{OUT}	-0.5 ~ $V_{CC}+0.5$	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±35	mA
DC V_{CC} /Ground Current	I_{CC}	±75	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	-65 ~ 150	°C
Lead Temperature 10sec	T_L	300	°C

*500mW in the range of $T_a = -40^\circ\text{C} \sim 65^\circ\text{C}$. From $T_a = 65^\circ\text{C}$ to 85°C a derating factor of $-10\text{mW}/^\circ\text{C}$ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	-40 ~ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ~ 1000($V_{CC}=2.0\text{V}$)	ns
		0 ~ 500($V_{CC}=4.5\text{V}$)	
		0 ~ 400($V_{CC}=6.0\text{V}$)	

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	$T_a=25^\circ\text{C}$				$T_a=-40 \sim 85^\circ\text{C}$		UNIT	
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.		
High-Level Input Voltage	V_{IH}		2.0	1.5	-	-	1.5	-	V	
			4.5	3.15	-	-	3.15	-		
			6.0	4.2	-	-	4.2	-		
Low-Level Input Voltage	V_{IL}		2.0	-	-	0.5	-	0.5	V	
			4.5	-	-	1.35	-	1.35		
			6.0	-	-	1.8	-	1.8		
High-Level Output Voltage	V_{OH}	$V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OH} = -20 \mu\text{A}$	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
			$I_{OH} = -6 \text{ mA}$ $I_{OH} = -7.8 \text{ mA}$	6.0	5.9	6.0	-	5.9	-	
				4.5	4.18	4.31	-	4.13	-	
Low-Level Output Voltage	V_{OL}	$V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OL} = 20 \mu\text{A}$	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
			$I_{OL} = 6 \text{ mA}$ $I_{OL} = 7.8 \text{ mA}$	6.0	-	0.0	0.1	-	0.1	
				4.5	-	0.17	0.26	-	0.33	
3-State Output Off-State Current	I_{OZ}	$V_{IN} = V_{IH} \text{ or } V_{IL}$ $V_{OUT} = V_{CC} \text{ or } \text{GND}$	6.0	-	-	±0.5	-	±5.0	μA	
Input Leakage Current	I_{IN}	$V_{IN} = V_{CC} \text{ or } \text{GND}$	6.0	-	-	±0.1	-	±1.0		
Quiescent Supply Current	I_{CC}	$V_{IN} = V_{CC} \text{ or } \text{GND}$	-	-	-	4.0	-	40.0		

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TIMING REQUIREMENTS (Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION	T _a =25°C			T _a =-40 ~85°C	UNIT
			V _{CC}	TYP.	LIMIT	LIMIT	
Minimum Pulse Width (LE)	t _{w(GH)}		2.0	-	75	95	ns
			4.5	-	15	19	
			6.0	-	13	16	
Minimum Set-up Time (Data)	t _s		2.0	-	50	65	
			4.5	-	10	13	
			6.0	-	9	11	
Minimum Hold Time (Data)	t _h		2.0	-	5	5	
			4.5	-	5	5	
			6.0	-	5	5	

AC ELECTRICAL CHARACTERISTICS (Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION	CL	V _{CC}	T _a =25°C			T _a =-40 ~85°C		UNIT
					MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t _{TLH} t _{THL}		50	2.0	-	20	60	-	75	ns
				4.5	-	6	12	-	15	
				6.0	-	5	10	-	13	
Propagation Delay Time (LE-Q, \bar{Q})	t _{pLH}		50	2.0	-	42	125	-	155	
				4.5	-	14	25	-	31	
				6.0	-	12	21	-	26	
	t _{pHL}	150	2.0	-	57	175	-	220		
			4.5	-	19	35	-	44		
			6.0	-	16	30	-	37		
Propagation Delay Time (D-Q, \bar{Q})	t _{pLH}		50	2.0	-	42	125	-	155	
				4.5	-	14	25	-	31	
				6.0	-	12	21	-	26	
	t _{pHL}	150	2.0	-	57	175	-	220		
			4.5	-	19	35	-	44		
			6.0	-	16	30	-	37		
Output Enable time	t _{pZL}	R _L = 1 kΩ	50	2.0	-	39	125	-	155	
				4.5	-	13	25	-	31	
				6.0	-	11	21	-	26	
	t _{pZH}	150	2.0	-	54	175	-	220		
			4.5	-	18	35	-	44		
			6.0	-	15	30	-	37		
Output Disable time	t _{pLZ} t _{pHZ}	R _L = 1 kΩ	50	2.0	-	30	125	-	155	
				4.5	-	14	25	-	31	
				6.0	-	13	21	-	26	
Input Capacitance	C _{IN}				-	5	10	-	10	pF
Output Capacitance	C _{OUT}				-	10	-	-	-	
Power Dissipation Capacitance	C _{PD(1)}				-	38	-	-	-	

Note(1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

$$I_{CC(tot)} = C_{PD} \cdot V_{CC} \cdot f_L + I_{CC} / 8 (\text{per Latch})$$

And the total C_{PD} when n pcs. of Latch operate can be gained by the following equation:

$$C_{PD(\text{total})} = 22 + 16 \cdot n$$