

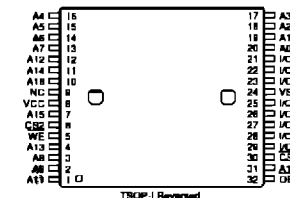
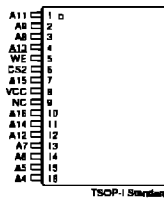
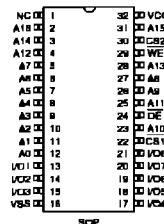
DESCRIPTION

The HY628100 is a high-speed, low power and 131,072 x 8-bits CMOS static RAM fabricated using Hyundai's high performance twin tub CMOS process technology. This high reliability process coupled with innovative circuit design techniques, yields maximum access time of 70ns. The HY628100 has a data retention mode that guarantees data to remain valid at a minimum power supply voltage of 2.0 volt. Using CMOS technology, supply voltages from 2.0 to 5.5 volt have little effect on supply current in data retention mode. Reducing the supply voltage to minimize current drain is unnecessary with the HY628100 Series.

FEATURES

- High speed - 70/85/100/120ns (max.)
- Low power consumption
 - Operating : 150 mW (typ.)
 - Standby (CMOS) : 5 μ W (typ.)
- Single 5V \pm 10% power supply
- Battery backup (L/LL-part)
 - 2.0V (min.) data retention
- Fully static operation
 - No clock or refresh required
- TTL compatible inputs and outputs
- Tri-state output
- Standard pin configuration
 - 32 pin 500 mil PDIP
 - 32 pin 525 mil SOP
 - 32 pin 8x20 mm TSOP-I

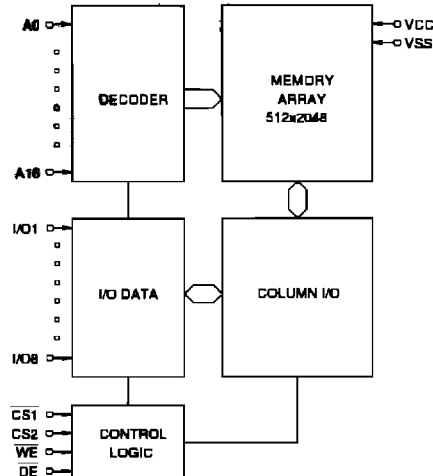
PIN CONNECTION



PIN DESCRIPTION

Pin Name	Pin Function
CS1	Chip Select 1
CS2	Chip Select 2
WE	Write Enable
OE	Output Enable
A0-A15	Address Inputs
I/O1-I/O8	Data Input/Output
Vcc	Power (+ 5V)
Vss	Ground

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS⁽¹⁾

SYMBOL	PARAMETER	RATING	UNIT
V _{CC} , V _{IN} , V _{OUT}	Power Supply, Input/Output Voltage	- 0.5 to 7.0	V
T _A	Operating Temperature	0 to 70	°C
T _{BIAS}	Temperature under Bias	- 10 to 125	°C
T _{STG}	Storage Temperature	- 65 to 150	°C
P _D	Power Dissipation	1.0	W
I _{OUT}	Data Output Current	50	mA
T _{SOLDER}	Lead Soldering Temperature & Time	260•10	°C •sec

Note :

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational of this specification is not implied. Exposure to absolute maximum rating conditions for extended period may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(T_A= 0°C to 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V _{CC}	Power Supply Voltage	4.5	5.0	5.5	V
V _{IH}	Input High Voltage	2.2	-	V _{CC} + 0.5	V
V _{IL}	Input Low Voltage	-0.5 ⁽¹⁾	-	0.8	V

Note :

1. V_{IL} = -3.0V for pulse width less than 50ns.

TRUTH TABLE

MODE	I/O OPERATION	CS1	CS2	WE	DE
Standby	High-Z	H	X	X	X
	High-Z	X	L	X	X
Output Disabled	High-Z	L	H	H	H
Read	Data Out	L	H	H	L
Write	Data In	L	H	L	X

Note :

1. H= V_{IH}, L= V_{IL}, X= Don't Care

DC CHARACTERISTICS

(TA= 0°C to 70°C, VCC= 5V ± 10%, unless otherwise specified.)

SYMBOL	PARAMETER	TEST CONDITIONS	POWER	MIN.	TYP.	MAX.	UNIT
I _{LI}	Input Leakage Current	V _{SS} ≤ V _{IN} ≤ V _{CC}		-1	-	1	μA
I _{LO}	Output Leakage Current	V _{SS} ≤ V _{OUTS} ≤ V _{CC} , CS1= V _{IH} or CS2= V _{IL} or OE= V _{IH} or WE= V _{IL}		-1	-	1	μA
I _{CC}	Operating Power Supply Current	CS1= V _{IL} , CS2= V _{IH} , V _{IN} = V _{IH} or V _{IL} , I _{I/O} = 0mA		-	30	50	mA
I _{CC1}	Average Operating Current	CS1 = V _{IL} , CS2= V _{IH} Min. Duty Cycle= 100%, I _{I/O} = 0mA		-	40	70	mA
I _{SB}	TTL Standby Current (TTL Inputs)	CS1= V _{IH} or CS2= V _{IL}		-	1	3	mA
I _{SB1}	CMOS Standby Current (CMOS Inputs)	CS1 ≥ V _{CC} - 0.2V, CS2 ≤ 0.2V or CS2 ≥ V _{CC} - 0.2V		-	-	2	mA
			L	-	2	100	μA
			LL	-	1	50	μA
V _{OL}	Output Low Voltage	I _{OL} = 2.1mA		-	-	0.4	V
V _{OH}	Output High Voltage	I _{OH} = - 1.0mA		2.4	-	-	V

Note :

1. Typical values are at VCC= 5.0V, TA= 25°C.

AC CHARACTERISTICS

(TA= 0°C to 70°C, VCC= 5V ±10%, unless otherwise noted.)

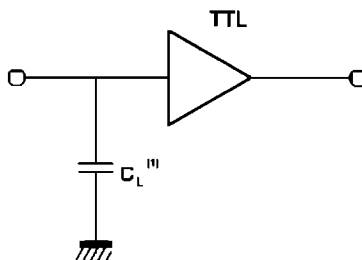
#	SYMBOL	PARAMETER	-70		-85		-10		-12		UNIT
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
READ CYCLE											
1	tRC	Read Cycle Time	70	-	85	-	100	-	120	-	ns
2	tAA	Address Access Time	-	70	-	85	-	100	-	120	ns
3	tACS	Chip Select Access Time	-	70	-	85	-	100	-	120	ns
4	tOE	Output Enable to Output Valid	-	35	-	45	-	50	-	60	ns
5	tCLZ	Chip Select to Low-Z Output	10	-	10	-	10	-	15	-	ns
6	tOLZ	Output Enable to Low-Z Output	5	-	5	-	5	-	5	-	ns
7	tCHZ	Chip Disable to High-Z Output	0	25	0	30	0	35	0	40	ns
8	tOHZ	Output Disable to High-Z Output	0	25	0	30	0	35	0	40	ns
9	tDH	Output Hold from Address Change	10	-	10	-	10	-	10	-	ns
WRITE CYCLE											
10	tWC	Write Cycle Time	70	-	85	-	100	-	120	-	ns
11	tCW	Chip Select to End of Write	60	-	75	-	90	-	100	-	ns
12	tAW	Address Valid to End of Write	60	-	75	-	90	-	100	-	ns
13	tAS	Address Set-up Time	0	-	0	-	0	-	0	-	ns
14	tWP	Write Pulse Width	50	-	60	-	70	-	80	-	ns
15	tWR	Write Recovery Time	0	-	0	-	0	-	0	-	ns
16	tWHZ	Write to High-Z Output	0	25	0	30	0	30	0	30	ns
17	tDW	Data to Write Time Overlap	35	-	35	-	40	-	50	-	ns
18	tDH	Data Hold from Write Time	0	-	0	-	0	-	0	-	ns
19	tOW	Output Active from End of Write	5	-	5	-	5	-	5	-	ns

AC TEST CONDITIONS

($T_A = 0^\circ\text{C}$ to 70°C , $V_{CC} = 5\text{V} \pm 10\%$, unless otherwise specified.)

PARAMETER	VALUE
Input Pulse Level	0.8V to 2.4V
Input Rise and Fall Time	5ns
Input and Output Timing Reference Levels	1.5V
Output Load	$C_L = 100\text{pF} + 1\text{TTL Load}$

AC TEST LOADS



Notes :
1. Including jig and scope capacitance.

CAPACITANCE

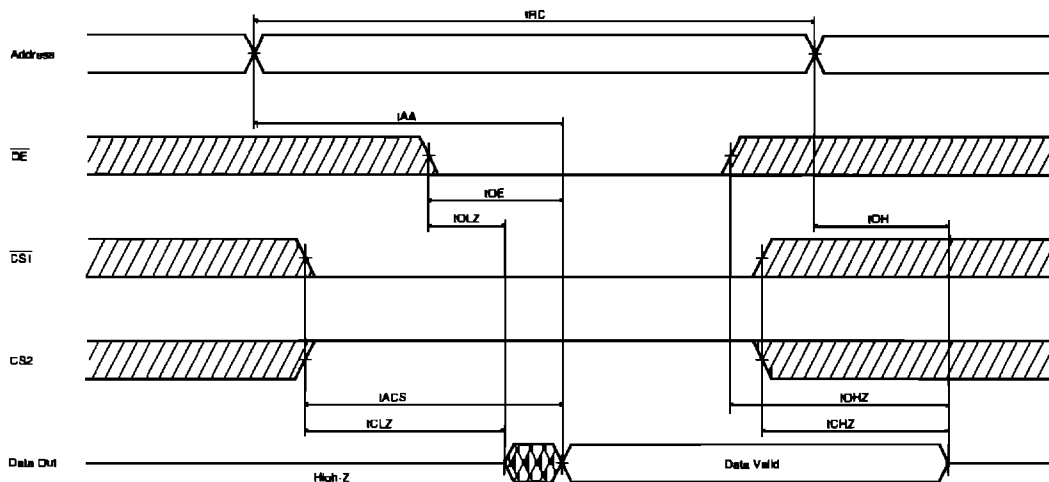
($T_A = 25^\circ\text{C}$, $f = 1\text{MHz}$)

SYMBOL	PARAMETER	CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	$V_{IN} = 0\text{V}$	6	pF
$C_{I/O}$	Input/Output Capacitance	$V_{I/O} = 0\text{V}$	8	pF

Notes :
1. This parameter is sampled and not 100% tested.

TIMING DIAGRAM

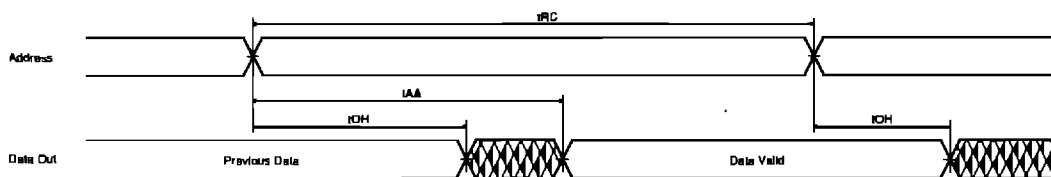
READ CYCLE 1



Note (READ CYCLE):

1. I_{CHZ} and I_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, I_{CHZ} max. is less than t_{CLZ} min. both for a given device and from device to device.
3. WE is high for read cycle.

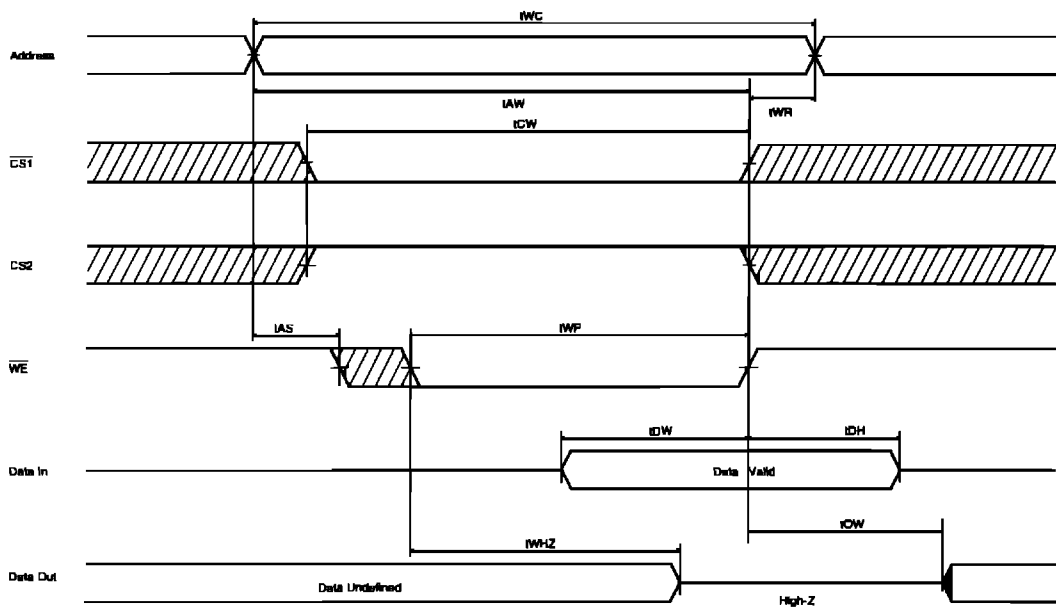
READ CYCLE 2



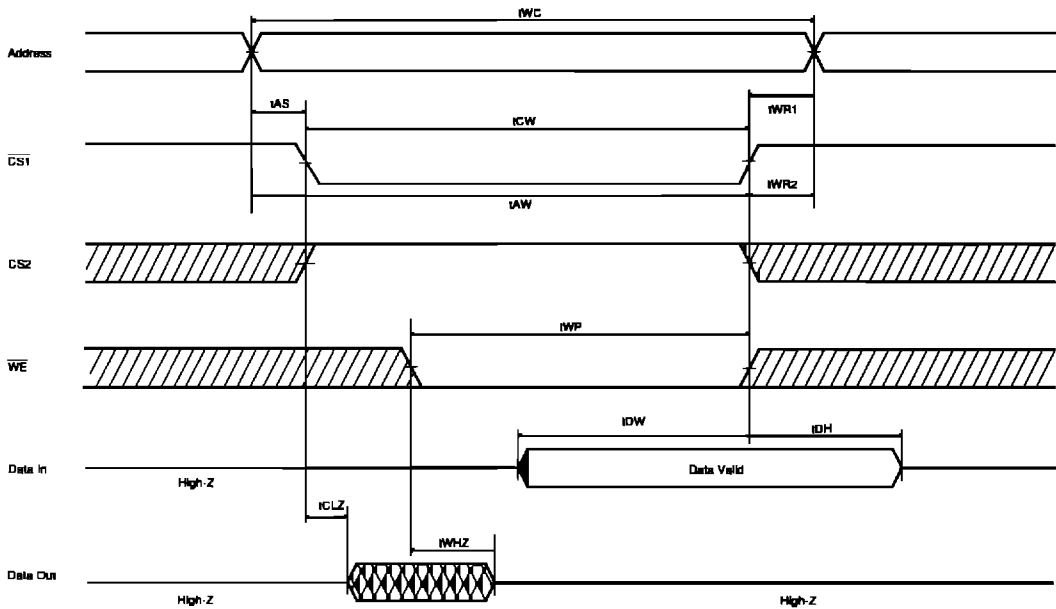
Note(READ CYCLE):

1. WE is high for read cycle.
2. Device is continuously selected $CS1 = V_{IL}$, $CS2 = V_{IH}$.
3. $OE = V_{IL}$.

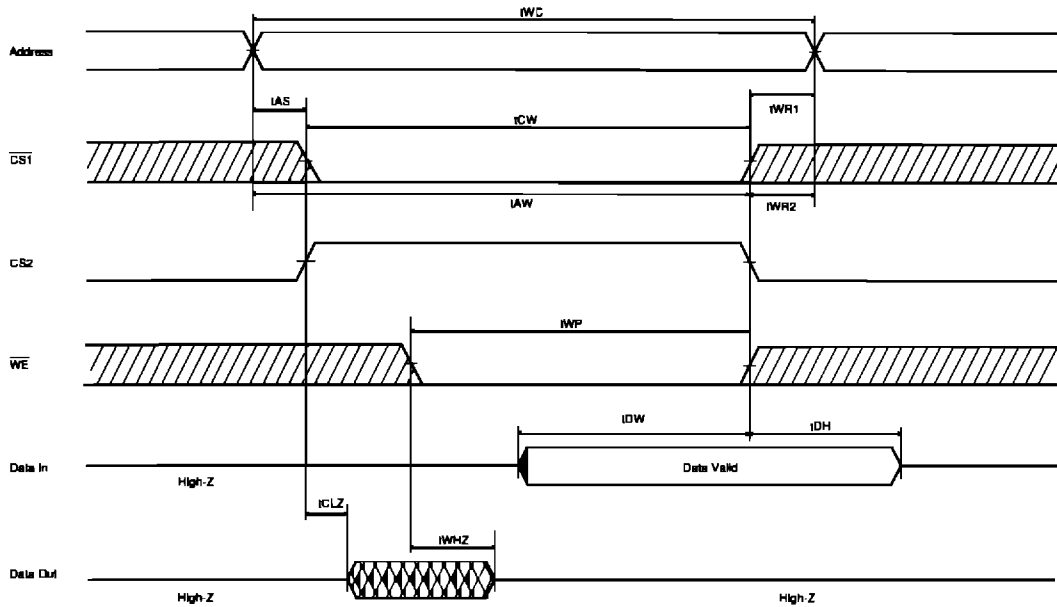
WRITE CYCLE 1 (WE Controlled)



WRITE CYCLE 2 (CS1 Controlled)



WRITE CYCLE 3 (CS2 Controlled)



Note (WRITE CYCLE):

1. A write occurs during the overlap of a low $\overline{CS1}$ and high CS2 and a low \overline{WE} . A write begins at the latest transition among $\overline{CS1}$ going low, CS2 going high and \overline{WE} going low. A write ends at the earliest transition among $\overline{CS1}$ going high, CS2 going low and \overline{WE} going high. t_{WP} is measured from the beginning of write to the end of write.
2. t_{AW} is measured from the later of $\overline{CS1}$ going low or CS2 going high to end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR1} is measured from the end of write to the address change. t_{WR1} applied in case a write ends as $\overline{CS1}$, or \overline{WE} going high, t_{WR2} applied in case a write ends at CS2 going low.
5. If \overline{OE} , CS2 and \overline{WE} are in the read mode during this period, the I/O pins are in the output low-Z state, inputs of opposite phase of the output must not be applied because bus contention can occur.
6. if $\overline{CS1}$ goes low simultaneously with \overline{WE} going low or after \overline{WE} going low, the outputs remain in high impedance state.
7. D_{OUT} is the read data of the new address.
8. When $\overline{CS1}$ is low and CS2 is high, I/O pins are in the output state. The input signals in the opposite phase leading to the outputs should not be applied.

DATA RETENTION CHARACTERISTICS

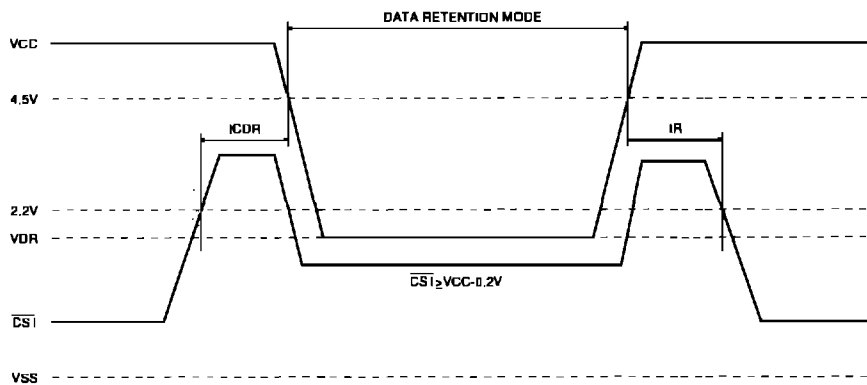
($T_A = 0^\circ\text{C}$ to 70°C)

SYMBOL	PARAMETER	TEST CONDITION	POWER	MIN.	TYP.	MAX.	UNIT
VDR	VCC for Data Retention	$CS1 \geq V_{CC}-0.2V$, $CS2 \leq 0.2V$ or $\geq V_{CC}-0.2V$, $V_{SS} \leq V_{IN} \leq V_{CC}$		2.0	-	-	V
ICCDR	Data Retention Current	$V_{CC} = 3.0V$, $CS1 \geq V_{CC}-0.2V$, $CS2 \leq 0.2V$ or $\geq V_{CC}-0.2V$, $V_{SS} \leq V_{IN} \leq V_{CC}$	L	-	2	50	μA
			LL	-	1	30 ⁽²⁾	μA
ICDR	Chip Disable to Data Retention Time	See Data Retention Timing Diagram		0	-	-	ns
IR	Operating Recovery Time		t_{RC} ⁽³⁾	-	-	-	ns

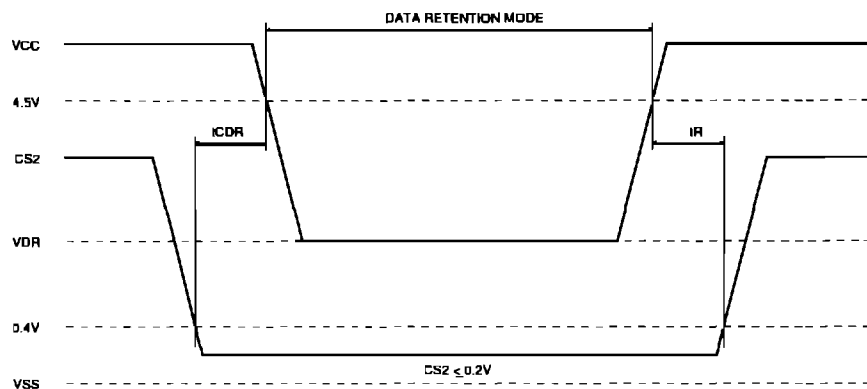
Notes :

1. Typical values are at the condition of $T_A = 25^\circ\text{C}$.
2. $3\mu\text{A}$ max. at $T_A = 0^\circ\text{C}$ to 40°C .
3. t_{RC} is read cycle time.

DATA RETENTION TIMING DIAGRAM 1

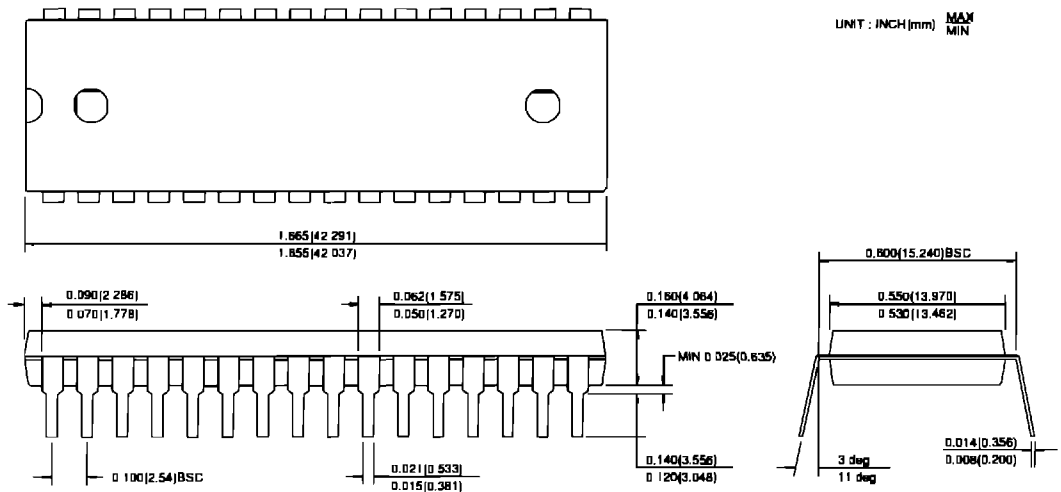


DATA RETENTION TIMING DIAGRAM 2

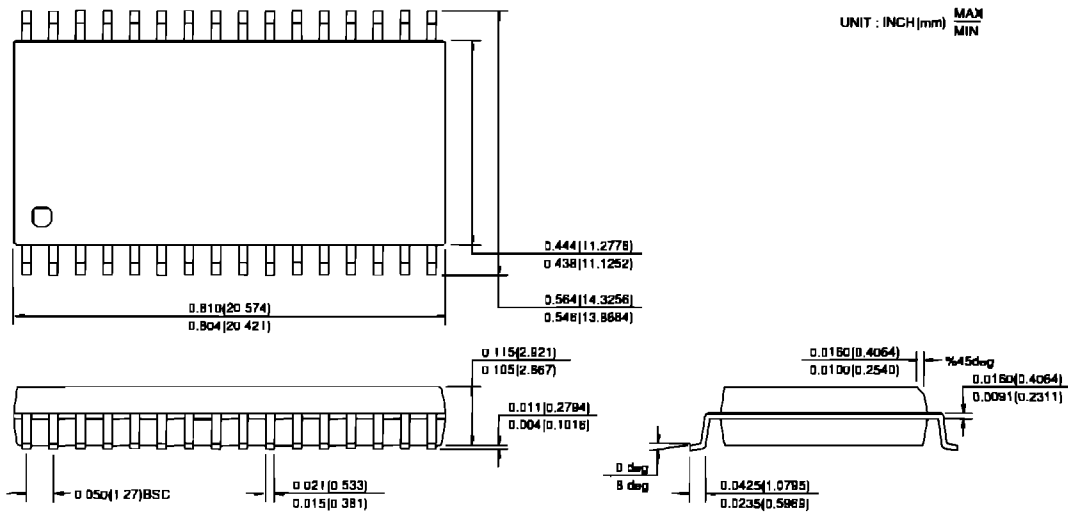


PACKAGE INFORMATION

600 mil 32 pin Plastic Dual In Line Package (P)

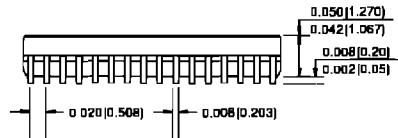
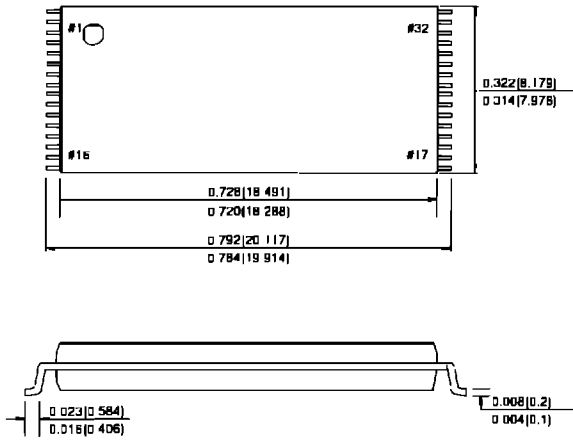


525 mil 32 pin Small Outline Package (G)



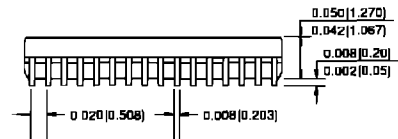
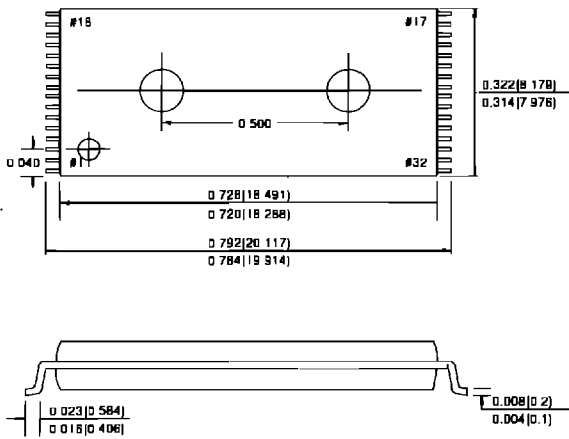
32 pin Thin Small Outline Package 8 x 20 mm Standard (T1)

UNIT : INCH(mm)



32 pin Thin Small Outline Package 8 x 20 mm Reversed (R1)

UNIT : INCH(mm)



ORDERING INFORMATION

PART NO.	SPEED	POWER	PACKAGE
HY62B100P	70/85/100/120		PDIP
HY62B100LP	70/85/100/120	L-part	PDIP
HY62B100LLP	70/85/100/120	LL-part	PDIP
HY62B100G	70/85/100/120		SOP
HY62B100LG	70/85/100/120	L-part	SOP
HY62B100LLG	70/85/100/120	LL-part	SOP
HY62B100T1	70/85/100/120		TSOP-I Standard
HY62B100LT1	70/85/100/120	L-part	TSOP-I Standard
HY62B100LLT1	70/85/100/120	LL-part	TSOP-I Standard
HY62B100R1	70/85/100/120		TSOP-I Reversed
HY62B100LR1	70/85/100/120	L-part	TSOP-I Reversed
HY62B100LLR1	70/85/100/120	LL-part	TSOP-I Reversed