



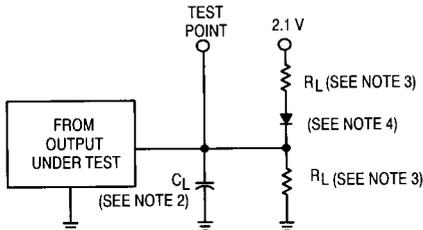
Quad 2-Input Data Selector/Multiplexer 3-State Outputs With Enable

ELECTRICALLY TESTED PER:
MIL-M-38510/30906

The 54LS257A is a Quad 2-Input Multiplexer with 3-state outputs. Four bits of data from two sources can be selected using a Common Data Select input. The four outputs present the selected data in true (non-inverted) form. The outputs may be switched to a high impedance state with HIGH on the common Output Enable (\overline{EO}) Input, allowing the outputs to interface directly with the bus oriented systems. It is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all Motorola TTL families.

- Schottky Process For High-Speed
- Multiplexer Expansion By Tying Outputs Together
- Non-Inverting 3-State Outputs
- Input Clamp Diodes Limit High-Speed Termination Effects

LOAD CIRCUIT FOR 3-STATE OUTPUT



TRUTH TABLE				
Output Enable	Select Input	Data Inputs		Output
\overline{EO}	S	I_0	I_1	Z
H	X	X	X	(Z)
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
(Z) = High Impedance

Military 54LS257A



AVAILABLE AS:

- 1) JAN: JM38510/30906BXA
- 2) SMD: 7603701
- 3) 883: 54LS257A/BXAJC

X = CASE OUTLINE AS FOLLOWS:
PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

THE LETTER "M" APPEARS
BEFORE THE / ON LCC.

PIN ASSIGNMENTS

FUNCT.	DIL 620-09	FLATS 650-05	LCC 756A-02	BURN-IN (COND. A)
S	1	1	2	VCC
I_{0a}	2	2	3	VCC
I_{1a}	3	3	4	VCC
Z_a	4	4	5	OPEN
I_{0b}	5	5	7	VCC
I_{1b}	6	6	8	VCC
Z_b	7	7	9	OPEN
GND	8	8	10	GND
Z_d	9	9	12	OPEN
I_{1d}	10	10	13	VCC
I_{0d}	11	11	14	VCC
Z_c	12	12	15	OPEN
I_{1c}	13	13	17	VCC
I_{0c}	14	14	18	VCC
\overline{EO}	15	15	19	VCC
VCC	16	16	20	VCC

BURN-IN CONDITIONS:
VCC = 5.0 V MIN/6.0 V MAX

NOTES:

1. Input pulse characteristics: PRR \leq 1.0 MHz, $t_r = 15$ ns, $t_f \leq 6.0$ ns.
2. $C_L = 50$ pF \pm 10% for t_{pLH} , t_{PHL} , t_{pZL} and t_{pZH} tests, $C_L = 15$ pF minimum for t_{pHZ} and t_{pLZ} tests. C_L includes scope probe, wiring and stray capacitance.
3. $R_L = 2.0$ k Ω \pm 5.0%.
4. All diodes are 1N3064 or 1N916.
5. The limits specified for $C_L = 15$ pF, and $C_L = 5.0$ pF are guaranteed but not tested.

54LS257A

FUNCTIONAL DESCRIPTION

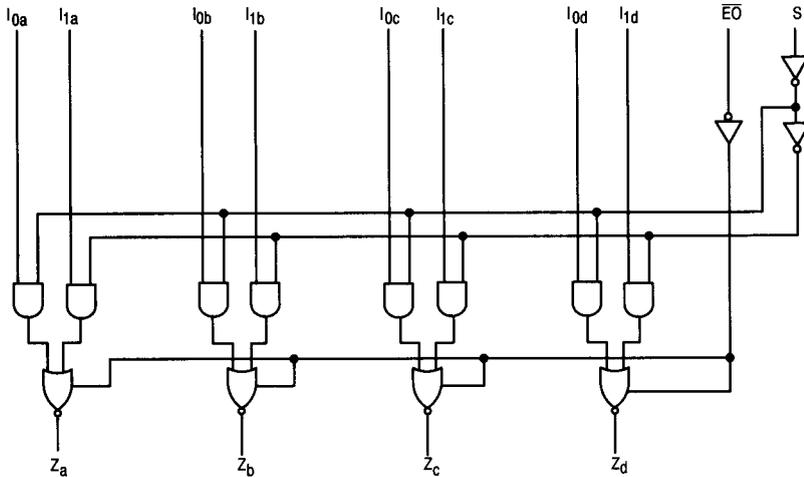
The 'LS257A is a Quad 2-input Multiplexer with 3-state outputs. It selects four bits of data from two sources under the control of a Common Data Select input. When the Select input is LOW, the I_0 inputs are selected and when Select is HIGH, I_1 inputs are selected. The data on the selected inputs appears at the outputs in true (non-inverted) form. The device is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select input. The logic equations for the outputs are shown:

$$Z_a = \overline{EO} \cdot (I_{1a} \cdot S + I_{0a} \cdot \overline{S}) \quad Z_b = \overline{EO} \cdot (I_{1b} \cdot S + I_{0b} \cdot \overline{S})$$

$$Z_c = \overline{EO} \cdot (I_{1c} \cdot S + I_{0c} \cdot \overline{S}) \quad Z_d = \overline{EO} \cdot (I_{1d} \cdot S + I_{0d} \cdot \overline{S})$$

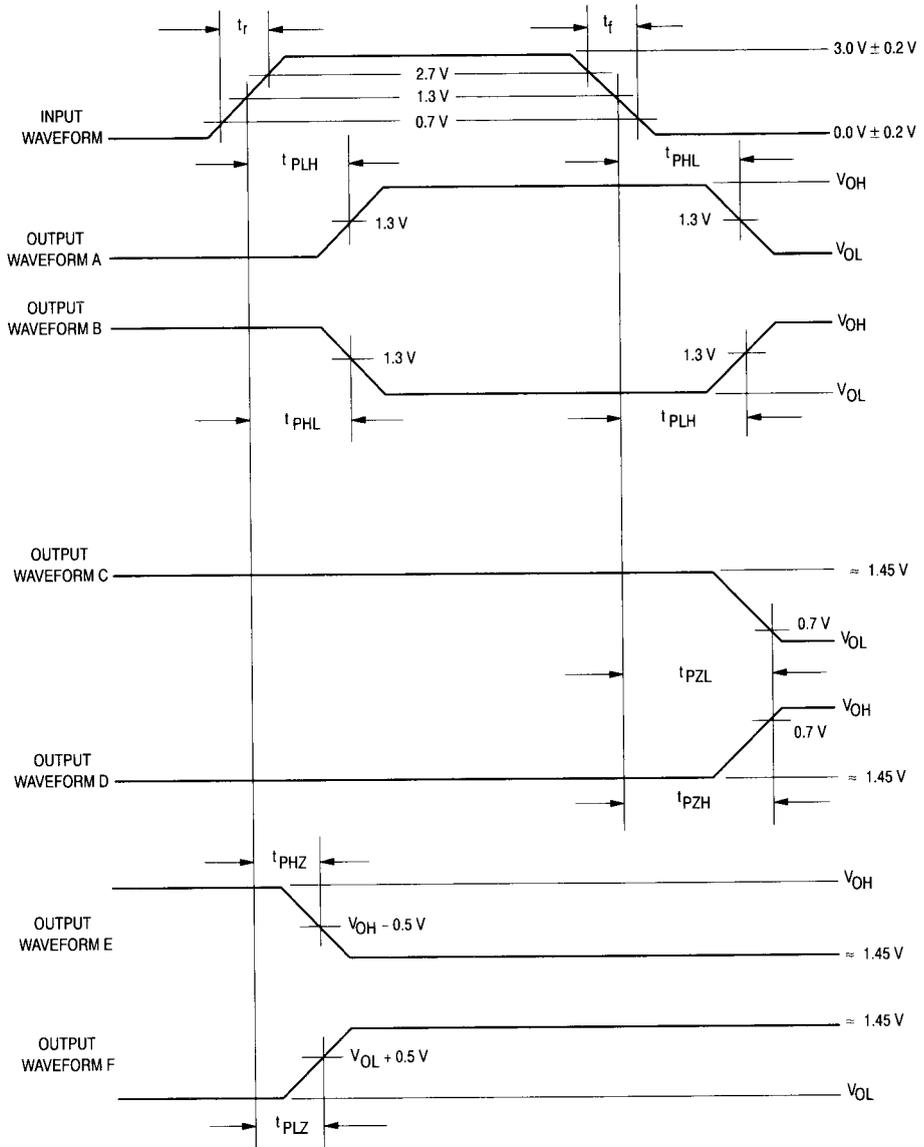
When the Output Enable Input (\overline{EO}) is HIGH, the outputs are forced to a high impedance "Off" state. If the outputs are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure the Output Enable signals to 3-state devices whose outputs are tied together are designed so there is no overlap.

LOGIC DIAGRAM



54LS257A

WAVEFORMS



5

54LS257A

Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
		+ 25°C		+ 125°C		- 55°C			
		Subgroup 1		Subgroup 2		Subgroup 3			
		Min	Max	Min	Max	Min	Max		
V _{OH}	Logical "1" Output Voltage	2.4		2.4		2.4		V	V _{CC} = 4.5 V, I _{OH} = -1.0 mA, V _{IH} = 2.0 V, S = 0.7 V or 2.0 V, V _{IL} = 0.7 V, E _O = 0.7 V, other inputs are open.
V _{OL}	Logical "0" Output Voltage		0.4		0.4		0.4	V	V _{CC} = 4.5 V, I _{OL} = 12 mA, V _{IL} = 0.7 V, S = 2.0 V, V _{IN} = 2.0 V, E _O = 0.7 V, other inputs are open.
V _{IC}	Input Clamping Voltage		- 1.5					V	V _{CC} = 4.5 V, I _{IN} = -18 mA, other inputs are open.
I _{IH}	Logical "1" Input Current		20		20		20	μA	V _{CC} = 5.5 V, V _{IH} = 2.7 V, other inputs are open, S = 5.5 V or GND.
I _{IHH}	Logical "1" Input Current		100		100		100	μA	V _{CC} = 5.5 V, V _{IHH} = 5.5 V, other inputs are open, S = 5.5 V or GND.
I _{IH(S)}	Logical "1" Input Current		40		40		40	μA	V _{CC} = 5.5 V, V _{IH} = 2.7 V, other inputs are open.
I _{IHH(S)}	Logical "1" Input Current		200		200		200	μA	V _{CC} = 5.5 V, V _{IHH} = 5.5 V, other inputs are open.
I _{IL}	Logical "0" Input Current	- 0	- 0.2	- 0	- 0.2	- 0	- 0.2	mA	V _{CC} = 5.5 V, V _{IN} = 0.4 V, other inputs are open, S = 5.5 V or GND.
I _{IL(S)}	Logical "0" Input Current	- 0	- 0.1	- 0	- 0.1	- 0	- 0.1	mA	V _{CC} = 5.5 V, V _{IN} = 0.4 V, other inputs are open.
I _{OS}	Output Short Circuit Current	- 30	- 130	- 30	- 130	- 30	- 130	mA	V _{CC} = 5.5 V, V _{IN} = 5.5 V, other inputs are open, V _{OUT} = GND S & E _O = GND.
I _{OZH}	Output Off Current High		20		20		20	μA	V _{CC} = 5.5 V, V _{IN} = 0.7 V, all other inputs are open, V _{OUT} = 2.7 V, E _O & S = 2.0 V.
I _{OZL}	Output Off Current Low		- 20		- 20		- 20	μA	V _{CC} = 5.5 V, V _{IN} = 2.0 V, V _{OUT} = 0.4 V, S = 0.7 V, E _O = 2.0 V.
I _{CCH}	Power Supply Current		10		10		10	mA	V _{CC} = 5.5 V, V _{IN} = 5.5 V (all inputs), E _O = GND.
I _{CCL}	Power Supply Current		16		16		16	mA	V _{CC} = 5.5 V, all inputs are GND.
I _{CCZ}	Power Supply Current		19		19		19	mA	V _{CC} = 5.5 V, all inputs are GND, E _O = 5.5 V
V _{IH}	Logical "1" Input Voltage	2.0		2.0		2.0		V	V _{CC} = 4.5 V.
V _{IL}	Logical "0" Input Voltage		0.7		0.7		0.7	V	V _{CC} = 4.5 V.
	Functional Tests	Subgroup 7		Subgroup 8A		Subgroup 8B			per Truth Table with V _{CC} = 5.0 V, V _{INL} = 0.4 V, and V _{INH} = 2.4 V.

54LS257A

Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
		+ 25°C		+ 125°C		- 55°C			
		Subgroup 9		Subgroup 10		Subgroup 11			
		Min	Max	Min	Max	Min	Max		
t _{PHL1} t _{PHL1}	Propagation Delay /Data-Output Data to Output	3.0 —	23 18	3.0 —	35 30	3.0 —	35 30	ns	V _{CC} = 5.0 V, C _L = 50 pF, R _L = 2.0 kΩ V _{CC} = 5.0 V, C _L = 45 pF.
t _{PLH1} t _{PLH1}	Propagation Delay /Data-Output Data to Output	3.0 —	23 18	3.0 —	35 30	3.0 —	35 30	ns	V _{CC} = 5.0 V, C _L = 50 pF, R _L = 2.0 kΩ V _{CC} = 5.0 V, C _L = 45 pF.
t _{PHL5} t _{PHL5}	Propagation Delay /Data-Output Select to Output	3.0 —	26 21	3.0 —	39 34	3.0 —	39 34	ns	V _{CC} = 5.0 V, C _L = 50 pF, R _L = 2.0 kΩ V _{CC} = 5.0 V, C _L = 45 pF.
t _{PLH5} t _{PLH5}	Propagation Delay /Data-Output Select to Output	3.0 —	26 21	3.0 —	39 34	3.0 —	39 34	ns	V _{CC} = 5.0 V, C _L = 50 pF, R _L = 2.0 kΩ V _{CC} = 5.0 V, C _L = 45 pF.
t _{PZH3} t _{PZH3}	Propagation Delay /Data-Output Output High-Low	3.0 —	35 30	3.0 —	53 48	3.0 —	53 48	ns	V _{CC} = 5.0 V, C _L = 50 pF, R _L = 2.0 kΩ V _{CC} = 5.0 V, C _L = 45 pF, R _L = 667 Ω.
t _{PZL3} t _{PZL3}	Propagation Delay /Data-Output Output High-Low	3.0 —	35 30	3.0 —	53 48	3.0 —	53 48	ns	V _{CC} = 5.0 V, C _L = 50 pF, R _L = 2.0 kΩ V _{CC} = 5.0 V, C _L = 45 pF, R _L = 667 Ω.
t _{PHZ3} t _{PHZ3}	Propagation Delay /Data-Output Output High-Low	3.0 —	35 30	3.0 —	53 48	3.0 —	53 48	ns	V _{CC} = 5.0 V, C _L = 15 pF, R _L = 2.0 kΩ V _{CC} = 5.0 V, C _L = 15 pF, R _L = 667 Ω.
t _{PLZ3} t _{PLZ3}	Propagation Delay /Data-Output Output Low-High	3.0 —	30 25	3.0 —	45 40	3.0 —	45 40	ns	V _{CC} = 5.0 V, C _L = 5.0 pF, R _L = 2.0 kΩ V _{CC} = 5.0 V, C _L = 5.0 pF, R _L = 667 Ω.