


SGS-THOMSON
 MICROELECTRONICS

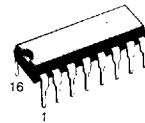
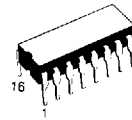
M54/74HC190
M54/74HC191

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T-45-23-09

4-BIT SYNCHRONOUS UP/DOWN COUNTERS

- LOW POWER DISSIPATION
 $I_{CC} = 4 \mu\text{A (MAX.)}$ at $T_A = 25^\circ\text{C}$
- HIGH NOISE IMMUNITY
 $V_{NIH} = V_{NIL} = 28\% V_{CC}$ (Min.)
- OUTPUT DRIVE CAPABILITY
 10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
 $|I_{OH}| = I_{OL} = 4 \text{ mA (MIN.)}$
- BALANCED PROPAGATION DELAYS
 $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
 V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE
 WITH 54/74LS190/191


B1N
 Plastic Package

F1
 Ceramic Frit Seal Package

M1
 Micro Package

C1
 Plastic Chip Carrier

ORDERING NUMBERS:

 M54HCXXX F1
 M74HCXXX B1N
 M74HCXXX F1

 M74HCXXX C1
 M74HCXXX M1

DESCRIPTION

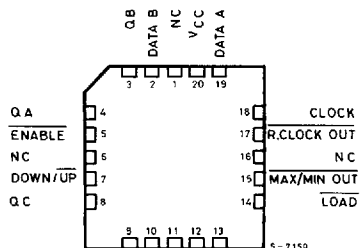
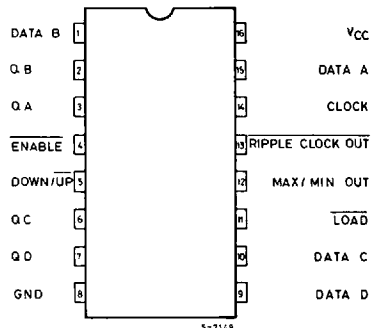
The M54/74HC190/191 are high speed CMOS 4-BIT SYNCHRONOUS UP/DOWN COUNTERS fabricated in silicon gate C²MOS technology. They have the same high speed performance of LSTTL combined with true CMOS low power consumption.

State changes of the counter are synchronous with the LOW-to-HIGH transition of the Clock Pulse input.

An asynchronous parallel load input overrides counting and loads the data present on the DATA inputs into the flip-flops, which makes it possible to use the circuits as programmable counters. A count enable input serves as the carry/borrow input in multi-stage counters. Control input, Down/Up, determines whether a circuit counts up or down. A MAX/MIN output and a Ripple Clock output provide overflow/underflow indication and make possible a variety of methods for generating carry/borrow signals in multi-stage counter applications.

All inputs are equipped with protection circuits against static discharge and transient excess voltage.

PIN CONNECTIONS (top view)


 NC =
 No Internal
 Connection

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TRUTH TABLE

INPUTS				OUTPUTS				FUNCTION
LOAD	ENABLE	D/U	CLOCK	QA	QB	QC	QD	
L	X	X	X	a	b	c	d	PRESET DATA
H	L	L	\uparrow	UP COUNT				UP COUNT
H	L	H	\downarrow	DOWN COUNT				DOWN COUNT
H	H	X	\uparrow	NO CHANGE				NO COUNT
H	X	X	\downarrow	NO CHANGE				NO COUNT

X : DON'T CARE

a-d:THE LEVEL OF STEADY STATE INPUTS AT INPUTS A THROUGH D RESPECTIVELY.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to 7	V
V_I	DC Input Voltage	-0.5 to $V_{CC}+0.5$	V
V_O	DC Output Voltage	-0.5 to $V_{CC}+0.5$	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
PD	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to 150	$^{\circ}C$

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

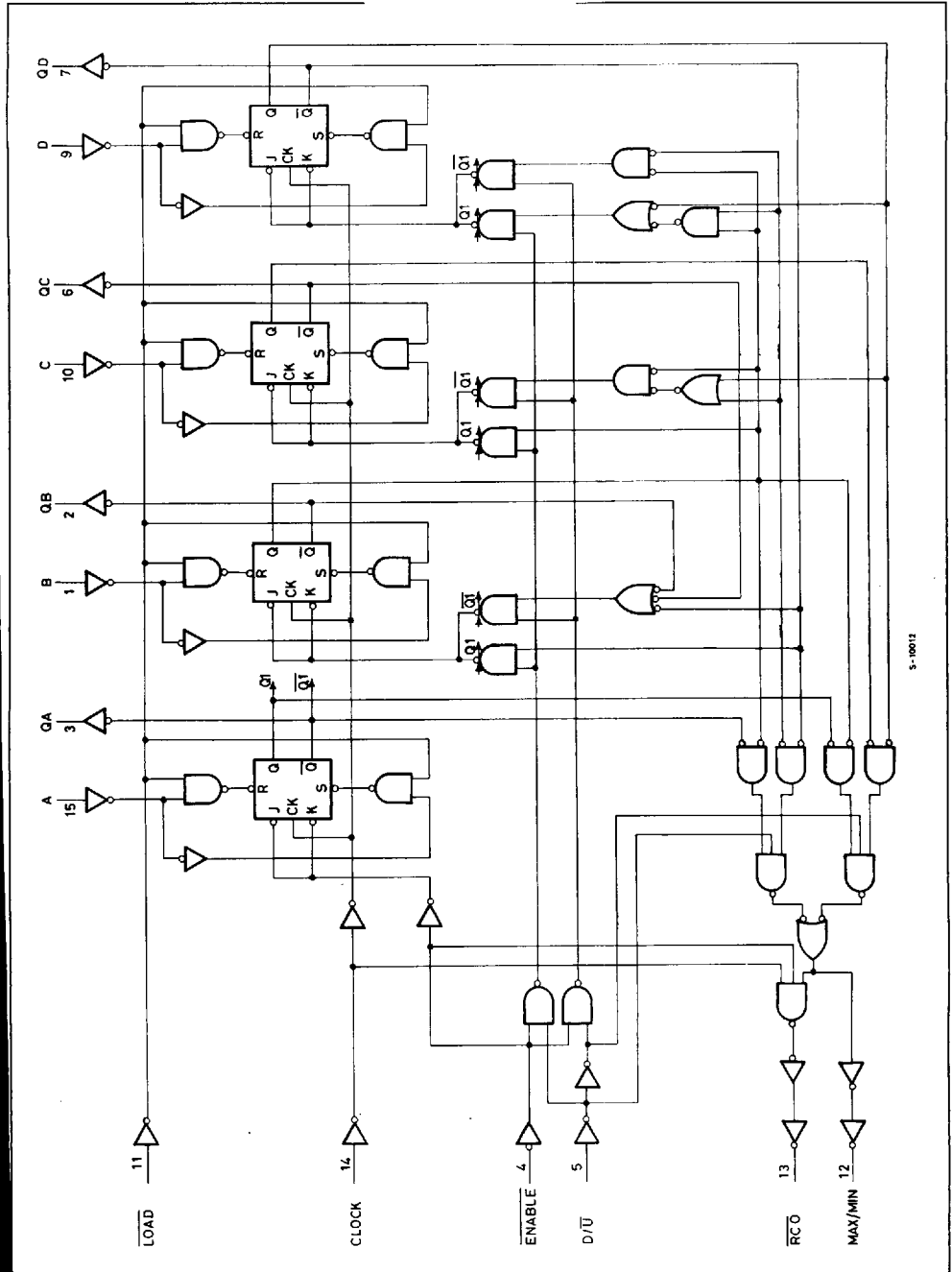
(*) 500 mW: $\cong 65^{\circ}C$ derate to 300 mW by 10 mW/ $^{\circ}C$: $65^{\circ}C$ to $85^{\circ}C$

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	2 to 6	V
V_I	Input Voltage	0 to V_{CC}	V
V_O	Output Voltage	0 to V_{CC}	V
T_A	Operating Temperature	74HC Series 54HC Series	$^{\circ}C$
t_r, t_f	Input Rise and Fall Time	V_{CC} $\left\{ \begin{array}{l} 2 \text{ V} \\ 4.5 \text{ V} \\ 6 \text{ V} \end{array} \right.$	ns
			0 to 1000 0 to 500 0 to 400

LOGIC DIAGRAM (HC190)

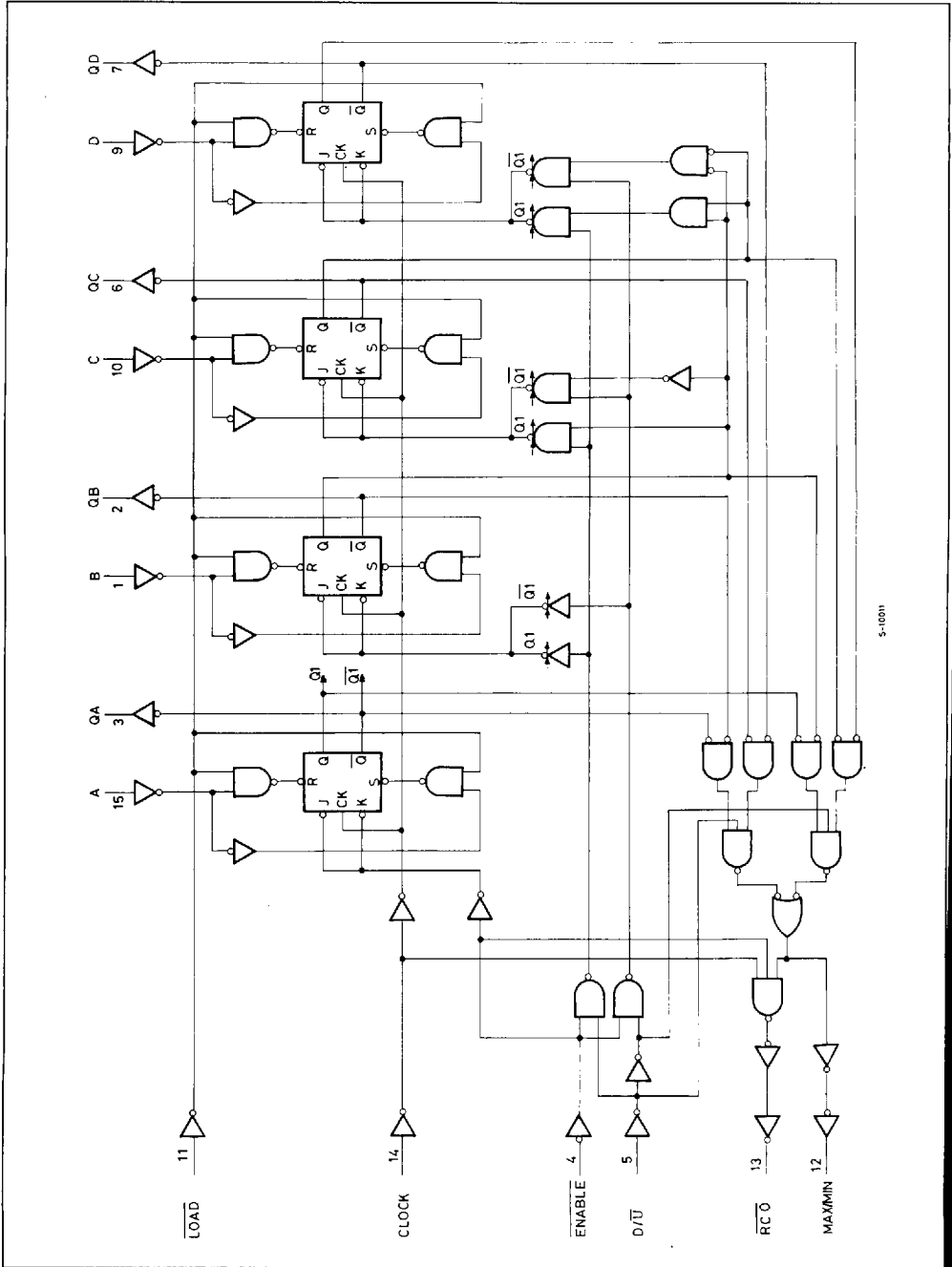
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5-100012

LOGIC DIAGRAM (HC191)

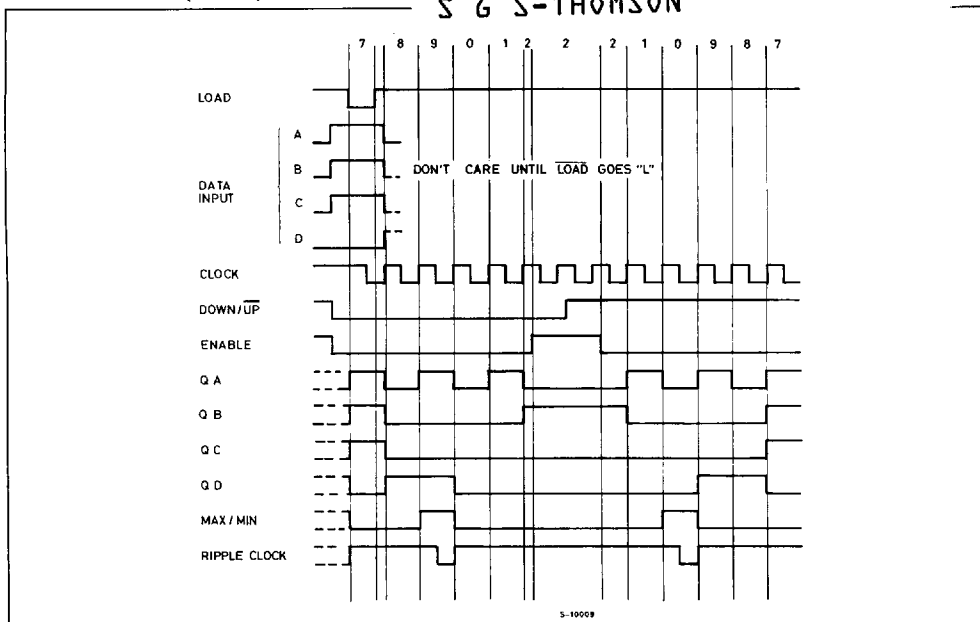
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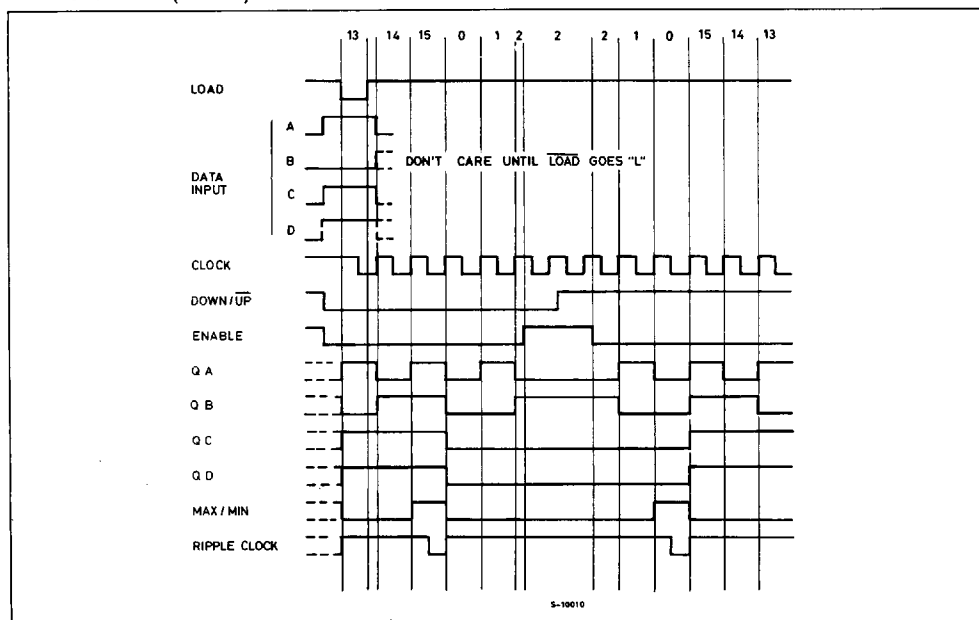
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TIMING CHART - (HC190)

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TIMING CHART (HC191)



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DC SPECIFICATIONS

Symbol	Parameter	V _{CC}	Test Condition	T _A = 25°C 54HC and 74HC			- 40 to 85°C 74HC		- 55 to 125°C 54HC		Unit	
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.		
V _{IH}	High Level Input Voltage	2.0 4.5 6.0		1.5 3.15 4.2	— — —	— — —	1.5 3.15 4.2	— — —	1.5 3.15 4.2	— — —	V	
V _{IL}	Low Level Input Voltage	2.0 4.5 6.0		— — —	— — —	0.5 1.35 1.8	— — —	0.5 1.35 1.8	— — —	0.5 1.35 1.8	V	
V _{OH}	High Level Output Voltage	2.0	V _{IN}	I _{OH}	1.9	2.0	—	1.9	—	1.9	—	V
		4.5	V _{IH} or V _{IL}	- 20 μA	4.4	4.5	—	4.4	—	4.4	—	
		6.0			5.9	6.0	—	5.9	—	5.9	—	
		4.5		- 4.0 mA	4.18	4.31	—	4.13	—	4.10	—	
		6.0		- 5.2 mA	5.68	5.8	—	5.63	—	5.60	—	
V _{OL}	Low Level Output Voltage	2.0	V _{IH} or V _{IL}	20 μA	—	0	0.1	—	0.1	—	0.1	V
		4.5			—	0	0.1	—	0.1	—	0.1	
		6.0			—	0	0.1	—	0.1	—	0.1	
		4.5		4.0 mA	—	0.17	0.26	—	0.33	—	0.40	
		6.0		5.2 mA	—	0.18	0.26	—	0.33	—	0.40	
I _{IN}	Input Leakage Current	6.0	V _{IN} = V _{CC} or GND	—	—	±0.1	—	±1	—	±1	μA	
I _{CC}	Quiescent Supply Current	6.0	V _{IN} = V _{CC} or GND	—	—	4	—	40	—	80		

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V, T_A = 25°C, C_L = 15pF, Input t_r = t_f = 6ns)

Symbol	Parameter	54HC and 74HC			Unit
		Min.	Typ.	Max.	
t _{TLH} t _{THL}	Output Transition Time		4	8	ns
t _{PLH} t _{PHL}	Propagation Delay Time (CLOCK-Q)		20	31	ns
t _{PLH} t _{PHL}	Propagation Delay Time (CLOCK-RCO)		14	22	ns
t _{PLH} t _{PHL}	Propagation Delay Time (CLOCK-MAX/MIN)		27	42	ns
t _{PLH} t _{PHL}	Propagation Delay Time (LOAD-Q)		23	35	ns
t _{PLH} t _{PHL}	Propagation Delay Time (DATA-Q)		19	30	ns

AC ELECTRICAL CHARACTERISTICS (Continued)

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Symbol	Parameter	54HC and 74HC			Unit
		Min.	Typ.	Max.	
t _{PLH} t _{PHL}	Propagation Delay Time (ENABLE-RCO)		14	22	ns
t _{PLH} t _{PHL}	Propagation Delay Time (D/ \bar{U} -RCO)		20	31	ns
t _{PLH} t _{PHL}	Propagation Delay Time (D/ \bar{U} -MAX/MIN)		17	27	ns
f _{MAX}	Maximum Clock Frequency	28	46		MHz

AC ELECTRICAL CHARACTERISTICS (C_L = 50pF, Input t_r = t_f = 6ns)

Symbol	Parameter	V _{CC}	Test Condition	T _A = 25°C 54HC and 74HC			-40 to 85°C 74HC		-55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t _{TLH} t _{THL}	Output Transition Time	2.0 4.5 6.0		— — —	30 8 7	75 15 13	— — —	95 19 16	— — —	110 22 19	ns
t _{PLH} t _{PHL}	Propagation Delay Time (CLOCK-Q)	2.0 4.5 6.0		— — —	92 23 20	180 36 31	— — —	225 45 38	— — —	270 54 46	ns
t _{PLH} t _{PHL}	Propagation Delay Time (CLOCK- \bar{RCO})	2.0 4.5 6.0		— — —	64 16 14	130 26 22	— — —	165 33 28	— — —	195 39 33	ns
t _{PLH} t _{PHL}	Propagation Delay Time (CLOCK-MAX/MIN)	2.0 4.5 6.0		— — —	124 31 26	240 48 41	— — —	300 60 51	— — —	360 72 61	ns
t _{PLH} t _{PHL}	Propagation Delay Time (LOAD-Q)	2.0 4.5 6.0		— — —	104 26 22	205 41 35	— — —	255 51 43	— — —	310 62 53	ns
t _{PLH} t _{PHL}	Propagation Delay Time (DATA-Q)	2.0 4.5 6.0		— — —	88 22 19	175 35 30	— — —	220 44 37	— — —	265 53 45	ns
t _{PLH} t _{PHL}	Propagation Delay Time (ENABLE-RCO)	2.0 4.5 6.0		— — —	64 16 14	130 26 22	— — —	165 33 28	— — —	195 39 33	ns
t _{PLH} t _{PHL}	Propagation Delay Time (D/ \bar{U} -RCO)	2.0 4.5 6.0		— — —	92 23 20	180 36 31	— — —	225 45 38	— — —	270 54 46	ns
t _{PLH} t _{PHL}	Propagation Delay Time (D/ \bar{U} -MAX/MIN)	2.0 4.5 6.0		— — —	80 20 17	160 32 27	— — —	200 40 34	— — —	240 48 41	ns

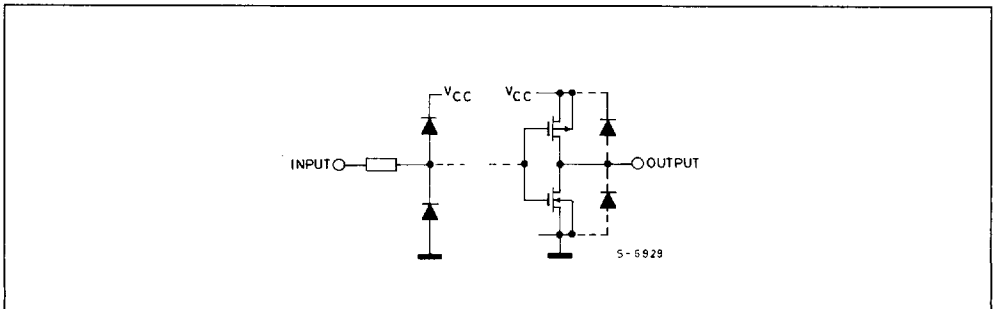
AC ELECTRICAL CHARACTERISTICS (Continued)

Symbol	Parameter	V _{CC}	Test Condition	T _A = 25°C 54HC and 74HC			-40 to 85°C 74HC		-55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
f _{MAX}	Maximum Clock Frequency	2.0 4.5 6.0		5 25 29	11 42 49	— — —	4 20 24	— — —	— — —	3 17 20	MHz
t _{W(H)} t _{W(L)}	Minimum Pulse Width (CLOCK)	2.0 4.5 6.0		— — —	45 11 9	100 20 17	— — —	125 25 21	— — —	150 30 26	ns
t _{W(L)}	Minimum Pulse Width (LOAD)	2.0 4.5 6.0		— — —	30 8 7	75 15 13	— — —	95 19 16	— — —	110 22 19	ns
t _{REM}	Minimum Removal Time	2.0 4.5 6.0		— — —	5 1 1	50 10 9	— — —	65 13 11	— — —	75 15 13	ns
t _s	Minimum Set-up Time (ENABLE-D/ <u>U</u>)	2.0 4.5 6.0		— — —	72 18 15	150 30 26	— — —	190 38 33	— — —	225 45 38	ns
t _h	Minimum Set-up Time (DATA-LOAD)	2.0 4.5 6.0		— — —	10 3 3	50 10 9	— — —	65 13 11	— — —	75 15 13	ns
t _h	Minimum Hold Time (ENABLE-D/ <u>U</u>)	2.0 4.5 6.0		— — —	— — —	0 0 0	— — —	0 0 0	— — —	0 0 0	ns
t _h	Minimum Hold Time (DATA-LOAD)	2.0 4.5 6.0		— — —	— — —	5 5 5	— — —	5 5 5	— — —	5 5 5	ns
C _{IN}	Input Capacitance			—	5	10	—	10	—	10	pF
C _{PD} (*)	Power Dissipation Capacitance			—	124	—	—	—	—	—	pF

Note (*) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit).

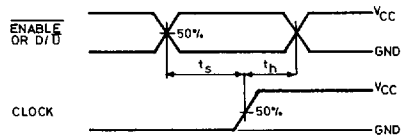
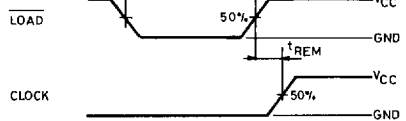
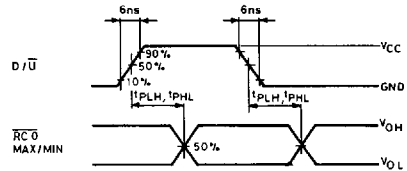
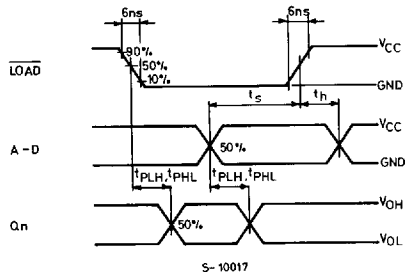
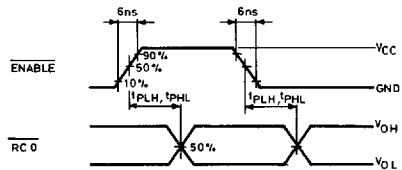
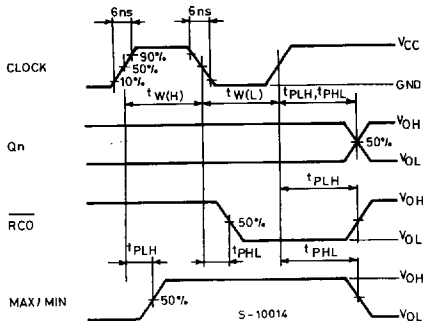
Average operating current can be obtained from the equation: I_{CC(opr.)} = C_{PD} · V_{CC} · f_{IN} + I_{CC}

INPUT AND OUTPUT EQUIVALENT CIRCUIT



SWITCHING CHARACTERISTICS TEST WAVEFORM

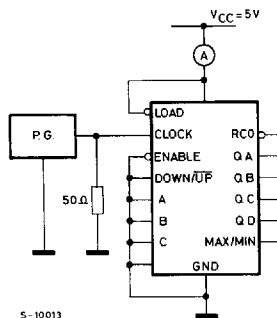
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S-10019

S-10018

TEST CIRCUIT I_{CC} (Opr.)



S-10013

INPUT TRANSITION TIME IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST