This X24128 device has been acquired by IC MICROSYSTEMS from Xicor, Inc.

ICmic IC MICROSYSTEMS

128K X24128 16K x 8 Bit

400KHz 2-Wire Serial E²PROM with Block Lock™

FEATURES

- Save Critical Data with Programmable Block Lock Protection
  - —Block Lock (0, 1/4, 1/2, or all of E²PROM Array)
  - —Software Write Protection
  - —Programmable Hardware Write Protect
- In Circuit Programmable ROM Mode
- 400KHz 2-Wire Serial Interface
  - —Schmitt Trigger Input Noise Suppression
  - —Output Slope Control for Ground Bounce Noise Elimination
- Longer Battery Life With Lower Power
  - —Active Read Current Less Than 1mA
  - —Active Write Current Less Than 3mA
  - —Standby Current Less Than 1∝A
- 1.8V to 3.6V, 2.5V to 5.5V and 4.5V to 5.5V Power Supply Versions
- 32 Word Page Write Mode
  - —Minimizes Total Write Time Per Word
- Internally Organized 16K x 8
- Bidirectional Data Transfer Protocol
- Self-Timed Write Cycle
  - —Typical Write Cycle Time of 5ms
- High Reliability
  - —Endurance: 100,000 Cycles
  - —Data Retention: 100 Years
- 14-Lead SOIC
- 16-Lead SOIC
- 8-Lead PDIP

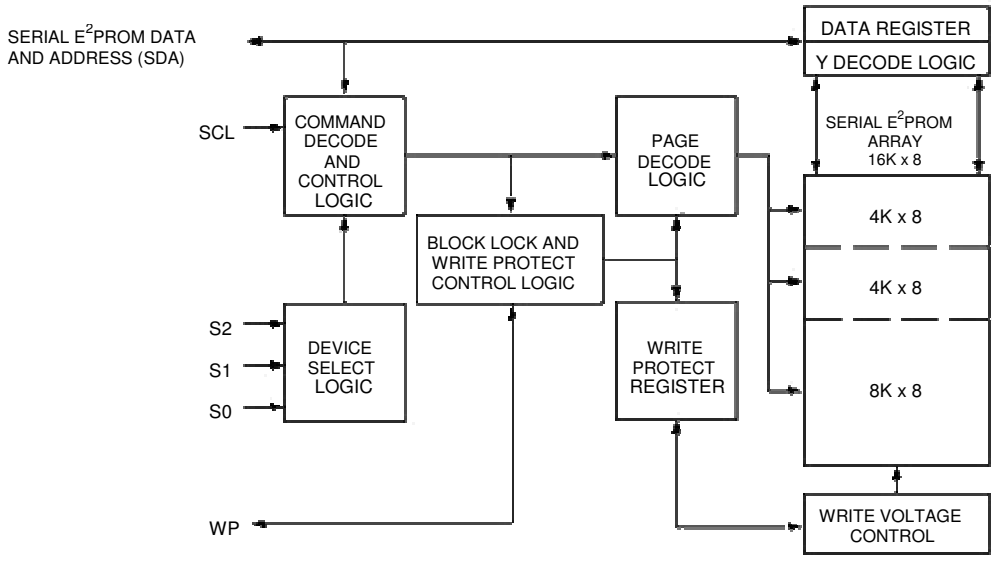
DESCRIPTION

The X24128 is a CMOS Serial E²PROM, internally organized 16K x 8. The device features a serial interface and software protocol allowing operation on a simple two wire bus.

Three device select inputs (S_0–S_2) allow up to eight devices to share a common two wire bus.

A Write Protect Register at the highest address location, FFFFh, provides three write protection features: Software Write Protect, Block Lock Protect, and Programmable Hardware Write Protect. The Software Write Protect feature prevents any nonvolatile writes to the device until the WEL bit in the Write Protect Register is set. The Block Lock Protection feature gives the user four array block protect options, set by programming two bits in the Write Protect Register. The Programmable Hardware Write Protect feature allows the user to install the device with WP tied to V_{CC}, write to and Block Lock the desired portions of the memory array in circuit, and then enable the In Circuit Programmable ROM Mode by programming the WPEN bit HIGH in the Write Protect Register. After this, the Block Locked portions of the array, including the Write Protect Register itself, are permanently protected from being erased.

FUNCTIONAL DIAGRAM



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Xicor E^2PROMs are designed and tested for applica- tions requiring extended endurance. Inherent data retention is greater than 100 years.

PIN DESCRIPTIONS

Serial Clock (SCL)

The SCL input is used to clock all data into and out of the device.

Serial Data (SDA)

SDA is a bidirectional pin used to transfer data into and out of the device. It is an open drain output and may be wire-ORed with any number of open drain or open collector outputs.

An open drain output requires the use of a pull-up resistor. For selecting typical values, refer to the Pull-up resistor selection graph at the end of this data sheet.

Device Select (S_0, S_1, S_2)

The device select inputs (S_0, S_1, S_2) are used to set the first three bits of the 8-bit slave address. This allows up to eight devices to share a common bus. These inputs can be static or actively driven. If used statically they must be tied to V_{SS} or V_{CC} as appropriate. If actively driven, they must be driven with CMOS levels (driven to V_{CC} or V_{SS}).

Write Protect (WP)

The Write Protect input controls the Hardware Write Protect feature. When held LOW, Hardware Write Protection is disabled. When this input is held HIGH, and the WPEN bit in the Write Protect Register is set HIGH, the Write Protect Register is protected, preventing changes to the Block Lock Protection and WPEN bits.

PIN NAMES

Symbol	Description
S_0, S_1, S_2	Device Select Inputs
SDA	Serial Data
SCL	Serial Clock
WP	Write Protect
V_{SS}	Ground
V_{CC}	Supply Voltage
NC	No Connect

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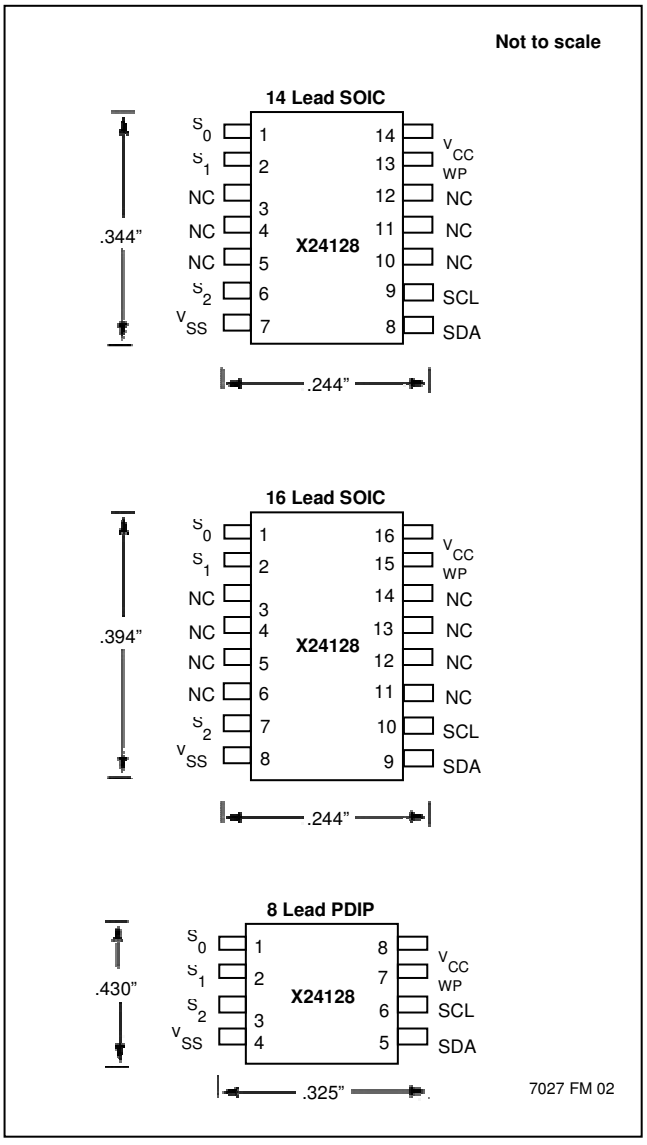
PIN CONFIGURATION



DEVICE OPERATION

The device supports a bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter, and the receiving device as the receiver. The device controlling the transfer is a master and the device being controlled is the slave. The master will always initiate data transfers, and provide the clock for both transmit and receive operations. Therefore, the device will be considered a slave in all applications.

Clock and Data Conventions

Data states on the SDA line can change only during SCL LOW. SDA state changes during SCL HIGH are reserved for indicating start and stop conditions. Refer to Figures 1 and 2.

Start Condition

All commands are preceded by the start condition, which is a HIGH to LOW transition of SDA when SCL is HIGH. The device continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met.

Figure 1. Data Validity

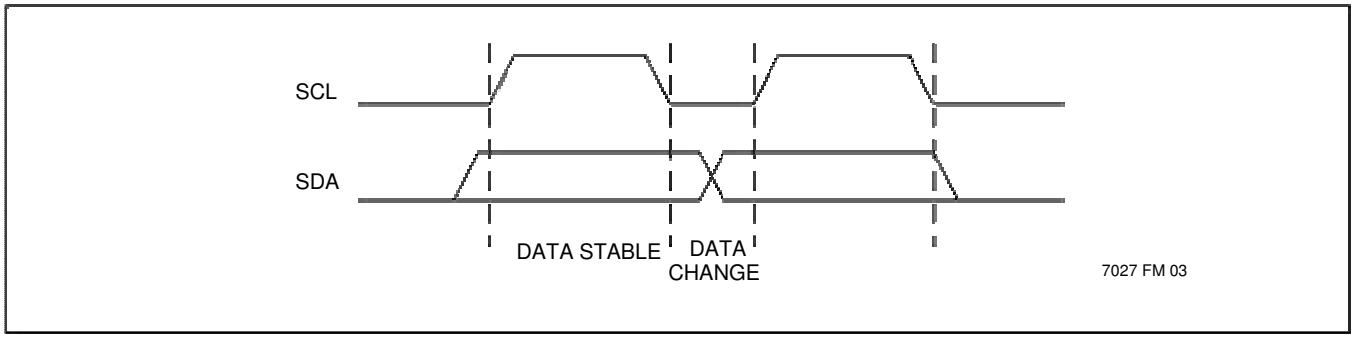
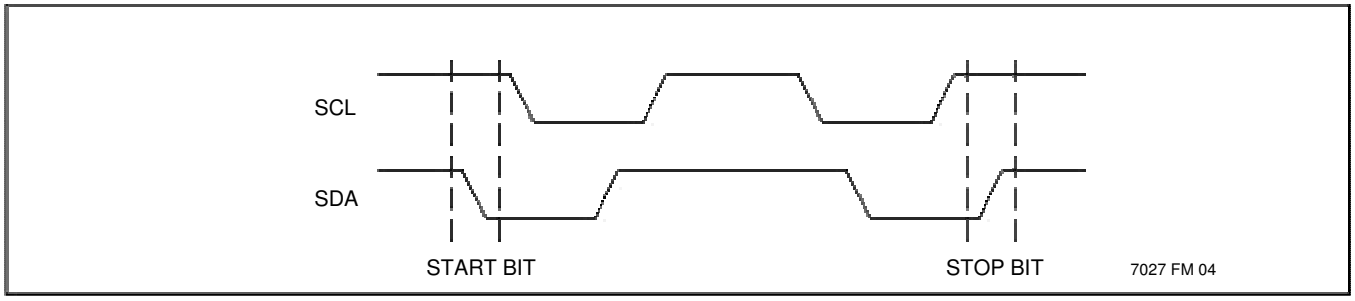


Figure 2. Definition of Start and Stop



Stop Condition

All communications must be terminated by a stop condition, which is a LOW to HIGH transition of SDA when SCL is HIGH. The stop condition is also used to place the device into the standby power mode after a read sequence. A stop condition can only be issued after the transmitting device has released the bus.

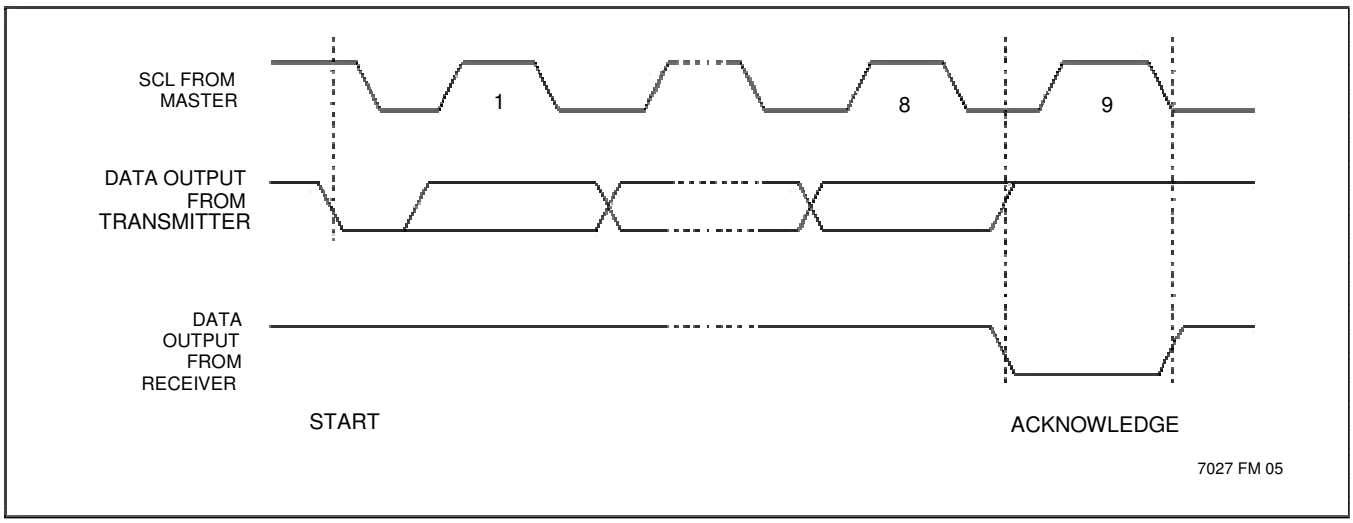
Acknowledge

Acknowledge is a software convention used to indicate successful data transfer. The transmitting device, either master or slave, will release the bus after transmitting eight bits. During the ninth clock cycle the receiver will pull the SDA line LOW to acknowledge that it received the eight bits of data. Refer to Figure 3.

The device will respond with an acknowledge after recognition of a start condition and its slave address. If both the device and a write operation have been selected, the device will respond with an acknowledge after the receipt of each subsequent 8-bit word.

In the read mode the device will transmit eight bits of data, release the SDA line and monitor the line for an acknowledge. If an acknowledge is detected and no stop condition is generated by the master, the device will continue to transmit data. If an acknowledge is not detected, the device will terminate further data transmissions. The master must then issue a stop condition to return the device to the standby power mode and place the device into a known state.

Figure 3. Acknowledge Response From Receiver



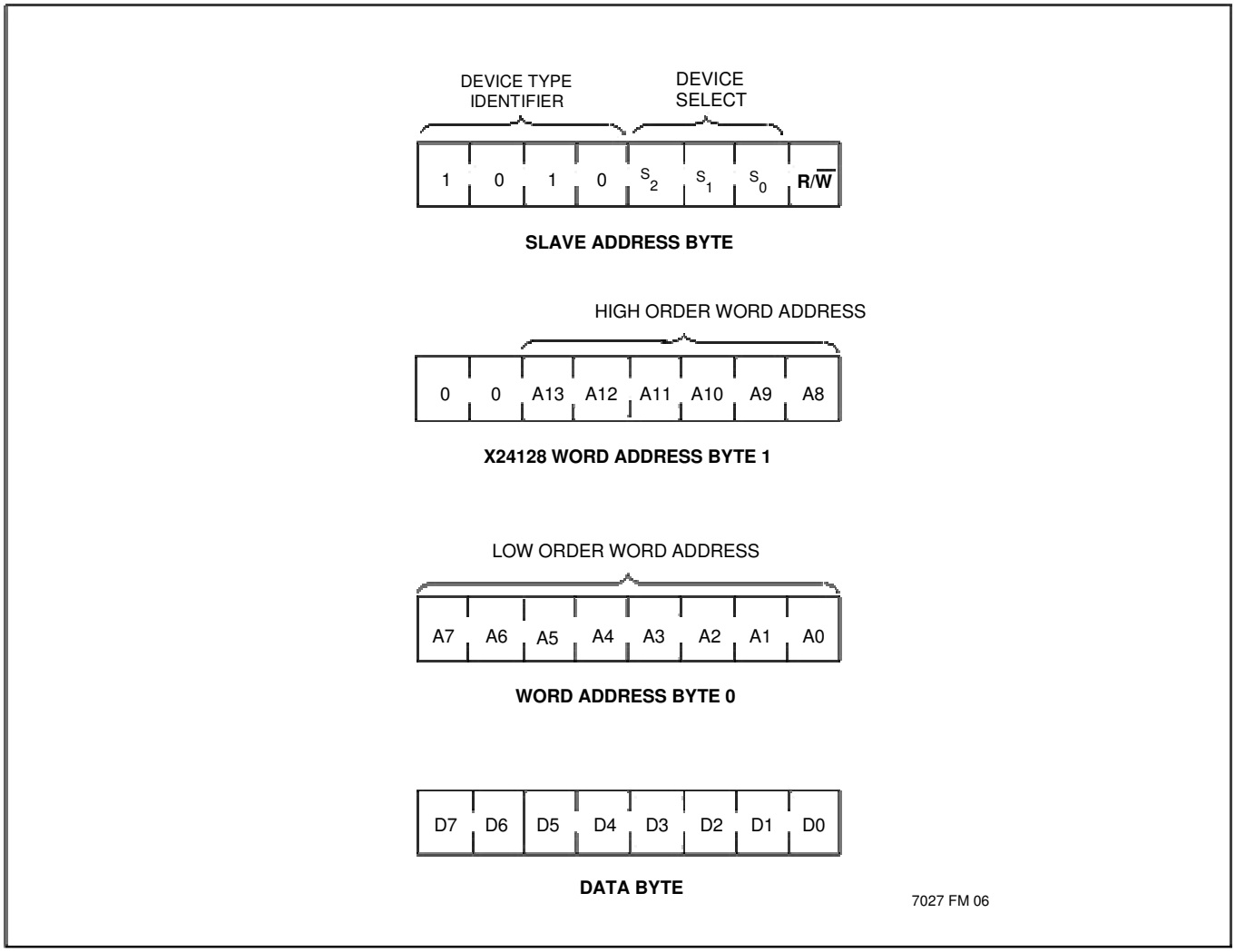
DEVICE ADDRESSING

Following a start condition, the master must output the address of the slave it is accessing. The first four bits of the Slave Address Byte are the device type identifier bits. These must equal "1010". The next 3 bits are the device select bits S_0, S_1, and S_2. This allows up to 8 devices to share a single bus. These bits are compared to the S_0, S_1, and S_2 device select input pins. The last bit of the Slave Address Byte defines the operation to be performed. When the R/W bit is a one, then a read operation is selected. When it is zero then a write operation is selected. Refer to figure 4. After loading the Slave Address Byte from the SDA bus, the device compares the device type bits with the value "1010" and the device select bits with the status of the device select input pins. If the compare is not successful, no acknowledge is output during the ninth clock cycle and the device returns to the standby mode.

The word address is either supplied by the master or obtained from an internal counter, depending on the operation. The master must supply the two Word Address Bytes as shown in figure 4.

The internal organization of the E^2 array is 512 pages by 32 bytes per page. The page address is partially contained in the Word Address Byte 1 and partially in bits 7 through 5 of the Word Address Byte 0. The byte address is contained in bits 4 through 0 of the Word Address Byte 0. See figure 4.

Figure 4. Device Addressing



WRITE OPERATIONS

Byte Write

For a write operation, the device requires the Slave Address Byte, the Word Address Byte 1, and the Word Address Byte 0, which gives the master access to any one of the words in the array. Upon receipt of the Word Address Byte 0, the device responds with an acknowledge, and waits for the first eight bits of data. After receiving the 8 bits of the data byte, the device again responds with an acknowledge. The master then terminates the transfer by generating a stop condition, at which time the device begins the internal write cycle to the nonvolatile memory. While the internal write cycle is in progress the device inputs are disabled and the device will not respond to any requests from the master. The SDA pin is at high impedance. See figure 5.

Page Write

The device is capable of a thirty-two byte page write operation. It is initiated in the same manner as the byte write operation; but instead of terminating the write operation after the first data word is transferred, the master can transmit up to thirty-one more words. The device will respond with an acknowledge after the receipt of each word, and then the byte address is internally incremented by one. The page address remains constant. When the counter reaches the end of the page, it "rolls over" and goes back to the first byte of the current page. This means that the master can write 32 words to the page beginning at any byte.

If the master begins writing at byte 16, and loads 32 words, then the first 16 words are written to bytes 16 through 31, and the last 16 words are written to bytes 0 through 15. Afterwards, the address counter would point to byte 16. If the master writes more than 32 words, then the previously loaded data is overwritten by the new data, one byte at a time.

The master terminates the data byte loading by issuing a stop condition, which causes the device to begin the nonvolatile write cycle. As with the byte write operation, all inputs are disabled until completion of the internal write cycle. Refer to figure 6 for the address, acknowledge, and data transfer sequence.

Figure 5. Byte Write Sequence

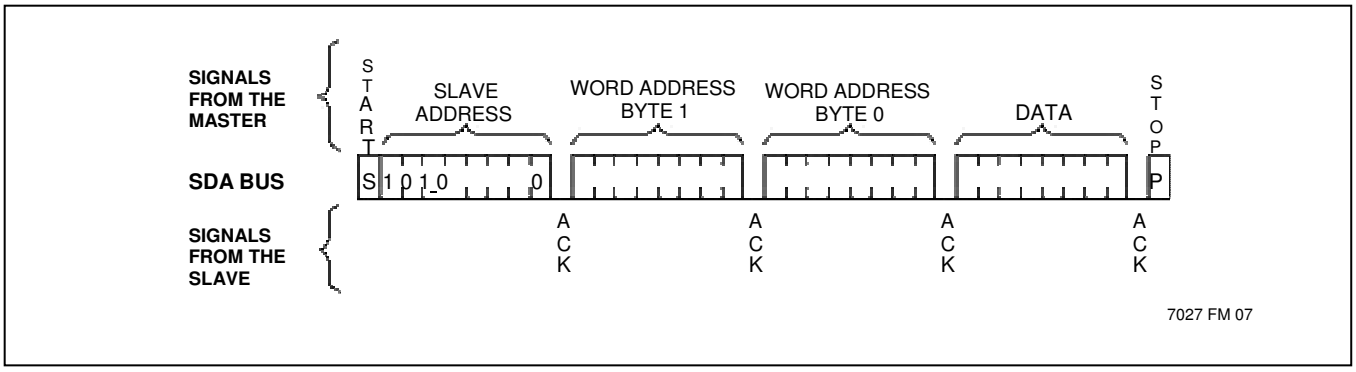
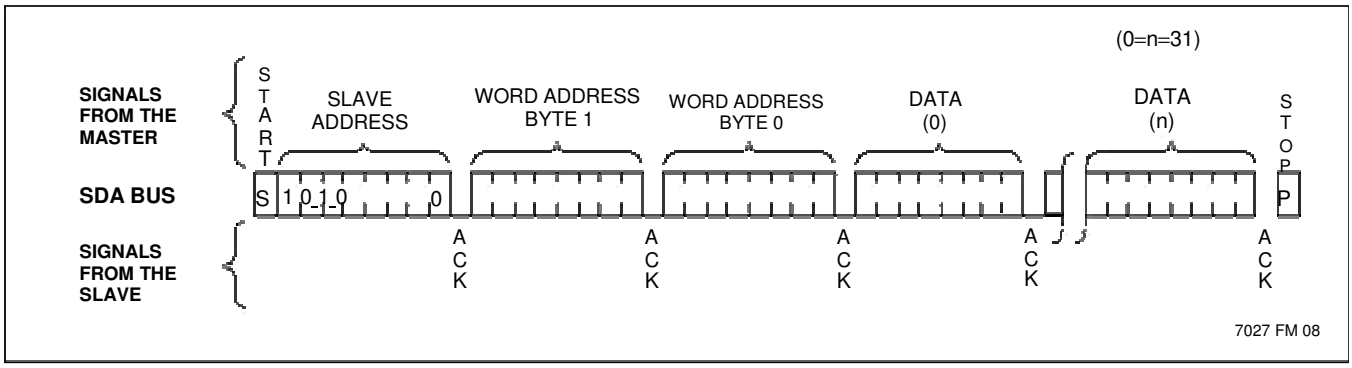


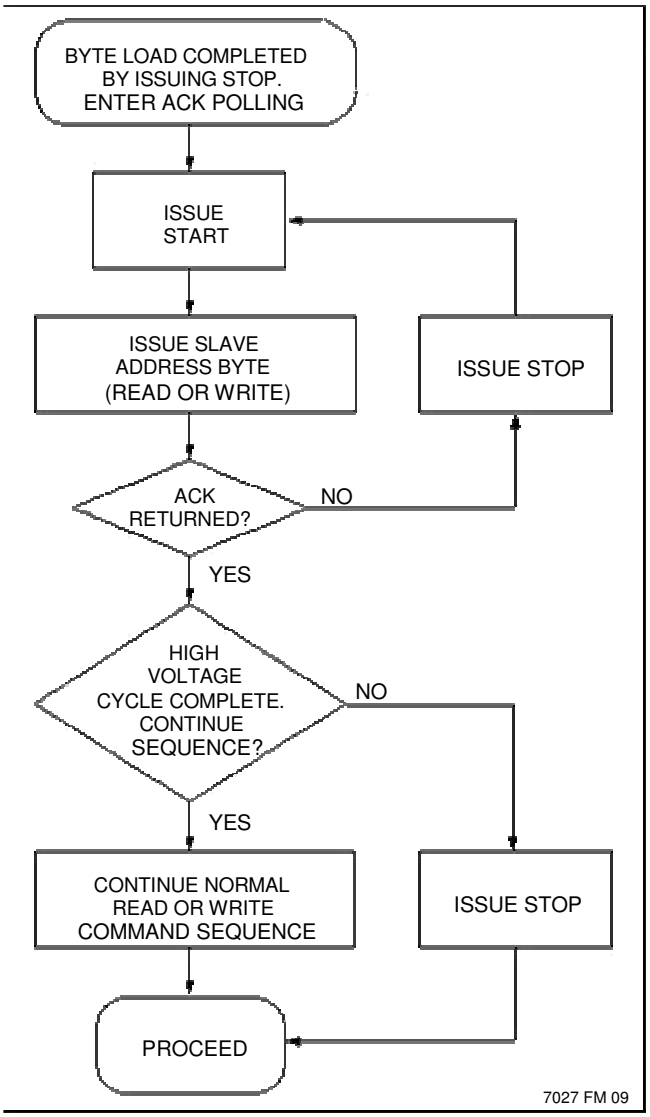
Figure 6. Page Write Sequence



Acknowledge Polling

The maximum write cycle time can be significantly reduced using Acknowledge Polling. To initiate Acknowledge Polling, the master issues a start condition followed by the Slave Address Byte for a write or read operation. If the device is still busy with the internal write cycle, then no ACK will be returned. If the device has completed the internal write operation, an ACK will be returned and the host can then proceed with the read or write operation. Refer to figure 7 .

Figure 7. Acknowledge Polling Sequence



READ OPERATIONS

Read operations are initiated in the same manner as write operations with the exception that the R/W bit of the Slave Address Byte is set to one. There are three basic read operations: Current Address Reads, Random Reads, and Sequential Reads.

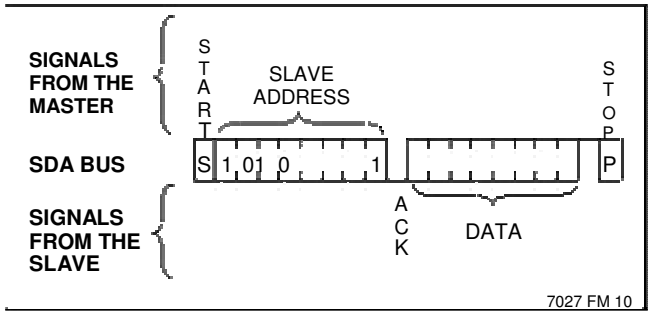
Current Address Read

Internally, the device contains an address counter that maintains the address of the last word read or written incremented by one. After a read operation from the last address in the array, the counter will "roll over" to the first address in the array. After a write operation to the last address in a given page, the counter will "roll over" to the first address on the same page.

Upon receipt of the Slave Address Byte with the R/W bit set to one, the device issues an acknowledge and then transmits the eight bits of the Data Byte. The master terminates the read operation when it does not respond with an acknowledge during the ninth clock and then issues a stop condition. Refer to figure 8 for the address, acknowledge, and data transfer sequence.

It should be noted that the ninth clock cycle of the read operation is not a "don't care." To terminate a read operation, the master must either issue a stop condition during the ninth cycle or hold SDA HIGH during the ninth clock cycle and then issue a stop condition.

Figure 8. Current Address Read Sequence



Random Read

Random read operation allows the master to access any memory location in the array. Prior to issuing the Slave Address Byte with the R/W bit set to one, the master must first perform a "Dummy" write operation. The master issues the start condition and the Slave Address Byte with the R/W bit low, receives an acknowledge, then issues the Word Address Byte 1, receives another acknowledge, then issues the Word Address Byte 0. After the device acknowledges receipt of the Word Address Byte 0, the master issues another start condition and the Slave Address Byte with the R/W bit set to one. This is followed by an acknowledge and then eight bits of data from the device. The master terminates the read operation by not responding with an acknowl- edge and then issuing a stop condition. Refer to figure 9 for the address, acknowledge, and data transfer sequence.

The device will perform a similar operation called "Set Current Address" if a stop is issued instead of the second start shown in figure 9. The device will go into standby mode after the stop and all bus activity will be ignored until a start is detected. The effect of this operation is that the new address is loaded into the address counter, but no data is output by the device.

The next Current Address Read operation will read from the newly loaded address.

Sequential Read

Sequential reads can be initiated as either a current address read or random read. The first Data Byte is transmitted as with the other modes; however, the master now responds with an acknowledge, indicating it requires additional data. The device continues to output data for each acknowledge received. The master terminates the read operation by not responding with an acknowledge and then issuing a stop condition.

The data output is sequential, with the data from address n followed by the data from address n + 1. The address counter for read operations increments through all byte addresses, allowing the entire memory contents to be read during one operation. At the end of the address space the counter "rolls over" to address 0000h and the device continues to output data for each acknowledge received. Refer to figure 10 for the acknowledge and data transfer sequence.

Figure 9. Random Read Sequence

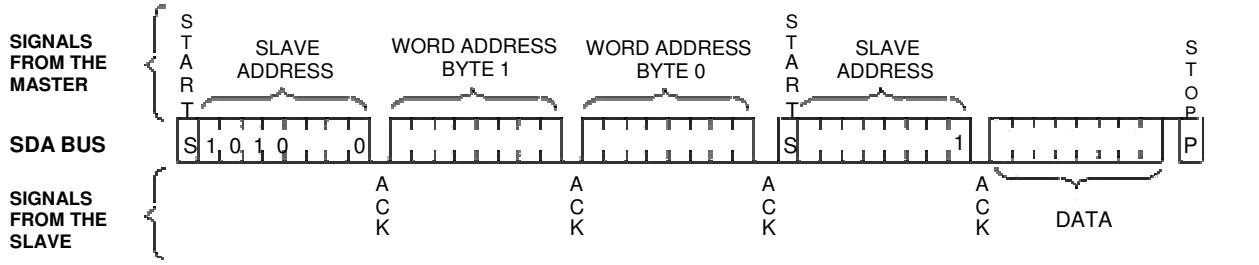
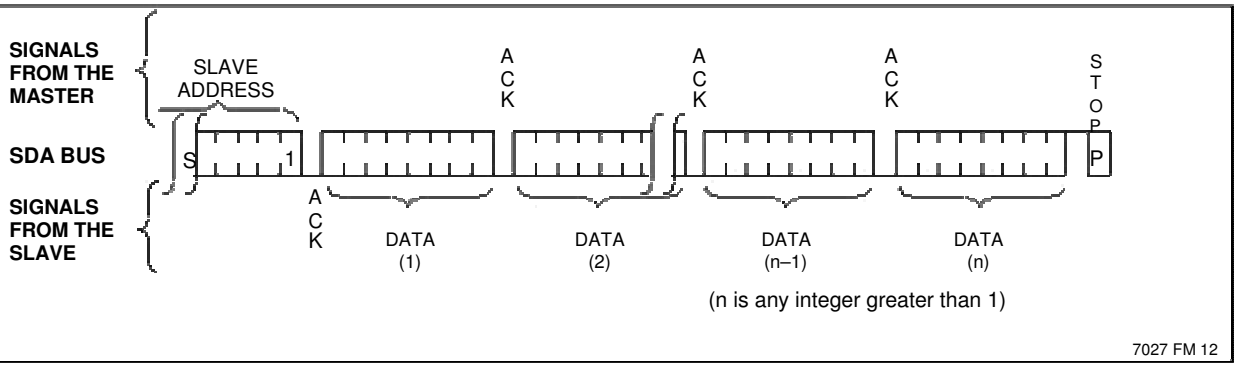


Figure 10. Sequential Read Sequence



WRITE PROTECT REGISTER (WPR)
Writing to the Write Protect Register

The Write Protect Register can only be modified by performing a "ByteWrite" operation directly to the address FFFFh as described below.

The Data Byte must contain zeroes where indicated in the procedural descriptions below; otherwise the operation will not be performed. Only one Data Byte is allowed for each register write operation. The part will not acknowledge any data bytes after the first byte is entered. The user then has to issue a stop to initiate the nonvolatile write cycle that writes BL0, BL1, and WPEN to the nonvolatile bits. A stop must also be issued after volatile register write operations to put the device into Standby.

The state of the Write Protect Register can be read by performing a random byte read at FFFFh at any time. The part will reset itself after the first byte is read. The master should supply a stop condition to be consistent with the protocol, but a stop is not required to end this operation. After the read, the address counter contains 0000h.

Write Protect Register: WPR (ADDR = $FFFF_h$)

7	6	5	4	3	2	1	0
WPEN	0	0	BL1	BL0	RWEL	WEL	0

WEL: Write Enable Latch (Volatile)
0 = Write Enable Latch reset, writes disabled.

1 = Write Enable Latch set, writes enabled.

RWEL: Register Write Enable Latch (Volatile)
0 = Register Write Enable Latch reset, writes to the Write Protect Register disabled.

1 = Register Write Enable Latch set, writes to the Write Protect Register enabled.

BL0, BL1: Block Lock Protect Bits (Nonvolatile) The Block Lock Protect Bits, BL0 and BL1, determine which blocks of the array are protected. A write to a protected block of memory is ignored, but will receive an acknowledge. The master must issue a stop to put the part into standby, just as it would for a valid write; but the stop will not initiate an internal nonvolatile write cycle. See figure 11.

WPEN: Write Protect Enable Bit (Nonvolatile)
The Write Protect (WP) pin and the Write Protect Enable (WPEN) bit in the Write Protect Register control the Programmable Hardware Write Protection feature. Hardware Write Protection is enabled when the WP pin is HIGH and the WPEN bit is HIGH, and disabled when either the WP pin is LOW or the WPEN bit is LOW. Figure 12 defines the write protect status for each combination of WPEN and WP. When the chip is Hardware Write Protected, nonvolatile writes are disabled to the Write Protect Register, including the Block Lock Protect bits and the WPEN bit itself, as well as to the Block Lock protected sections in the memory array. Only the sections of the memory array that are not Block Lock protected, and the volatile bits WEL and RWEL, can be written.

In Circuit Programmable ROM Mode
Note that when the WPEN bit is write protected, it cannot be changed back to a LOW state; so write protection is enabled as long as the WP pin is held HIGH. Thus an In Circuit Programmable ROM function can be implemented by hardwiring the WP pin to V_{CC}, writing to and Block Locking the desired portion of the array to be ROM, and then programming the WPEN bit HIGH.

Unused Bit Positions
Bits 0, 5 & 6 are not used. All writes to the WPR must have zeros in these bit positions. The data byte output during a WPR read will contain zeros in these bits.

Writing to the WEL and RWEL bits
WEL and RWEL are volatile latches that power up in the LOW (disabled) state. While the WEL bit is LOW, writes to any address other than FFFFh will be ignored (no acknowledge will be issued after the Data Byte).

The WEL bit is set by writing 00000010 to address FFFFh. Once set, WEL remains HIGH until either it is reset to 0 (by writing 00000000 to FFFFh) or until the part powers up again. Writes to WEL and RWEL do not cause a nonvolatile write cycle, so the device is ready for the next operation immediately after the stop condition.

The RWEL bit controls writes to the Block Lock Protect bits, BL0 and BL1, and the WPEN bit. If RWEL is 0 then no writes can be performed on BL0, BL1, or WPEN. RWEL is reset when the device powers up or after any nonvolatile write, including writes to the Block Lock Protect bits, WPEN bit, or any bytes in the memory array. When RWEL is set, WEL cannot be

reset, nor can RWEL and WEL be reset in one write operation. RWEL can be reset by writing 00000010 to FFFFh; but this is the same operation as in step 3 described below, and will result in programing BL0, BL1, and WPEN.

Writing to the BL and WPEN Bits

A 3 step sequence is required to change the nonvola- tile Block Lock Protect or Write Protect Enable bits:

1) Set WEL=1, Write 00000010 to address FFFFh (Volatile Write Cycle.)

2) Set RWEL=1, Write 00000110 to address FFFFh (Volatile Write Cycle.)

3) Set BL1, BL0, and/or WPEN bits, Write u00xy010 to address FFFFh, where u=WPEN, x=BL1, and y=BL0. (Nonvolatile Write Cycle.)

The three step sequence was created to make it diffi

previous register write operation, the user may start at step 2. RWEL is reset to zero in step 3 so that user is required to perform steps 2 and 3 to make another change. RWEL must be 0 in step 3. If the RWEL bit in the data byte for step 3 is a one, then no changes are made to the Write Protect Register and the device remains at step 2.

The WP pin must be LOW or the WPEN bit must be LOW before a nonvolatile register write operation is initiated. Otherwise, the write operation will abort and the device will go into standby mode after the master issues the stop condition in step 3.

Step 3 is a nonvolatile write operation, requiring t_{WC} to complete (acknowledge polling may be used to reduce this time requirement). It should be noted that step 3 MUST end with a stop condition. If a start condition is issued during or at the end of step 3 (instead of a stop condition) the device will abort the nonvolatile register write and remain at step 2. If the operation is aborted with a start condition, the master must issue a stop to put the device into standby mode.

Figure 11. Block Lock Protect Bits and Protected Addresses

BL1	BL0	Protected Addresses	Array Location
0	0	None	No Protect
0	1	3000h - 3FFFh	Upper 1/4
1	0	2000h - 3FFFh	Upper 1/2
1	1	0000h - 3FFFh	Full Array

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Figure 12. WP Pin and WPEN Bit Functionality

WP	WPEN	Memory Array Not Lock Block Protected	Memory Array Block Lock Protected	Block Lock Bits	WPEN Bit
0	X	Unprotected	Protected	Unprotected	Unprotected
X	0	Unprotected	Protected	Unprotected	Unprotected
1	1	Unprotected	Protected	Protected	Protected

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ABSOLUTE MAXIMUM RATINGS*

Temperature under Bias
X24128 .....–65°C to +135°C
Storage Temperature .....–65°C to +150°C
Voltage on any Pin with
Respect to V_{SS} .....–1V to +7V
D.C. Output Current 5mA
Lead Temperature
(Soldering, 10 seconds) .....300°C

***COMMENT**
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Temperature	Min.	Max.
Commercial	0°C	+70°C
Industrial	–40°C	+85°C

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Supply Voltage	Limits
X24128	4.5V to 5.5V
X24128–2.5	2.5V to 5.5V
X24128–1.8	1.8V to 3.6V

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D.C. OPERATING CHARACTERISTICS

Symbol	Parameter	Limits		Units	Test Conditions
		Min.	Max.		
I_{CC1}	V_{CC} Supply Current (Read)		1	mA	SCL = V_{CC} X 0.1/V_{CC} X 0.9 Levels @ 400KHz, SDA = Open, All Other Inputs = V_{SS} or V_{CC} – 0.3V
I_{CC2}	V_{CC} Supply Current (Write)		3	mA	
I_{SB1} (1)	V_{CC} Standby Current		5	∝A	SCL = SDA = V_{CC}, All Other Inputs = V_{SS} or V_{CC} – 0.3V, V_{CC} = 5V ± 10%
I_{SB2} (1)	V_{CC} Standby Current		1	∝A	SCL = SDA = V_{CC}, All Other Inputs = V_{SS} or V_{CC} – 0.3V, V_{CC} = 2.5V
I_{LI}	Input Leakage Current		10	∝A	V_{IN} = V_{SS} to V_{CC}
I_{LO}	Output Leakage Current		10	∝A	V_{OUT} = V_{SS} to V_{CC}
V_{IL} (2)	Input LOW Voltage	–0.5	V_{CC} x 0.3	V	
V_{IH} (2)	Input HIGH Voltage	V_{CC} x 0.7	V_{CC} + 0.5	V	
V_{OL}	Output LOW Voltage		0.4	V	I_{OL} = 3mA
V_{hys} (3)	Hysteresis of Schmitt Trigger Inputs	V_{CC} x 0.05		V	

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CAPACITANCE T_A = +25°C, f = 1MHz, V_{CC} = 5V

Symbol	Parameter	Max.	Units	Test Conditions
$C_{I/O}$ (3)	Input/Output Capacitance (SDA)	8	pF	$V_{I/O}$ = 0V
C_{IN} (3)	Input Capacitance (S_0, S_1, S_2, SCL, WP)	6	pF	V_{IN} = 0V

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Notes: (1)Must perform a stop command prior to measurement.
(2)V_{IL} min. and V_{IH} max. are for reference only and are not 100% tested.
(3)This parameter is periodically sampled and not 100% tested.

A.C. CONDITIONS OF TEST

Input Pulse Levels	V_{CC} x 0.1 to V_{CC} x 0.9
Input Rise and Fall Times	10ns
Input and Output Timing Levels	V_{CC} X 0.5

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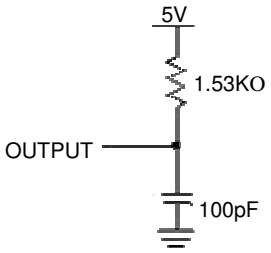
EQUIVALENT A.C. LOAD CIRCUIT



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A.C. OPERATING CHARACTERISTICS (Over the recommended operating conditions, unless otherwise specified.) **Read & Write Cycle Limits**

Symbol	Parameter	Min.	Max.	Units
f_{SCL}	SCL Clock Frequency	0	400	KHz
t_I	Noise Suppression Time Constant at SCL, SDA Inputs	50		ns
t_{AA}	SCL LOW to SDA Data Out Valid	0.1	0.9	∝s
t_{BUF}	Time the Bus Must Be Free Before a New Transmission Can Start	1.2		∝s
$t_{HD:STA}$	Start Condition Hold Time	0.6		∝s
t_{LOW}	Clock LOW Period	1.2		∝s
t_{HIGH}	Clock HIGH Period	0.6		∝s
$t_{SU:STA}$	Start Condition Setup Time (for a Repeated Start Condition)	0.6		∝s
$t_{HD:DAT}$	Data In Hold Time	0		∝s
$t_{SU:DAT}$	Data In Setup Time	100		ns
t_R	SDA and SCL Rise Time		300	ns
t_F	SDA and SCL Fall Time		300	ns
$t_{SU:STO}$	Stop Condition Setup Time	0.6		∝s
t_{DH}	Data Out Hold Time	50	300	ns
t_{OF}	Output Fall Time	$20+0.1C_b$ (5)	250	∝s

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POWER-UP TIMING(4)

Symbol	Parameter	Max.	Units
t_{PUR}	Power-up to Read Operation	1	ms
t_{PUW}	Power-up to Write Operation	5	ms

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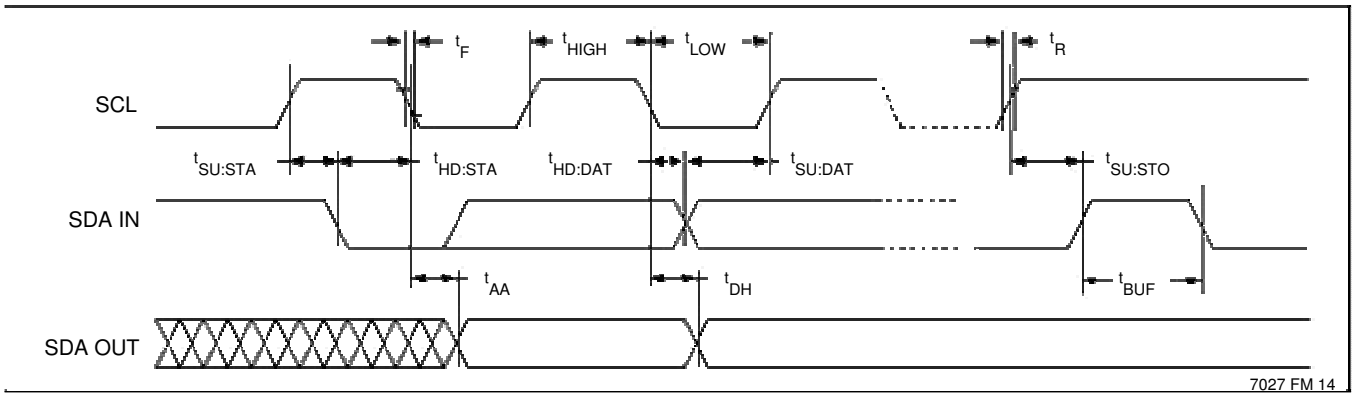
Notes: (4)t_{PUR} and t_{PUW} are the delays required from the time V_{CC} is stable until the specified operation can be initiated. These parameters are periodically sampled and not 100% tested.

(5)Typical values are for T_A = 25°C and nominal supply voltage (5V).

Bus Timing



Write Cycle Limits

Symbol	Parameter	Min.	Typ.(5)	Max.	Units
T_{WC}(6)	Write Cycle Time		5	10	ms

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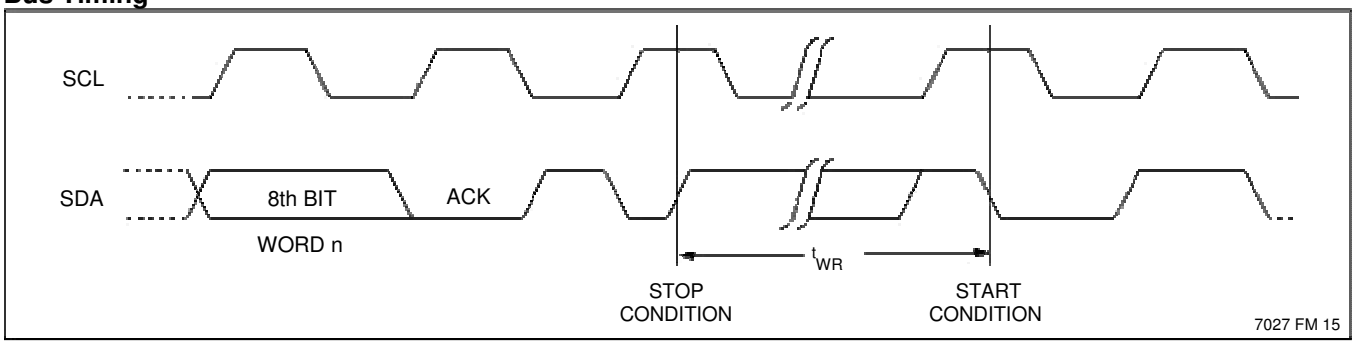
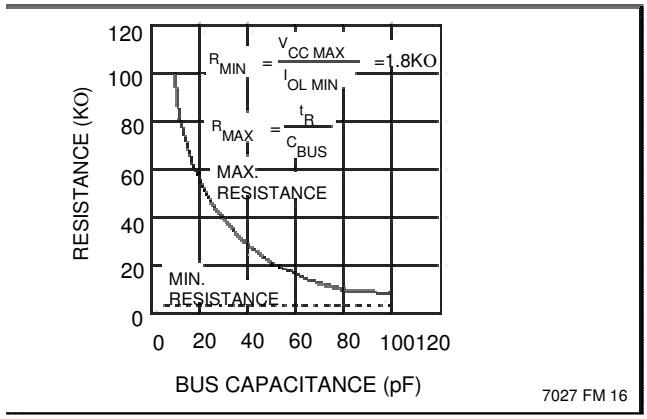
Notes: (5)Typical values are for T_A = 25°C and nominal supply voltage (5V).
(6)t_{WR} is the minimum cycle time to be allowed from the system perspective unless polling techniques are used. It is the maximum time the device requires to automatically complete the internal write operation.

The write cycle time is the time from a valid stop condition of a write sequence to the end of the internal erase/write cycle. During the write cycle, the X24128 bus interface circuits are disabled, SDA is allowed to remain HIGH, and the device does not respond to its slave address.

Bus Timing



Guidelines for Calculating Typical Values of Bus Pull-Up Resistors



SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from Low to High	Will change from Low to High
	May change from High to Low	Will change from High to Low
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

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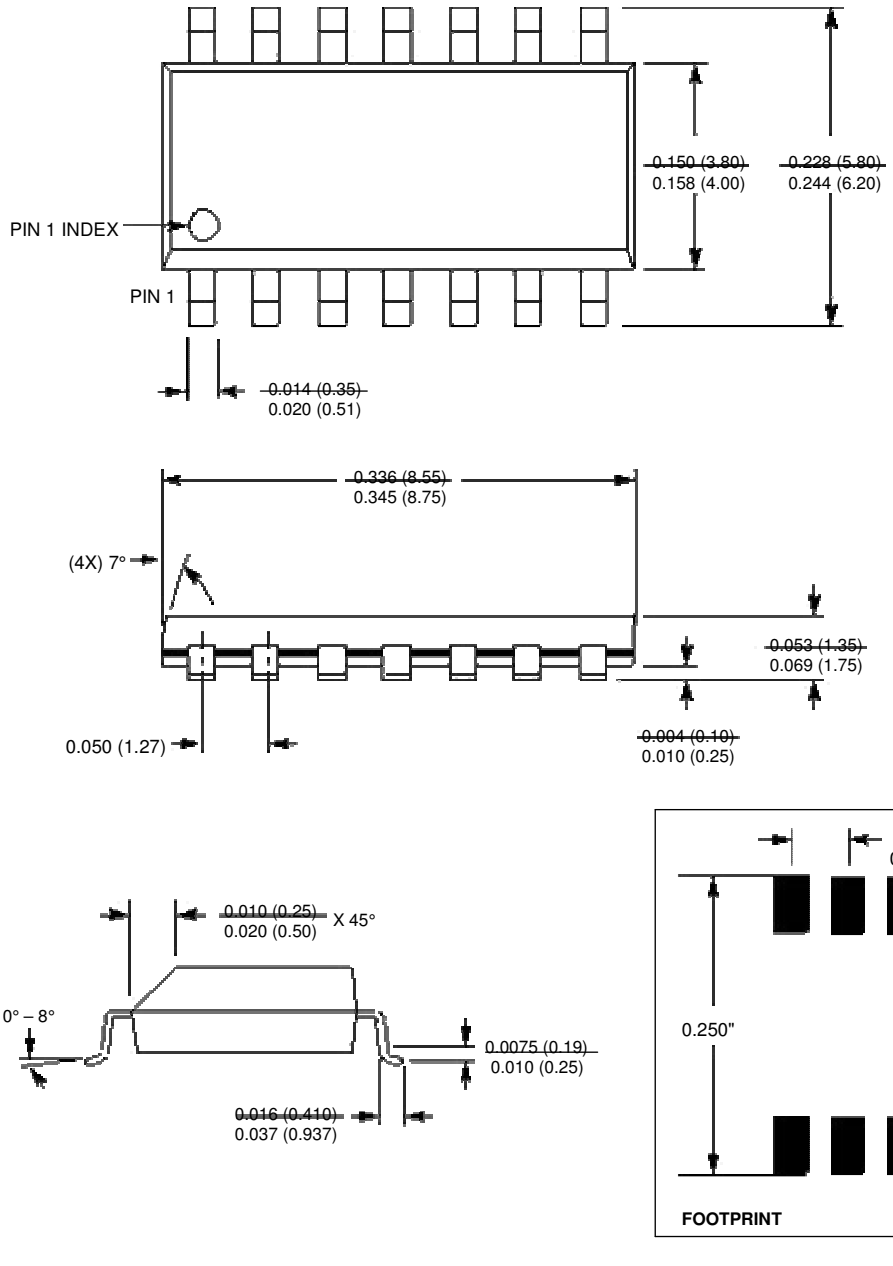
PACKAGING INFORMATION

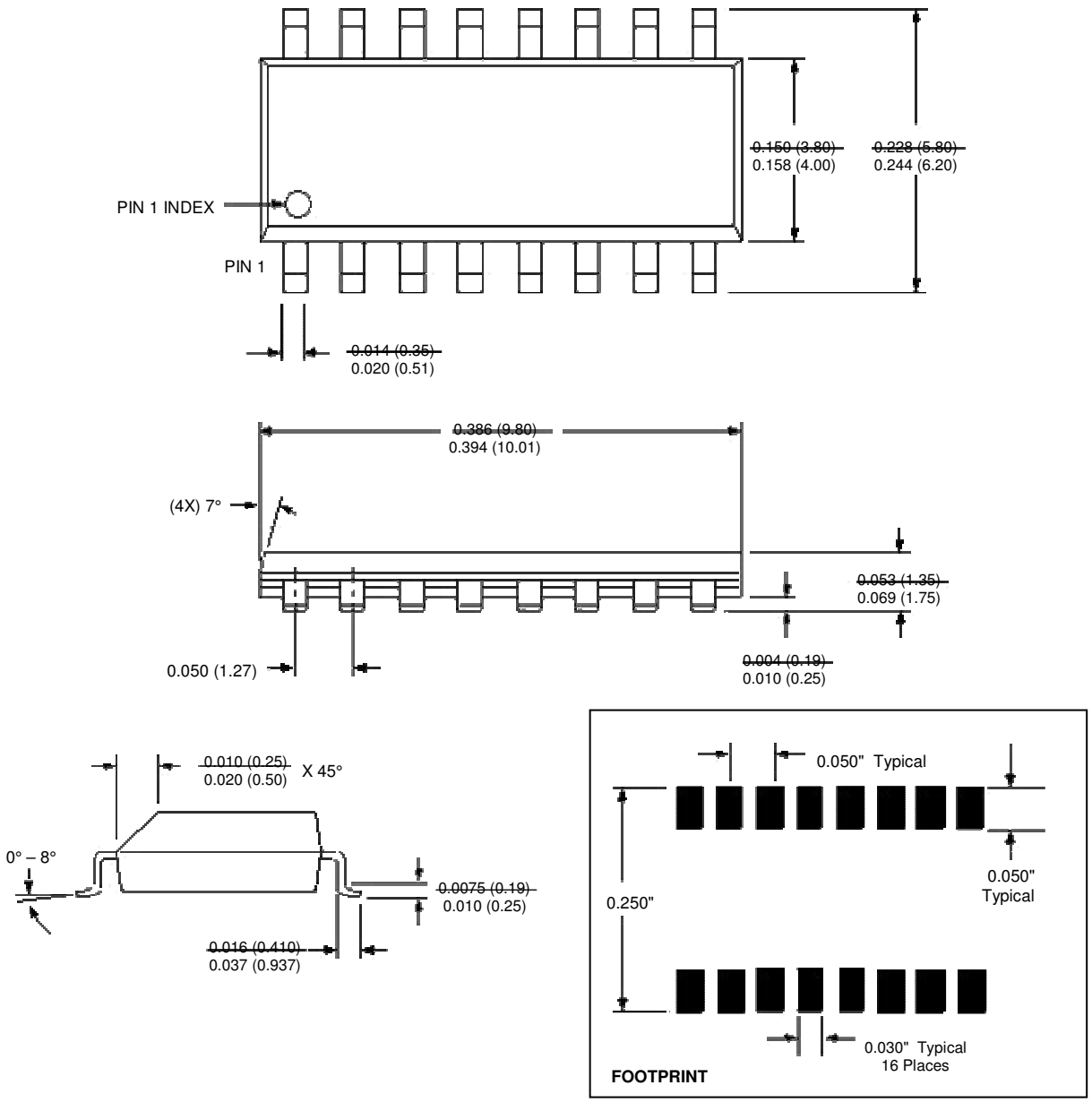
14-LEAD PLASTIC SMALL OUTLINE GULLWING PACKAGE TYPE S



NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

PACKAGING INFORMATION

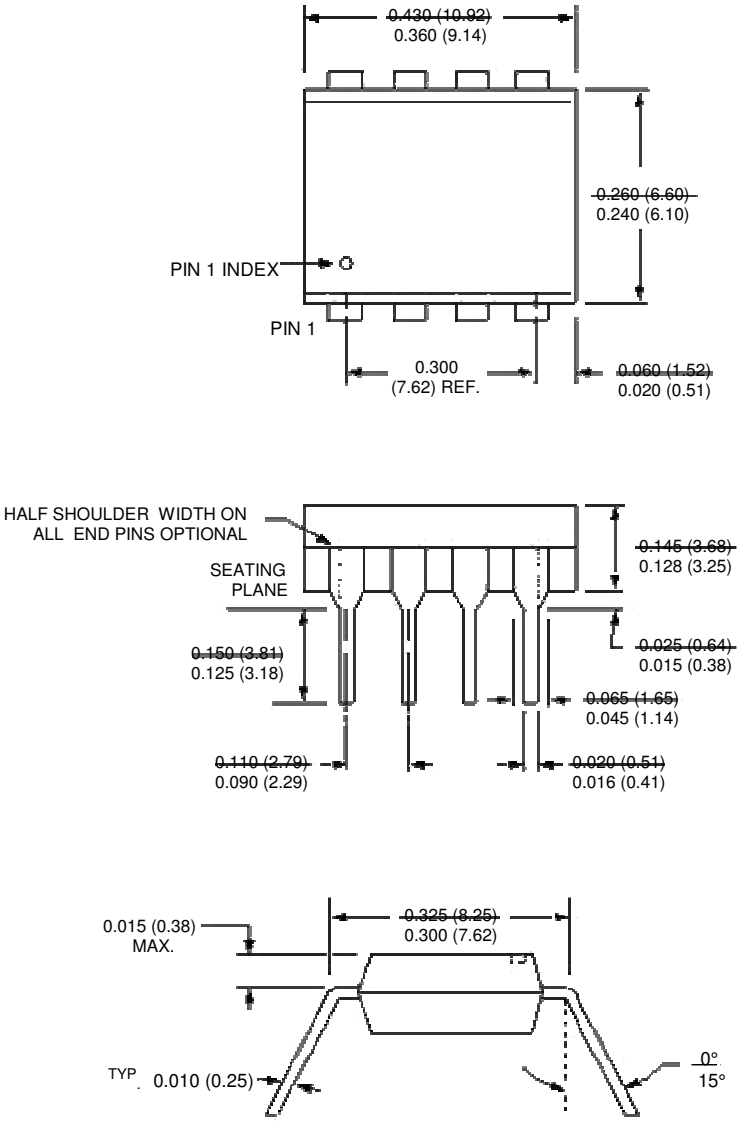
16-LEAD PLASTIC SMALL OUTLINE GULL WING PACKAGE TYPE S



NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

PACKAGING INFORMATION

8-LEAD PLASTIC DUAL IN-LINE PACKAGE TYPE P



NOTE:
1.ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS) 2. PACKAGE DIMENSIONS EXCLUDE MOLDING FLASH

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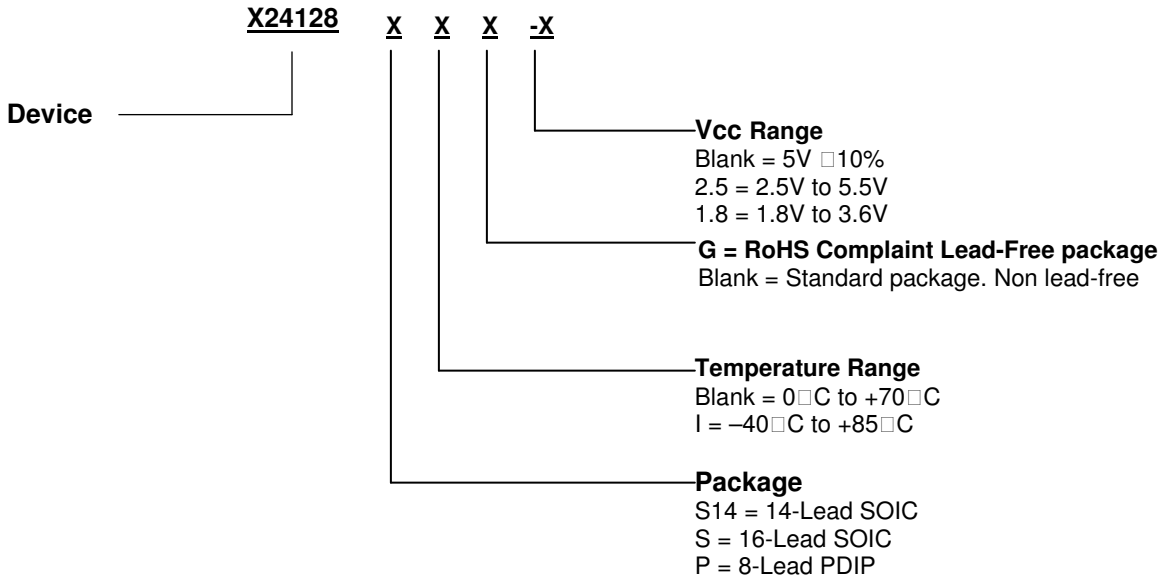
ORDERING INFORMATION



Part Mark Convention