First-in First-out (FIFO) 2048 x 9 CMOS Memory

FEATURES

- First-in, First-out dual port memory
  - 2048 x 9 organization
- Very high speed independent of depth/width
  - 20ns cycle times
- Asynchronous and simultaneous read and write
- Fully expandable by both word depth and/or width
- Low power consumption
  - Active: 150mA (max)
  - Power Down: 15mA (max)
- Half-full flag capability in standalone mode
- Empty and full warning flags
- Auto retransmit capability in standalone mode
- High performance 1.2 micron CMOS technology
- Available in 300 mil and 600 mil Plastic DIP and 32 pin PLCC

DESCRIPTION

The KM75C03A is dual port memory that implements a special First-In, First-Out algorithm that loads and empties data on a first-in, first-out basis. Full and empty flags are provided to prevent data overflow. Expansion logic allows unlimited expansion capability in both word size and depth without any loss in speed.

No address information is required for KM75C03A. Ring counters automatically generate the addresses required for every read and write operations. Data is toggled in and out of the device through the use of WRITE($\overline{W}$) and READ($\overline{R}$) pins. The device has a read/write cycle time of 20nsec (50MHz).

The device consists of a 9-bit wide array which is very useful in applications such as data communications where it is necessary to use parity bit. The RETRANSMIT ($\overline{RT}$) feature allows to re-read the previously read data. A half-full flag is available in the single device and width expansion modes.

The KM75C03A is fabricated using proprietary high speed CMOS 1.2 micron technology. It is designed for those applications requiring asynchronous and simultaneous read/writes in multiprocessing and rate buffer applications.

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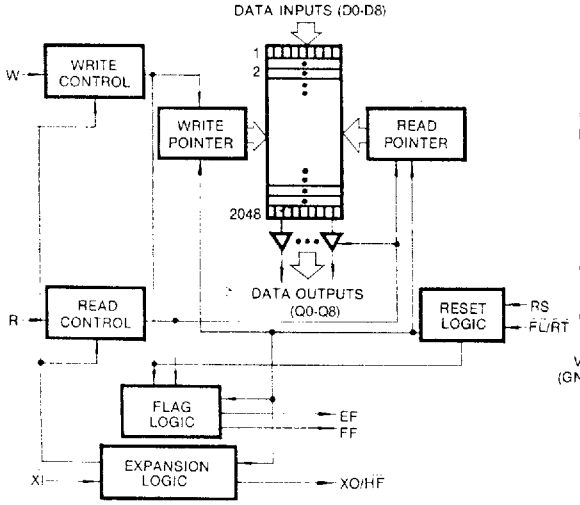
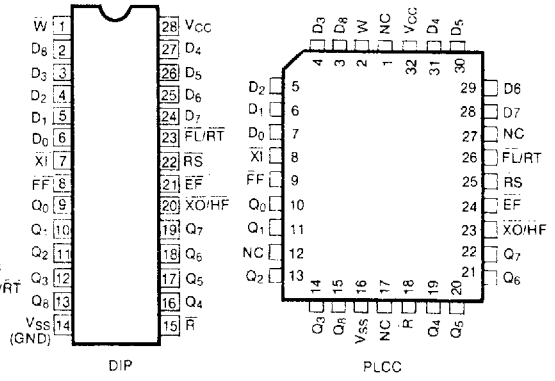
FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS (Top Views)



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ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage On Any Pin Relative to V_{SS}	V_{IN}	−0.5 to 7.0	V
Operating Temperature	T_A	0 to +70	°C
Temperature Under Bias	T_{bias}	−55 to +125	°C
Storage Temperature	T_{stg}	−65 to 150	°C
Power Dissipation	P_D	1.0	W
DC Output Current	I_{OUT}	50	mA

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may effect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, $T_A = 0$ to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.0			V
Input Low Voltage	V_{IL}			0.8	V

DC AND OPERATING CHARACTERISTICS ($V_{CC} = 5V \pm 10\%$)

Parameter	Symbol	T_A = 15/20ns			T_A = 25ns			Unit
		Min	Typ	Max	Min	Typ	Max	
V_{CC} Active Current	I_{CC}			150			120	mA
V_{CC} Standby Current-TTL[1] ($\overline{R} = \overline{W} = \overline{RS} = \overline{FL}/\overline{RT} = V_{IH}$)	I_{SB1}			15			15	mA
V_{CC} Standby Current-CMOS[1] (all inputs = V_{CC}-0.2V)	I_{SB2}			5			5	mA
Input Leakage Current[2]	I_{LI}	−1		1	−1		1	μA
Output Leakage Current[3]	I_{LO}	−10		10	−10		10	μA
Output High Voltage Level (I_{OH} = −2mA)	V_{OH}	2.4			2.4			V
Output Low Voltage Level (I_{OL} = 8mA)	V_{OL}			0.4			0.4	V

DC AND OPERATING CHARACTERISTICS ($V_{CC} = 5V \pm 10\%$)

Parameter	Symbol	T_A = 35ns			T_A = 50ns			Unit
		Min	Typ	Max	Min	Typ	Max	
V_{CC} Active Current	I_{CC}			100			60	mA
V_{CC} Standby Current-TTL[1] ($\overline{R} = \overline{W} = \overline{RS} = \overline{FL}/\overline{RT} = V_{IH}$)	I_{SB1}			15			15	mA
V_{CC} Standby Current-CMOS[1] (all inputs = V_{CC}-0.2V)	I_{SB2}			5			5	mA
Input Leakage Current[2]	I_{LI}	−1		1	−1		1	μA
Output Leakage Current[3]	I_{LO}	−10		10	−10		10	μA
Output High Voltage Level (I_{OH} = −2mA)	V_{OH}	2.4			2.4			V
Output Low Voltage Level (I_{OL} = 8mA)	V_{OL}			0.4			0.4	V

Notes: 1. I_{CC} and I_{SB} measurements are made with outputs open.
2. Measurements with $V_{SS} \leq V_{IN} \leq V_{CC}$.
3. $\overline{R} \geq V_{IH}$, $V_{SS} \leq V_{OUT} \leq V_{CC}$.

AC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10%, T_A=0°C to + 70°C)

Parameter	Symbol	KM75C03A-12		KM75C03A-15		KM75C03A-20		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	20		25		30		ns
Access Time	t_A		12		15		20	ns
Read Recovery Time	t_{RR}	8		10		10		ns
Read Pulse Width(2)	t_{RPW}	12		15		20		ns
Data Valid from Read Pulse High	t_{DV}	5		5		5		ns
Read Pulse High to Data Bus at High-Z(3)	t_{RHZ}		15		15		15	ns
Write Cycle Time	t_{WC}	20		25		30		ns
Write Pulse Width(2)	t_{WPW}	12		15		20		ns
Write Recovery Time	t_{WR}	8		10		10		ns
Data Setup Time	t_{DS}	8		10		12		ns
Data Hold Time	t_{DH}	0		0		0		ns
Reset Cycle Time	t_{RSC}	20		25		30		ns
Reset Pulse Width(2)	t_{RS}	12		15		20		ns
Reset Recovery Time	t_{RSR}	8		10		10		ns
Retransmit Cycle Time	t_{RTC}	25		25		30		ns
Retransmit Pulse Width(2)	t_{RT}	15		15		20		ns
Retransmit Recovery Time	t_{RTR}	10		10		10		ns
Reset to Empty Flag Low	t_{EFL}		20		25		30	ns
Reset to Half & Full Flag High	t_{HFH}, t_{FFH}		20		25		30	ns
Read Low to Empty Flag High	t_{REF}		20		20		20	ns
Read High to Full Flag High	t_{RFF}		20		20		20	ns
Write High to Empty Flag High	t_{WEF}		20		20		20	ns
Write Low to Full Flag Low	t_{WFF}		20		20		20	ns
Write Low to Half-Full Flag Low	t_{WHF}				25		30	ns
Read High to Half-Full Flag High	t_{RHF}				25		30	ns
Expansion Out Low Delay from Clock	t_{XOL}		16		20		20	ns
Expansion Out High Delay from Clock	t_{XOH}(4)		16		20		20	ns
$\overline{XI}$ Pulse Width	t_{PXI}	12		15		20		ns
$\overline{XI}$ Recovery Time	t_{XIR}	8		10		10		ns
$\overline{XI}$ Set-Up to Write or Clock	t_{XIS}	8		10		12		ns

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AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, T_A = 0°C to +70°C)

Parameter	Symbol	KM75C03A-25		KM75C03A-35		Unit
		Min	Max	Min	Max	
Read Cycle Time	t_{RC}	35		45		ns
Access Time	t_A		25		35	ns
Read Recovery Time	t_{RR}	10		10		ns
Read Pulse Width[2]	t_{RPW}	25		35		ns
Data Valid from Read Pulse High	t_{DV}	5		5		ns
Read Pulse High to Data Bus at High-Z[1]	t_{RHZ}		20		20	ns
Write Cycle Time	t_{WC}	35		45		ns
Write Pulse Width[2]	t_{WPW}	25		35		ns
Write Recovery Time	t_{WR}	10		10		ns
Data Setup Time	t_{DS}	15		18		ns
Data Hold Time	t_{DH}	0		0		ns
Reset Cycle Time	t_{RSC}	35		45		ns
Reset Pulse Width[2]	t_{RS}	25		35		ns
Reset Recovery Time	t_{RSR}	10		10		ns
Retransmit Cycle Time	t_{RTC}	35		45		ns
Retransmit Pulse Width[2]	t_{RT}	25		35		ns
Retransmit Recovery Time	t_{RTR}	10		10		ns
Reset to Empty Flag Low	t_{EFL}		35		45	ns
Reset to Half & Full Flag High	t_{HFH}, t_{FFH}		35		45	ns
Read Low to Empty Flag High	t_{REF}		25		30	ns
Read High to Full Flag High	t_{RFF}		25		30	ns
Write High to Empty Flag High	t_{WEF}		25		30	ns
Write Low to Full Flag Low	t_{WFF}		25		30	ns
Write Low to Half-Full Flag Low	t_{WHF}		35		45	ns
Read High to Half-Full Flag High	t_{RHF}		35		45	ns
Expansion Out Low Delay from Clock	t_{XOL}		25		35	ns
Expansion Out High Delay from Clock	t_{XOH}[4]		25		35	ns
$\overline{XI}$ Pulse Width	t_{PXI}	25		35		ns
$\overline{XI}$ Recovery Time	t_{XIR}	10		10		ns
$\overline{XI}$ Set-Up to Write or Clock	t_{XIS}	15		15		ns

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, T_A = 0°C to +70°C)

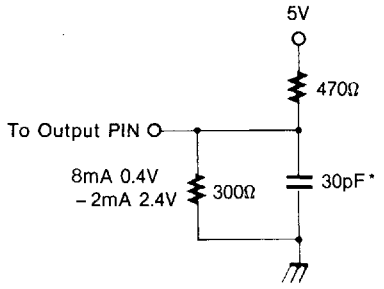
Parameter	Symbol	KM75C03A-50		KM75C03A-80		Unit
		Min	Max	Min	Max	
Read Cycle Time	t_{RC}	65		100		ns
Access Time	t_A		50		80	ns
Read Recovery Time	t_{RR}	15		20		ns
Read Pulse Width[2]	t_{RPW}	50		80		ns
Data Valid from Read Pulse High	t_{DV}	5		5		ns
Read Pulse High to Data Bus at High-Z[3]	t_{RHZ}		30		30	ns
Write Cycle Time	t_{WC}	65		100		ns
Write Pulse Width[2]	t_{WPW}	50		80		ns
Write Recovery Time	t_{WR}	15		20		ns
Data Setup Time	t_{DS}	30		40		ns
Data Hold Time	t_{DH}	5		10		ns
Reset Cycle Time	t_{RSC}	65		100		ns
Reset Pulse Width[2]	t_{RS}	50		80		ns
Reset Recovery Time	t_{RSR}	15		20		ns
Retransmit Cycle Time	t_{RTC}	65		100		ns
Retransmit Pulse Width[2]	t_{RT}	50		80		ns
Retransmit Recovery Time	t_{RTR}	15		20		ns
Reset to Empty Flag Low	t_{EFL}		65		100	ns
Reset to Half & Full Flag High	t_{HFH}, t_{FFH}		65		100	ns
Read Low to Empty Flag High	t_{REF}		45		60	ns
Read High to Full Flag High	t_{RFF}		45		60	ns
Write High to Empty Flag High	t_{WEF}		45		60	ns
Write Low to Full Flag Low	t_{WFF}		45		60	ns
Write Low to Half-Full Flag Low	t_{WHF}		65		100	ns
Read High to Half-Full Flag High	t_{RHF}		65		100	ns
Expansion Out Low Delay from Clock	t_{XOL}		50		80	ns
Expansion Out High Delay from Clock	t_{XOH}[4]		50		65	ns
$\overline{XI}$ Pulse Width	t_{PXI}	50		80		ns
$\overline{XI}$ Recovery Time	t_{XIR}	15		20		ns
$\overline{XI}$ Set-Up to Write or Clock	t_{XIS}	15		15		ns

Notes: 1. Timings referenced as in AC Test Conditions
2. Pulse widths less than minimum value are not allowed.
3. Values guaranteed by design, not currently tested
4. t_{XOH} is guaranteed to be greater than or equal to t_{XOL} under all conditions.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1

Figure 1. Output Load



* INCLUDES JIG AND SCOPE CAPACITANCES

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter	Conditions	Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	7	pF

Note: This parameter is sampled and not 100% tested.

Note: Generation $\overline{R}/\overline{W}$ Signals-When using these high-speed FIFO devices, it is necessary to have clean inputs on the $\overline{R}$ and $\overline{W}$ signals. It is important not to have glitches, spikes or ringing on the $\overline{R}$, $\overline{W}$ (that violate the V_{IL}, V_{IH} requirements); although the minimum pulse width low for the $\overline{R}$ and $\overline{W}$ are specified in tens of nanosecond, a glitch of 3ns can affect the read or write pointer and cause it to increment.

Master Reset ($\overline{RS}$)

Reset is accomplished whenever the MASTER RESET ($\overline{RS}$) input is taken to a low state. During this operation, both the internal read and the internal write pointers are set to the first FIFO location. A Master Reset pulse is required to initialize the FIFO after power-up before any write operation is performed. Both $\overline{R}$ and $\overline{W}$ inputs must be inactive for t_{RPW} or t_{WPW} before the rising edge of $\overline{RS}$, and should not change for t_{RSR} after the rising edge of $\overline{RS}$. Half-Full Flag ($\overline{HF}$) will be set to inactive (high) level after master reset ($\overline{RS}$).

Read Enable ($\overline{R}$)

READ cycles are initiated on the falling edge of the READ ENABLE ($\overline{R}$) input provided that EMPTY-FLAG ($\overline{EF}$) is not low. Read Cycles may be initiated asynchronously to any write operation in progress. After READ ENABLE ($\overline{R}$) goes high, the data outputs will return to a high impedance condition until the next READ operation. If the FIFO is empty, the EMPTY-FLAG ($\overline{EF}$) will go low and prevent any further read cycles. The data outputs will enter the high-impedance state after completion of the last read cycle.

Write Enable ($\overline{W}$)

WRITE cycles may be initiated by a low signal at the $\overline{W}$ input provided the FULL-FLAG ($\overline{FF}$) is not set. Data is stored in the memory array sequentially independent of any read operation that may be in progress.

When more than half of the memory bytes have been filled, the HALF-FULL ($\overline{HF}$) Flag output will be set low and will remain low till the difference between the write pointer and read pointer is less than or equal to one half of the total memory bytes of the device. The HALF-FULL flag is then reset by the rising edge of the read operation.

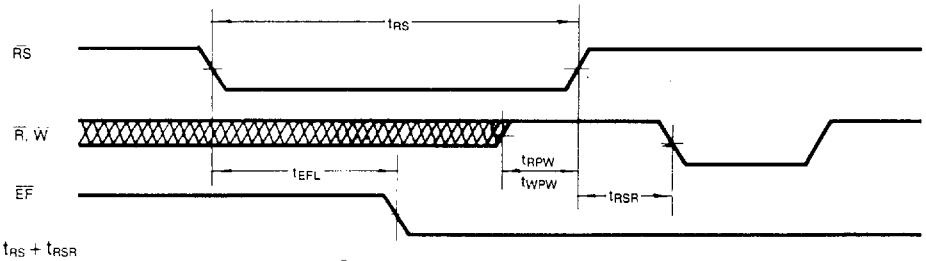
When the memory array is completely full, i.e., when the write pointer is one location from the read pointer, the FULL-FLAG ($\overline{FF}$) will go low preventing any further write operations. The FULL-FLAG will go high again t_{RFF} after completion of a valid read operation.

First Load/Retransmit ($\overline{FL}/\overline{RT}$)

This input may be used in two different ways depending upon the configuration of EXPANSION-IN ($\overline{XI}$):

1. Single Device or Retransmit Mode: In this mode the $\overline{XI}$ pin must be grounded. Using this mode the device can be used to retransmit data when $\overline{RT}$ is pulsed low. A retransmit operation will set the internal read pointer

Figure 2. Reset



Notes

1. $t_{RSC} = t_{RS} + t_{RSR}$
2. W and $\overline{R} = V_{IH}$ around the rising edge of $\overline{RS}$.

to the first memory location in the array. The write pointer is unaffected. Both write enable and read enable must be inactive during the retransmit operation. This feature is particularly useful for FIFO applications in communications buffers where noise levels may be high and transmission errors are frequently detected. The retransmit feature may not be used along with depth expansion.

2. Depth Expansion Mode: In this mode the ($\overline{FL}/\overline{RT}$) pin is grounded it that device is the first of the "daisy chain." The $\overline{FL}$ pin is kept high if it is further down the chain. For details of Depth Expansion see Operating Modes.

Expansion-In ($\overline{XI}$)

This is a dual purpose input pin. As explained above, $\overline{XI}$ is grounded to indicate single device mode operation. EXPANSION IN ($\overline{XI}$) is connected to EXPANSION OUT ($\overline{XO}$) of the previous device of the "daisy chain" in the Depth Expansion mode.

Full-Flag ($\overline{FF}$)

The FULL-FLAG output goes low inhibiting further write operations when the write pointer is one memory location from the read pointer i.e., the memory array is full. The total length of he memory array is 2048 bytes write operations for the KM75C03A.

Expansion Out/Half-Full Flag ($\overline{XO}/\overline{HF}$)

This output may be used in two different ways:

Single Device Mode: In this mode this output acts as a HALF-FULL Flag. After half the memory locations are full, and at the falling edge of the next write operation, the $\overline{HF}$ output is set to low. It is reset to high if the difference between the write pointer and the read pointer is half the memory depth or less at the rising edge of the read operation.

Depth Expansion Mode: In this mode EXPANSION IN ($\overline{XI}$) is connected to EXPANSION OUT ($\overline{XO}$) of the previous device of the "daisy chain." In this way a signal can be passed onto the next device when the current device reaches the last memory location.

FIFO's can also be expanded simultaneously in depth and width to provide word widths greater than 9 in increments of 9. Consequently, any depth or width FIFO can be created. When expanding in depth, a composite $\overline{FF}$ must be created by OR-ing the $\overline{FF}$s together. Likewise, a composite $\overline{EF}$ is created by OR-ing the $\overline{EF}$'s together. $\overline{HF}$ and $\overline{RT}$ functions are available in Depth Expansion Mode.

Single Device/Width Expansion Mode: Single Device and Width Expansion Modes are entered by grounding $\overline{XI}$ during a MR cycle. During these modes the $\overline{HF}$ and $\overline{RT}$ features are available. FIFO's can be expanded in width to provide word widths greater than 9 in increments of 9. During Width Expansion Mode all control line inputs are common to all devices and flag outputs from any device can be monitored.

Figure 3. Asynchronous Write and Read Operation

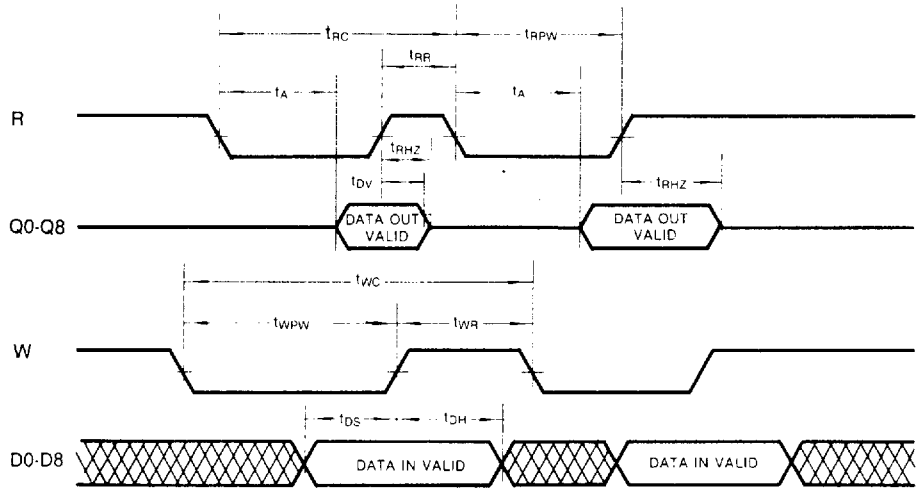


Figure 4. Full Flag From Last Write to First Read

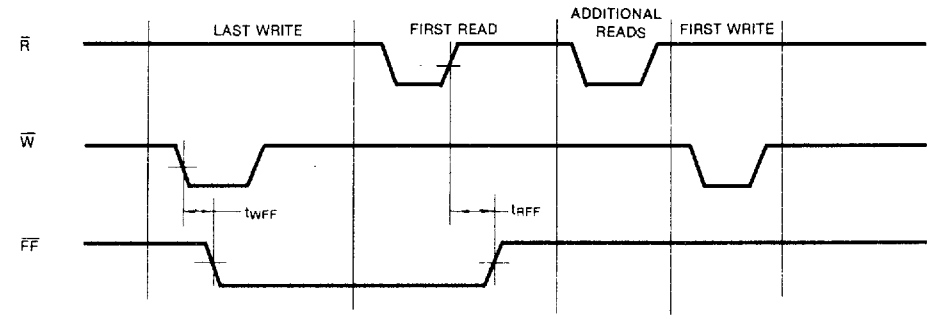


Figure 5. Empty Flag From Last Read to First Write

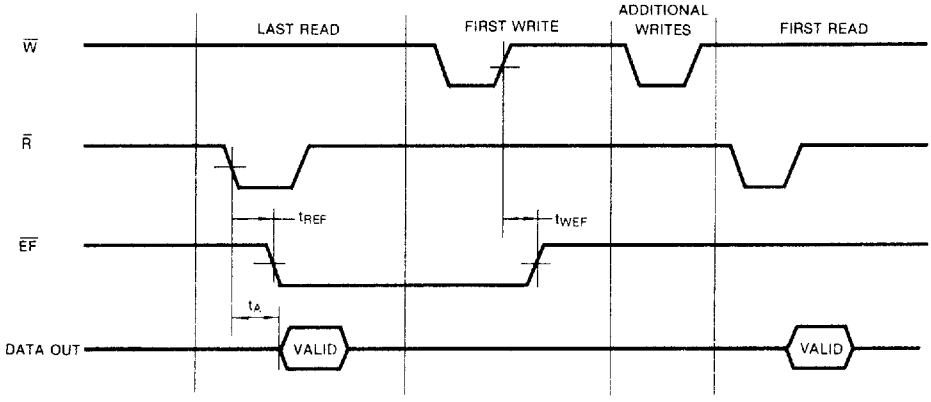
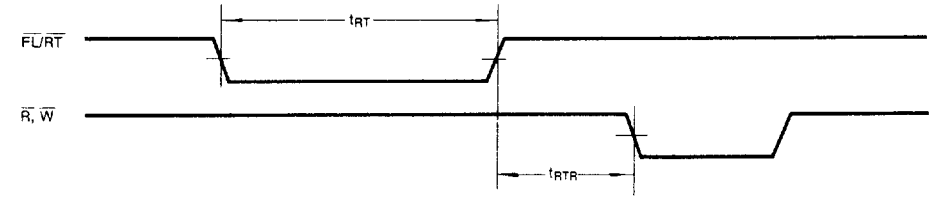


Figure 6. Retransmit



Notes:

1. $t_{RTC} = t_{RT} + t_{RTR}$
2. $\overline{EF}$, $\overline{HF}$, and $\overline{FF}$ may change state during retransmit as a result of the offset of the read and write pointers, but flags will be valid at t_{RTC}.

Figure 7. Expansion-In Timing Diagram

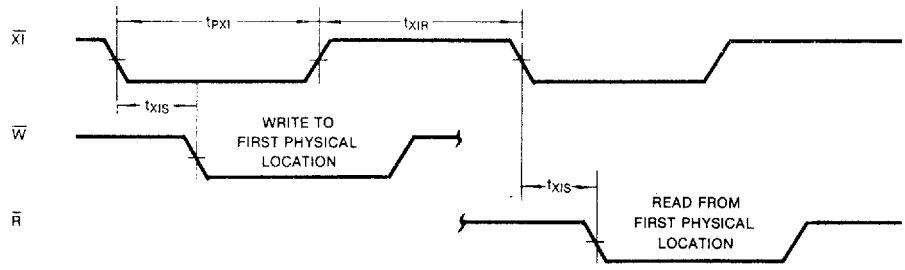


Figure 8. Expansion-Out Timing Diagram

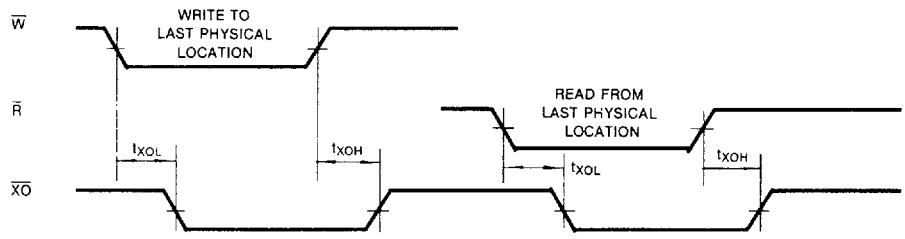
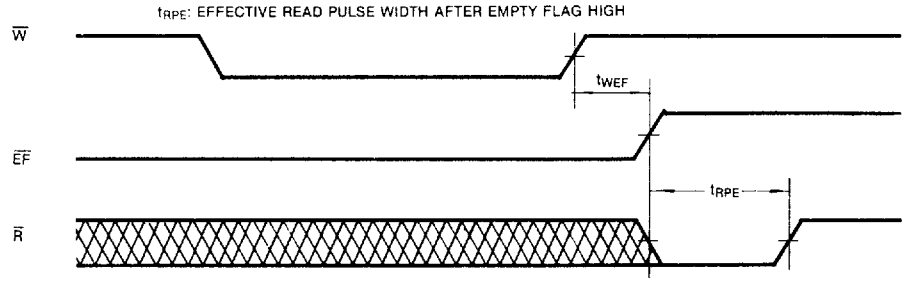


Figure 9. Empty Flag Timing



Note: 1. ($t_{RPE} = t_{RPW}$)

Figure 10. Full Flag Timing

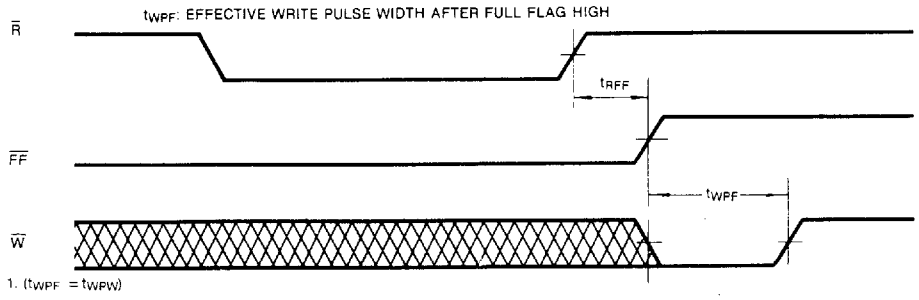
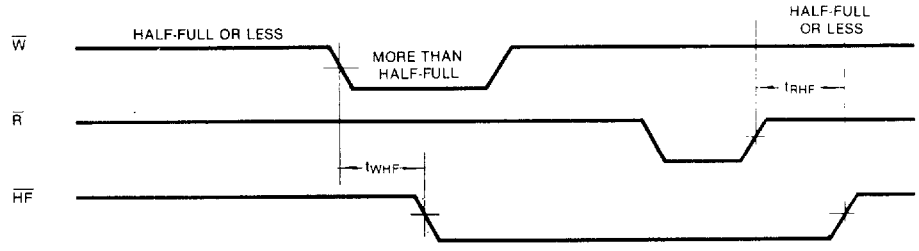


Figure 11. Half Full Flag Timing



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OPERATING MODES

Single Device Mode

A single KM75C03A may be used when the application requirements are for 2048 words or less. the device is placed in a Single Device Configuration when the EXPANSION IN (XI) control input is grounded (See Figure 12). In this mode the HALF-FULL FLAG (HF) and RETRANSMIT (RT) features are available.

Figure 12. Block Diagram of Single 2048 x 9 FIFO

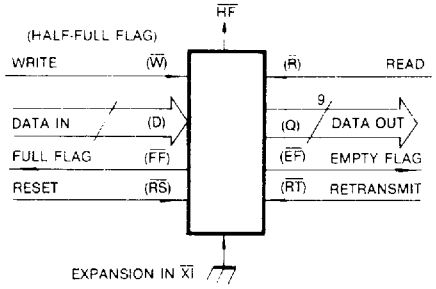
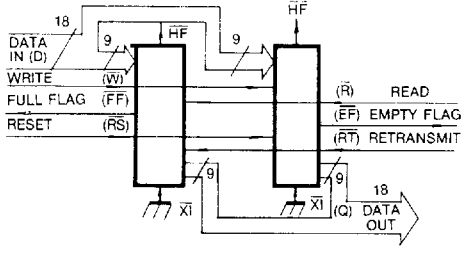


Figure 13. Block Diagram of 2048 x 18 FIFO Memory Used in Width Expansion Mode



Notes: Flag detection is accomplished by monitoring the $\overline{FF}$, $\overline{EF}$, and $\overline{HF}$ signals on either (any) device used in the width expansion configuration. Do not connect any output control signals together.

Width Expansion Mode

Word width may be increased simply by connecting the corresponding input control signals of multiple devices. Status flags ($\overline{EF}$, $\overline{FF}$ and $\overline{HF}$) can be detected from any one device. Figure 13 demonstrates an 18-bit word width by using two KM75C03A.

Depth Expansion (Daisy Chain) Mode

The KM75C03A can easily be adapted to applications when the requirements are for greater than words. Figure 14 demonstrates Depth Expansion using three KM75C03A. Any depth can be attained by adding additional KM75C03A's. The KM75C03A operates in the Depth Expansion configuration when the following conditions are met:

1. The first device must be designed by grounding the FIRST LOAD ($\overline{FL}$) control input. The RETRANSMIT feature is not available in this mode.
2. All other devices must have $\overline{FL}$ in the high state.
3. The EXPANSION OUT ($\overline{XO}$) pin of each device must be tied to the EXPANSION IN ($\overline{XI}$) pin of the next device. The half-full flag ($\overline{HF}$) function is not available in this mode.
4. External logic is needed to generate a composite FULL FLAG ($\overline{FF}$) and EMPTY FLAG ($\overline{EF}$). This requires the OR-ing of all $\overline{EF}$s and OR-ing of all $\overline{FF}$s (i.e., all must be set to generate the correct composite $\overline{FF}$ or $\overline{EF}$).

Compound Expansion Mode

The two expansion techniques described above can be applied together in a straightforward manner to achieve large FIFO arrays (See Figure 15).

Bidirection Mode

Applications which required data buffering between two systems (each system capable of READ and WRITE operations), can be achieved by pairing KM75C03A as shown in Figure 16. Care must be taken to assure that the appropriate flag is monitored by each system; (i.e., $\overline{FF}$ is monitored on the device where $\overline{W}$ is used; $\overline{EF}$ is monitored on the device where $\overline{R}$ is used). Both Depth Expansion and Width Expansion may be used in this mode.

Data Flow-Through Modes

This section describes two special conditions—when the FIFO is full or empty. For the read flow-through mode (Figure 17), the FIFO permits a reading of a single word after writing one word of data into an empty FIFO. The data is enabled on the bus in ($t_{WEF} + t_A$) ns after the rising edge of $\overline{W}$, called the first write edge, and it remains on the bus until the $\overline{R}$ line is raised from low-to-high, after which the bus would go into a tri-state mode after t_{RHZ} ns. The $\overline{EF}$ line would have a pulse showing temporary de-assertion and then would be asserted. In the interval of time that $\overline{R}$ was low, more words can be written to the FIFO (the subsequent writes after the first write edge would deassert the emptly flag); however, the same word (written the first write edge), presented to the output bus as the read pointer, would not be incremented when $\overline{R}$ is low. On toggling $\overline{R}$, the other words that were written to the FIFO will appear on the output bus as in the read cycle timings.

In the write flow-through mode (Figure 18), the FIFO permits the writing of a single word of data immediately after reading one word of data (from a full FIFO. The $\overline{R}$ line causes the $\overline{FF}$ to be de-asserted but the $\overline{W}$ line being low causes it to be asserted again in anticipation of a new data word. On the rising edge of $\overline{W}$, the new word is loaded in the FIFO. The $\overline{W}$ line must be toggled when $\overline{FF}$ is not asserted to write new data in the FIFO and to increment the write pointer.

TRUTH TABLES

Table 1. Reset and Retransmit-Single Device Configuration/Width Expansion Mode

Mode	Inputs			Internal Status		Outputs		
	$\overline{RS}$	$\overline{FL}/\overline{RT}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$	$\overline{HF}$
Reset	0	X	0	Location Zero	Location Zero	0	1	1
Retransmit	1	0	0	Location Zero	Unchanged	X	X	X
Read/Write	1	1	0	Increment (1)	Increment (1)	X	X	X

Note: 1. Pointer will increment if flag is high

Table 2. Reset and First Load Truth Table-Depth Expansion/Compound Expansion Mode

Mode	Inputs			Internal Status		Outputs	
	$\overline{RS}$	$\overline{FL}/\overline{RT}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{HF}$
Reset	0	0	(1)	Location Zero	Location Zero	0	1
Retransmit	0	1	(1)	Location Zero	Location Zero	0	1
Read/Write	1	X	(1)	X	X	X	X

Note: 1. $\overline{XI}$ is connected to $\overline{XO}$ of previous device. See Figure 14.
$\overline{RS}$ = Reset Input, $\overline{FL}/\overline{RT}$ = First Load/Retransmit, $\overline{EF}$ = Empty Flag Output, $\overline{FF}$ = Full Flag Output,
$\overline{XI}$ = Expansion Input, $\overline{HF}$ = Half-Full Flag Output.

Figure 14. Block Diagram of 1536 x 9 FIFO Memory (Depth Expansion)

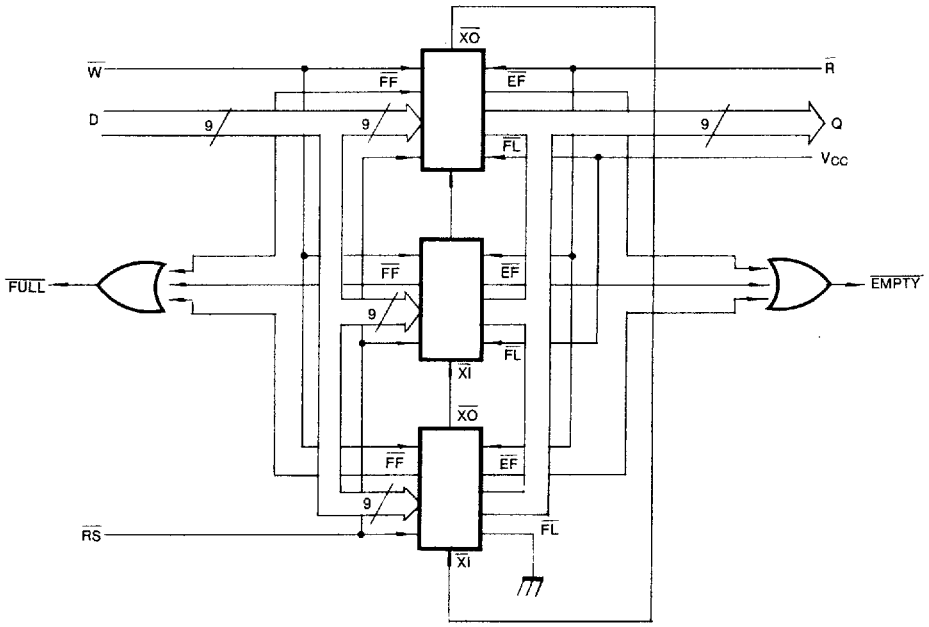


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Figure 15. Compound FIFO Expansion

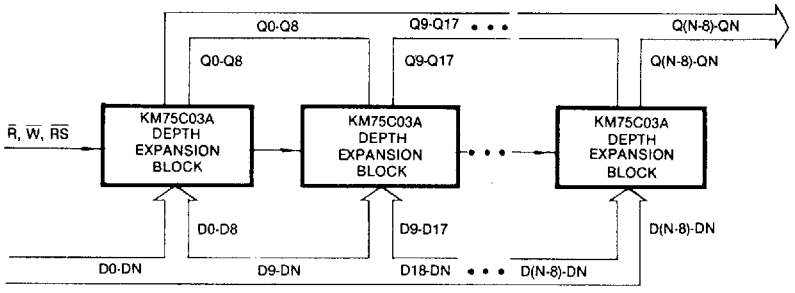
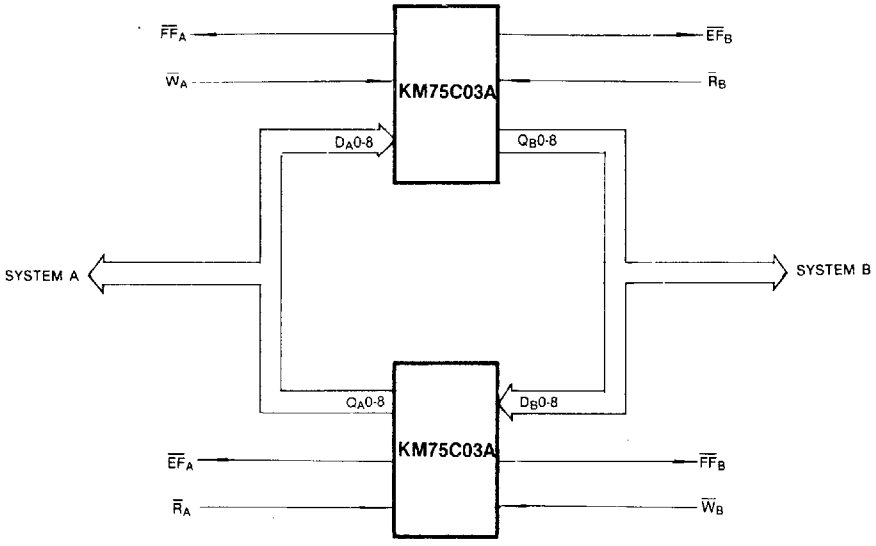
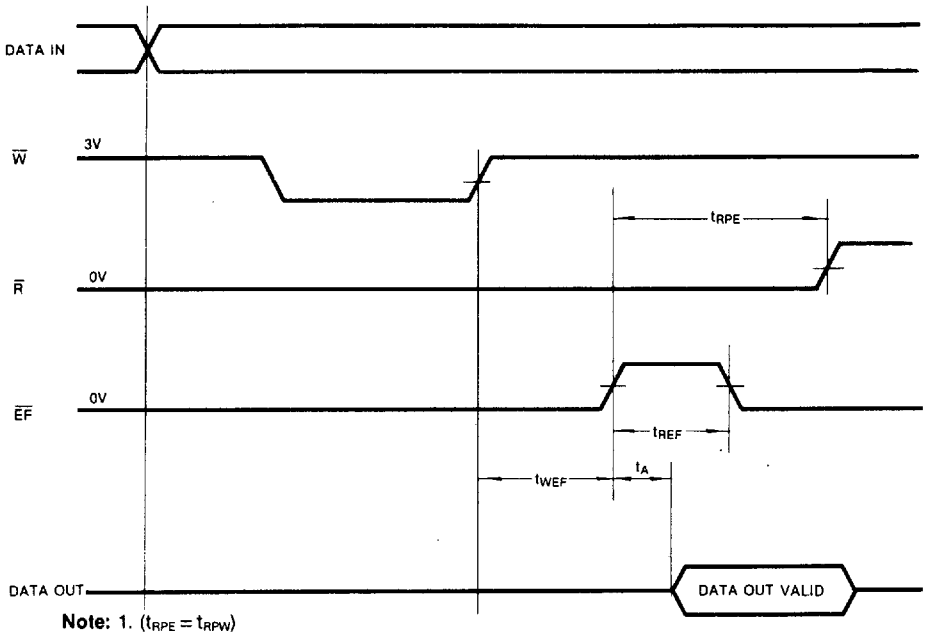


Figure 16. Bidirectional FIFO Mode



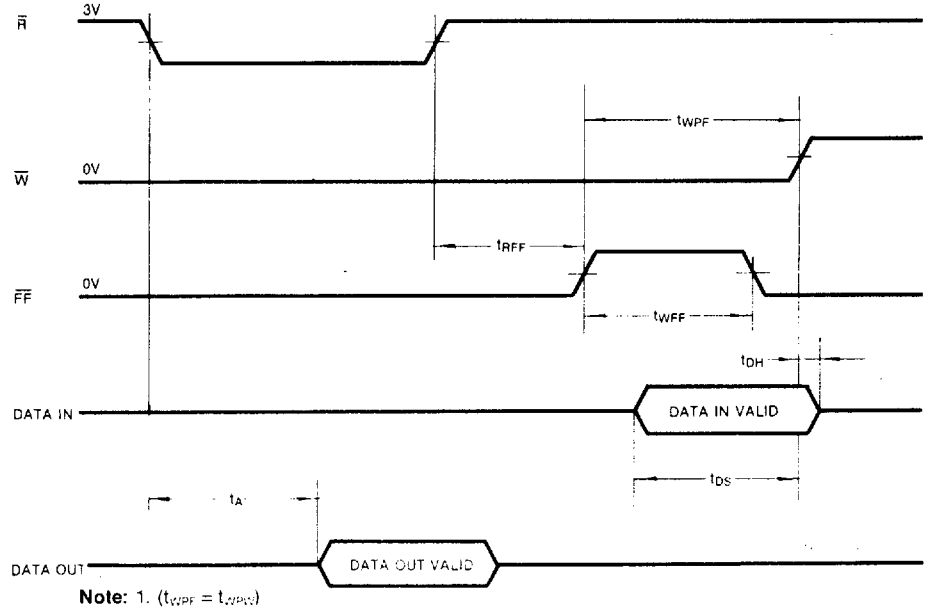
Notes:
1. For depth expansion block see DEPTH EXPANSION Section and Figure 14.
2. For detection see WIDTH EXPANSION Section and Figure 13.

Figure 17. Read Data Flow Through Mode



Note: 1. ($t_{RPE} = t_{RPW}$)

Figure 18. Write Data Flow Through Mode



Note: 1. ($t_{WPF} = t_{WPW}$)