Am29833-34/Am29853-54

Parity Bus Transceivers

PRELIMINARY

DISTINCTIVE CHARACTERISTICS

- High-speed bidirectional bus transceiver for processor organized devices
- Error flag with open-collector output
- Generates odd parity for all-zero protection
- Buffered direction three-state control
- Output short-circuit protected to V_{CC} limits
- 200mV minimum input hysteresis on input data ports
- High-capacitance drive capability
  48mA commercial I_{OL}
  32mA military I_{OL}

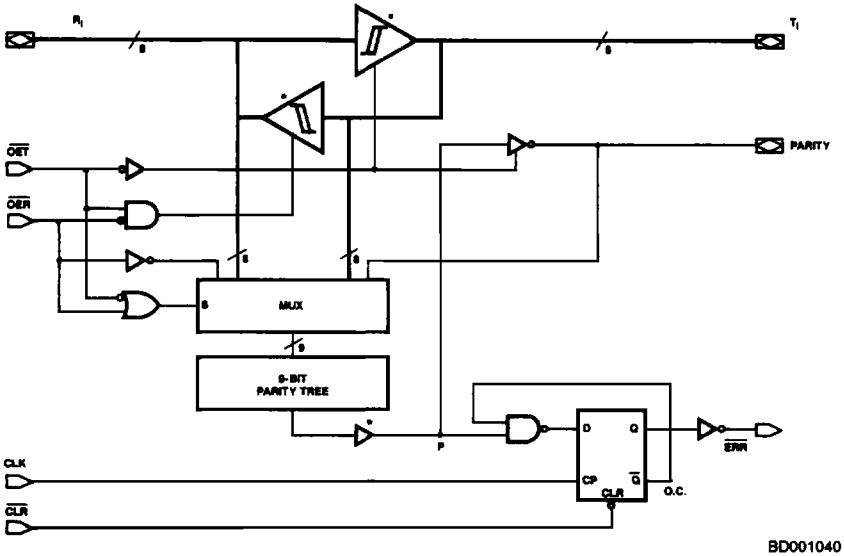
GENERAL DESCRIPTION

The Am29833/34/53/54 are high-performance bus transceivers designed for two-way communications. They each contain an 8-bit data path from the R (port) to the T (port), a 9-bit data path from the T (port) to the R (port), and a 9-bit parity checker/generator. Two options are available. The Am29833/34 register option, and the Am29853/54 latch option. With the register option, the error flag can be clocked and stored in a register and read at the open-collector $\overline{ERR}$ output. The clear ($\overline{CLR}$) input is used to clear the error flag register. With the latch option, the error can be either passed, stored, sampled or cleared at the error flag output by using the $\overline{EN}$ and $\overline{CLR}$ controls.

The output enables $\overline{OET}$ and $\overline{OER}$ are used to force the port outputs to the high-impedance state so that the device can drive bus lines directly. In addition, the $\overline{OER}$ and $\overline{OET}$ can be used to force a parity error by enabling both lines simultaneously. This transmission of inverted parity gives the designer more system diagnostic capability. The Am29833 and Am29853 are noninverting, while the Am29834 and Am29854 present inverting data at the outputs. The devices are specified at 48mA output sink current over the commercial range and 32mA over the military range.

BLOCK DIAGRAM

Am29833
(Device Shown Noninverting)



BD001040

*Noninverting buffer for Am29833; inverting buffer for Am29834.

*Note that the inverting device converts the positive logic "R" bus levels to negative logic levels on the "T" bus.

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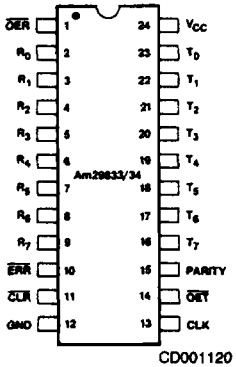
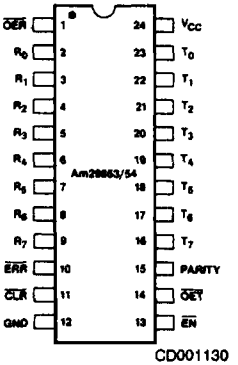
Refer to Page 13-1 for Essential Information on Military Devices

CONNECTION DIAGRAM
Top View

8-BIT TO 9-BIT PARITY TRANSCEIVERS



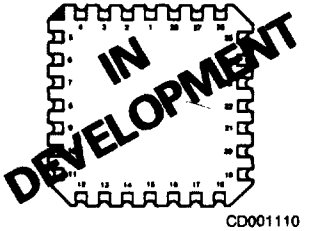
CD001120



CD001130

Leadless Chip Carrier

L-28-1



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ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).

Am29833 - 34
Am29853 - 54 **D** **C** **B**

- B — Screening Option
  - Blank – Standard processing
  - B – Burn-in
- C — Temperature (See Operating Range)
  - C – Commercial (0°C to +70°C)
  - M – Military (–55°C to +125°C)
- D — Package
  - D – 24-pin SLIM DIP (D-24-SLIM)
  - L – 28-pin Leadless Chip Carrier (L-28-1)
  - X – Dice

Device type
Parity Bus Transceivers

Valid Combinations	
Am29833 Am29834 Am29853 Am29854	DC, DCB, DM, DMB LC, LCB, LM, LMB XC, XM

Valid Combinations

Consult the AMD sales office in your area to determine if a device is currently available in the combination you wish.

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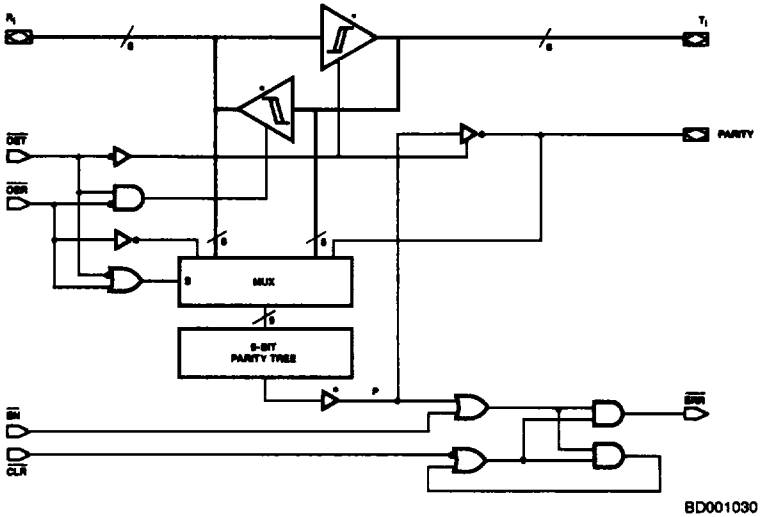
PIN DESCRIPTION

Pin No.	Name	I/O	Description
Am29833 – 34			
1	$\overline{OER}$	I	RECEIVE enable input.
	R_i	O	8-bit RECEIVE data output.
10	$\overline{ERR}$	O	Output from fault registers. Registers detection of odd parity fault on using clock edge (CLK). A registered $\overline{ERR}$ output remains LOW until cleared.
11	$\overline{CLR}$	O	Clears the fault register output.
	T_i	O	8-bit TRANSMIT data output.
15	PARITY	O	1-bit PARITY output.
14	$\overline{OET}$	I	TRANSMIT enable input.
13	CLK	I	External clock pulse input for fault register flag.
Am29853/54			
1	$\overline{OER}$	I	RECEIVE enable input.
	R_i	O	8-bit RECEIVE data output.
10	$\overline{ERR}$	O	Output from fault latches. Latches detection of odd parity fault on active enable $\overline{EN}$. A latched $\overline{ERR}$ output remains LOW until cleared.
11	$\overline{CLR}$	O	Clears the fault latch output.
	T_i	O	8-bit TRANSMIT data output.
15	PARITY	O	1-bit PARITY output.
14	$\overline{OET}$	I	TRANSMIT enable input.
13	$\overline{EN}$	I	Enable latch input for fault flag.

BLOCK DIAGRAM
Am29853
(Device Shown Noninverting)



BD001030

*Noninverting buffer for Am29853; inverting buffer for Am29854.
*Note that the inverting device converts the positive logic "R" bus levels to negative logic levels on the "T" bus.

FUNCTION TABLES

Am29833 NONINVERTING OPTION

Inputs						Outputs				
$\overline{OET}$	$\overline{OER}$	$\overline{CLR}$	CLK	R_i (Σ of H's)	T_i Incl Parity (Σ of H's)	R_i	T_i	Parity	$\overline{ERR}$[1]	Function
L	H	–	–	H (Odd)	NA	NA	H	L	NA	Transmit data from R Port
L	H	–	–	H (Even)	NA	NA	H	H	NA	to T Port with parity,
L	H	–	–	L (Odd)	NA	NA	L	L	NA	receiving path is disabled
L	H	–	–	L (Even)	NA	NA	L	H	NA	
H	L	H	↑	NA	H (Odd)	H	NA	NA	H	Receive data from T Port
H	L	H	↑	NA	H (Even)	H	NA	NA	L	to R Port with parity
H	L	H	↑	NA	L (Odd)	L	NA	NA	H	test resulting in flag,
H	L	H	↑	NA	L (Even)	L	NA	NA	L	transmitting path is disabled
–	–	L	–	–	–	–	NA	NA	H	Clear the state of error flag register
H	H	H	–	–	–	Z	Z	Z	NC	Both transmitting and
H	H	L	–	–	–	Z	Z	Z	H	receiving paths are disabled.
H	H	H	↑	L (Odd)	–	Z	Z	Z	H	Parity logic defaults to
H	H	H	↑	H (Even)	–	Z	Z	Z	L	transmit mode
L	L	–	–	H (Odd)	NA	NA	H	H	NA	Forced-error checking
L	L	–	–	H (Even)	NA	NA	H	L	NA	
L	L	–	–	L (Odd)	NA	NA	L	H	NA	
L	L	–	–	L (Even)	NA	NA	L	L	NA	

Am29834 INVERTING OPTION*

Inputs						Outputs				
$\overline{OET}$	$\overline{OER}$	$\overline{CLR}$	CLK	R_i (Σ of L's)	T_i Incl Parity (Σ of H's)	R_i	T_i	Parity	$\overline{ERR}$[1]	Function
L	H	–	–	H (Odd)	NA	NA	L	H	NA	Transmit data from R Port
L	H	–	–	H (Even)	NA	NA	L	L	NA	to T Port with parity,
L	H	–	–	L (Odd)	NA	NA	H	H	NA	receiving path is disabled
L	H	–	–	L (Even)	NA	NA	H	L	NA	
H	L	H	↑	NA	H (Odd)	L	NA	NA	H	Receive data from T Port
H	L	H	↑	NA	H (Even)	L	NA	NA	L	to R Port with parity
H	L	H	↑	NA	L (Odd)	H	NA	NA	H	test resulting in flag,
H	L	H	↑	NA	L (Even)	H	NA	NA	L	transmitting path is disabled
–	–	L	–	–	–	–	–	–	H	Clear the state of error flag register
H	H	H	–	–	–	Z	Z	Z	NC	Both transmitting and
H	H	L	–	–	–	Z	Z	Z	H	receiving paths are disabled.
H	H	H	↑	L (Odd)	–	Z	Z	Z	L	Parity logic defaults to
H	H	H	↑	L (Even)	–	Z	Z	Z	H	transmit mode
L	L	–	–	H (Odd)	NA	NA	L	L	NA	Forced-error checking
L	L	–	–	H (Even)	NA	NA	L	H	NA	
L	L	–	–	L (Odd)	NA	NA	H	L	NA	
L	L	–	–	L (Even)	NA	NA	H	H	NA	

H = High
L = Low
↑ = Low to high transition of clock
NC = No change
Z = High impedance
NA = Not applicable
– = Don't care or irrelevant
Odd = Odd number of logic one's
Even = Even number of logic one's
i = 0, 1, 2, 3, 4, 5, 6, 7

*Note that for the negative logic levels on the B Port, an "H" represents a logic "0" while an "L" represents a logic "1."
1. Output state assumes HIGH output pre-state.

ERROR FLAG OUTPUT TRUTH TABLE

Am29833 – Am29834 (REGISTER OPTION)

Inputs		Internal to Device	Outputs Pre-state	Output	
CLR	CLK	Point "P"	$\overline{ERR}_{n-1}$	$\overline{ERR}$	Function
H	↑	H	H	H	Sample*
H	↑	–	L	L	(1's
H	↑	L	–	L	Capture)
L	–	–	–	H	Clear

*Enable is used as strobe for the latch in sampled operation.

Am29853/Am29854 (LATCH OPTION)

Inputs		Internal to Device	Outputs Pre-state	Output	
$\overline{EN}$	$\overline{CLR}$	Point "P"	$\overline{ERR}_{n-1}$	$\overline{ERR}$	Function
L	L	L	–	L	Pass
L	L	H	–	H	
L	H	L	–	L	Sample*
L	H	–	L	L	(1's
L	H	H	H	H	Capture)
H	L	–	–	H	Clear
H	H	–	L	L	Store*
H	H	–	H	H	

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Refer to Page 13-1 for Essential Information on Military Devices

Am29853 NONINVERTING OPTION

Inputs						Outputs				
$\overline{OET}$	$\overline{OER}$	$\overline{CLR}$	CLK	R_I (Σ of H's)	T_I Incl Parity (Σ of H's)	R_I	T_I	Parity	$\overline{ERR}$[1]	Function
L	H	–	–	H (Odd)	NA	NA	H	L	NA	Transmit data from R Port to T Port with parity, receiving path is disabled
L	H	–	–	H (Even)	NA	NA	H	H	NA	
L	H	–	–	L (Odd)	NA	NA	L	L	NA	
L	H	–	–	L (Even)	NA	NA	L	H	NA	
H	L	L	L	NA	H (Odd)	H	NA	NA	H	Receive data from T Port to R Port with parity test resulting in flag, transmitting path is disabled
H	L	L	L	NA	H (Even)	H	NA	NA	L	
H	L	L	L	NA	L (Odd)	L	NA	NA	H	
H	L	L	L	NA	L (Even)	L	NA	NA	L	
H	L	H	L	NA	H (Odd)	H	NA	NA	H	Receive data from T Port to R Port, pass the error test resulting to error flag, transmitting path is disabled
H	L	H	L	NA	H (Even)	H	NA	NA	L	
H	L	H	L	NA	L (Odd)	L	NA	NA	H	
H	L	H	L	NA	H (Even)	L	NA	NA	L	
H	L	H	H	NA	–	–	NA	NA	ERR_{n-1}	Store the state of error flag register
–	–	L	H	–	–	–	NA	NA	H	Clear the state of error flag register
H	H	H	H	–	–	Z	Z	Z	NC	Both transmitting and receiving paths are disabled. Parity logic defaults to transmit mode
H	H	L	H	–	–	Z	Z	Z	H	
H	H	–	L	L (Odd)	–	Z	Z	Z	H	
H	H	–	L	H (Even)	–	Z	Z	Z	L	
L	L	–	–	H (Odd)	NA	NA	H	H	NA	Forced-error checking
L	L	–	–	H (Even)	NA	NA	H	L	NA	
L	L	–	–	L (Odd)	NA	NA	L	H	NA	
L	L	–	–	L (Even)	NA	NA	L	L	NA	

Am29854 INVERTING OPTION*

Inputs						Outputs				
$\overline{OET}$	$\overline{OER}$	$\overline{CLR}$	CLK	R_I (Σ of H's)	T_I Incl Parity (Σ of H's)	R_I	T_I	Parity	$\overline{ERR}$[1]	Function
L	H	–	–	H (Odd)	NA	NA	L	H	NA	Transmit data from R Port to T Port with parity, receiving path is disabled
L	H	–	–	H (Even)	NA	NA	L	L	NA	
L	H	–	–	L (Odd)	NA	NA	H	H	NA	
L	H	–	–	L (Even)	NA	NA	H	L	NA	
H	L	L	L	NA	H (Odd)	L	NA	NA	H	Receive data from T Port to R Port with parity test resulting in flag, transmitting path is disabled
H	L	L	L	NA	H (Even)	L	NA	NA	L	
H	L	L	L	NA	L (Odd)	H	NA	NA	H	
H	L	L	L	NA	L (Even)	H	NA	NA	L	
H	L	H	L	NA	H (Odd)	L	NA	NA	H	Receive data from T Port to R Port, pass the error test resulting to error flag, transmitting path is disabled
H	L	H	L	NA	H (Even)	L	NA	NA	L	
H	L	H	L	NA	L (Odd)	H	NA	NA	H	
H	L	H	L	NA	L (Even)	H	NA	NA	L	
H	L	H	H	NA	–	–	NA	NA	ERR_{n-1}	Store the state of error flag register
–	–	L	H	–	–	–	NA	NA	H	Clear the state of error flag register
H	H	H	H	–	–	Z	Z	Z	NC	Both transmitting and receiving paths are disabled. Parity logic defaults to transmit mode
H	H	L	H	–	–	Z	Z	Z	H	
H	H	–	L	L (Odd)	–	Z	Z	Z	L	
H	H	–	L	L (Even)	–	Z	Z	Z	H	
L	L	–	–	H (Odd)	NA	NA	L	L	NA	Forced-error checking
L	L	–	–	H (Even)	NA	NA	L	H	NA	
L	L	–	–	L (Odd)	NA	NA	H	L	NA	
L	L	–	–	L (Even)	NA	NA	H	H	NA	

H = High
L = Low
Z = High impedance
NC = No change

NA = Not applicable
$\overline{ERR}_{n-1}$ = Pre-state of $\overline{ERR}$
– = Don't care or irrelevant

Odd = Odd number of logic one's
Even = Even number of logic one's
i = 0, 1, 2, 3, 4, 5, 6, 7

*Note that for the negative logic levels on the B Port, an "H" represents a logic "0" while an "L" represents a logic "1."
1. Output state assumes HIGH output pre-state.

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Refer to Page 13-1 for Essential Information on Military Devices

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
Ambient Temperature with
Power Applied ..... −55°C to +125°C
Supply Voltage to Ground Potential
Continuous ..... −0.5V to +7.0V
DC Voltage Applied to Output
for High Output State ..... −1.5V to V_{CC} max
DC Input Voltage ..... −0.5V to +5.5V
DC Output Current, into Outputs 100mA
DC Input Current ..... −30mA to +5.0mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.75V to +5.25V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

Operating ranges define those limits over which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

Parameters	Description	Test Conditions			Min	Typ (Note 1)	Max	Units
V_{OH}	Output HIGH Voltage (Except ERR)	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}		I_{OH} = −15mA	2.4			V
				I_{OH} = −24mA	2.0			
V_{OL}	Output LOW Voltage	V_{CC} = MIN	ERR	I_{OL} = 48mA			0.5	V
			All Other Outputs V_{IN} = V_{IH} or V_{IL}	I_{OL} = 32mA MIL			0.5	
				I_{OL} = 48mA COM'L			0.5	
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for All Inputs			2.0			V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for All Inputs					0.8	V
V_I	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA					−1.2	V
V_{HYST}	Hysteresis for Inputs R_i, T_i	Output Connected to AC Test Load Circuit			200			mV
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.4V		Data			−1.0	mA
				Control			−2.0	
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.7V					50	μA
I_I	Input HIGH Current	V_{CC} = MAX, V_{IN} = 5.5V					1.0	mA
I_{OZH}	Off-State Output Current (High Impedance)	V_{CC} = MAX		V_O = 2.4V			+100	μA
I_{OZL}				V_O = 0.4V			−1.0	mA
I_{SC}	Output Short Circuit Current	V_{CC} = MAX			75		250	mA
I_{CC}	Power Supply Current	V_{CC} = MAX (All Outputs Are Open)		Over Temperature Range			195	mA
				+70°C			180	
				+125°C			170	

Note: 1 Typical units are TA = 25°C, V_{CC} = 5V.

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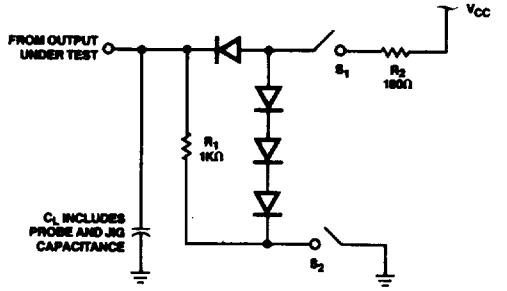
Refer to Page 13-1 for Essential Information on Military Devices

SWITCHING TEST CIRCUIT

CIRCUIT NO. 1



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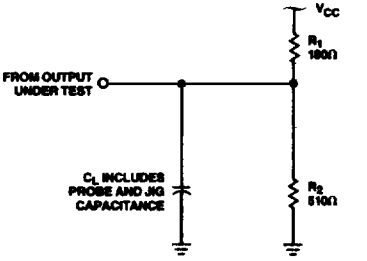
CIRCUIT NO. 2



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Note: Test Circuit No. 1 is used with Propagation delay

SWITCHING CHARACTERISTICS (T_A = +25°C, V_{CC} = 5.0V)

Parameters	Description		Test Conditions	Min	Type	Max	Units
t_{PLH}	Propagation Delay R_i to T_i, T_i to R_i		C_L = 50pF			12	ns
t_{PHL}						12	ns
t_{PLH}			C_L = 300pF			16	ns
t_{PHL}						16	ns
t_{PLH}	Propagation Delay R_i to PARITY		C_L = 50pF			15	ns
t_{PHL}						15	ns
t_{PLH}			C_L = 300pF			22	ns
t_{PHL}						22	ns
t_{ZH}	Output Enable Time $\overline{OER}$, $\overline{OET}$ to R_i, T_i		C_L = 50pF			15	ns
t_{ZL}						15	ns
t_{ZH}			C_L = 300pF			20	ns
t_{ZL}						23	ns
t_{HZ}	Output Disable Time $\overline{OER}$, $\overline{OET}$ to R_i, T_i		C_L = 5pF			9	ns
t_{LZ}						10	ns
t_{HZ}			C_L = 50pF			17	ns
t_{LZ}						12	ns
t_S	T_i, PARITY to CLK Setup Time*		C_L = 50pF	15			ns
t_H	T_i, PARITY to CLK Hold Time*			0			ns
t_S	Clear Recovery Time $\overline{CLR}$ to CLK**			15			ns
t_{PWH}	Clock Pulse Width*	HIGH		10			ns
t_{PWL}		LOW		10			ns
t_{PWL}	Clear Pulse Width	LOW		10			
t_{PHL}	Propagation Delay CLK to $\overline{ERR}$*		C_L = 50pF			15	ns
t_{PLH}	Propagation Delay $\overline{CLR}$ to $\overline{ERR}$		C_L = 50pF			15	ns
t_{PLH}	Propagation-Delay t_i, PARITY $\overline{ERR}$ (PASS Mode Only) Am29853/54		C_L = 50pF			22	ns
t_{PHL}						18	ns
t_{PLH}	Propagation Delay $\overline{OER}$ to Parity		C_L = 50pF Test Ckt #1			15	ns
t_{PHL}						15	ns
t_{PLH}			C_L = 300pFTest Ckt #1			22	ns
t_{PHL}						22	ns

*For Am29853/54 replace CLK with $\overline{EN}$.
**Note: Not applicable to Am29853/54.

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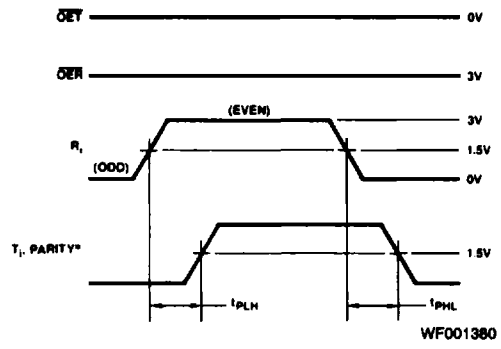
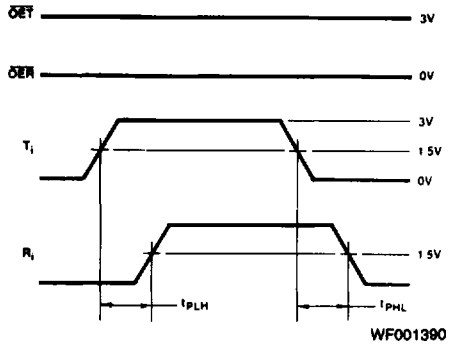
Refer to Page 13-1 for Essential Information on Military Devices

Am29833/53 SWITCHING WAVEFORMS (NONINVERTING OPTION)

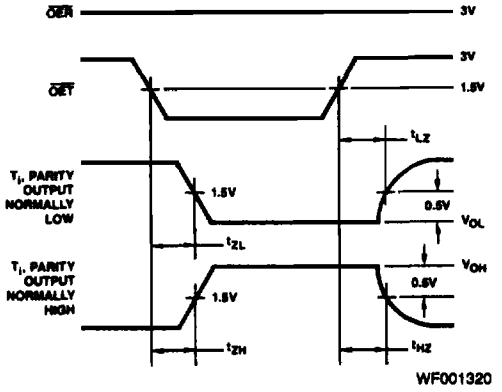


a. R_I to T_I, PARITY

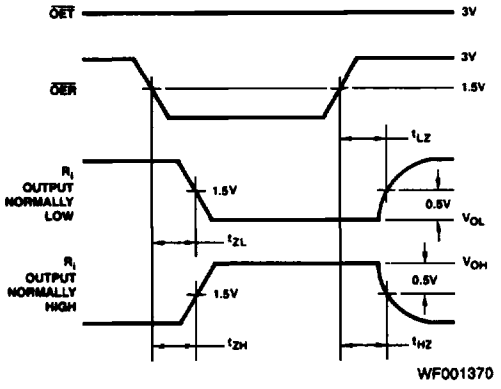


b. T_I to R_I

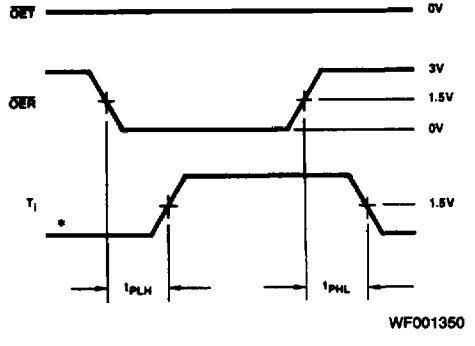
*Calculation must be done from last arriving signal.

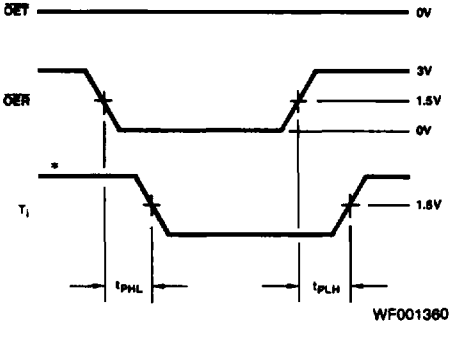


c. $\overline{OET}$ to T_I, PARITY



d. $\overline{OER}$ to R_I



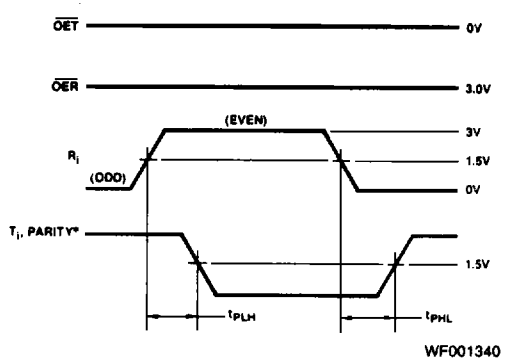


e. $\overline{OER}$ to PARITY

00370B

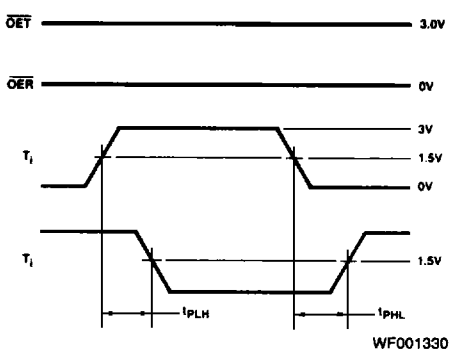
Refer to Page 13-1 for Essential Information on Military Devices

Am29834/54 SWITCHING WAVEFORMS (INVERTING OPTION)



WF001340

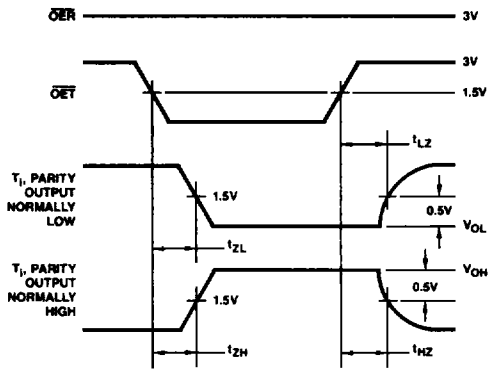
a. R_I to T_I, PARITY



WF001330

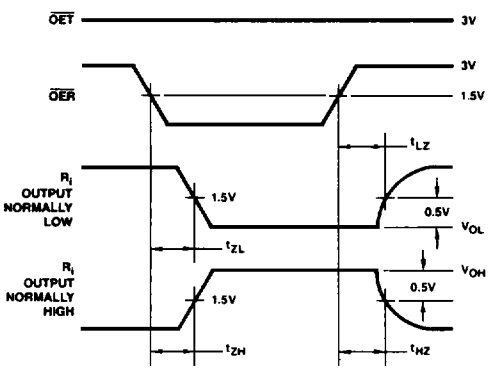
b. T_I to R_I

*Calculation must be done from last arriving signal.



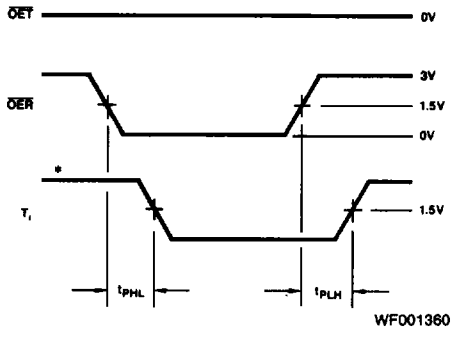
WF001320

c. $\overline{OET}$ to T_I, PARITY

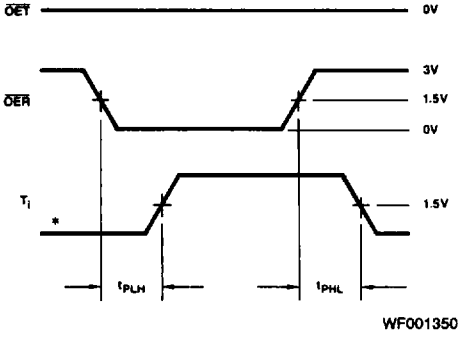


WF001370

d. $\overline{OER}$ to R_I



WF001360



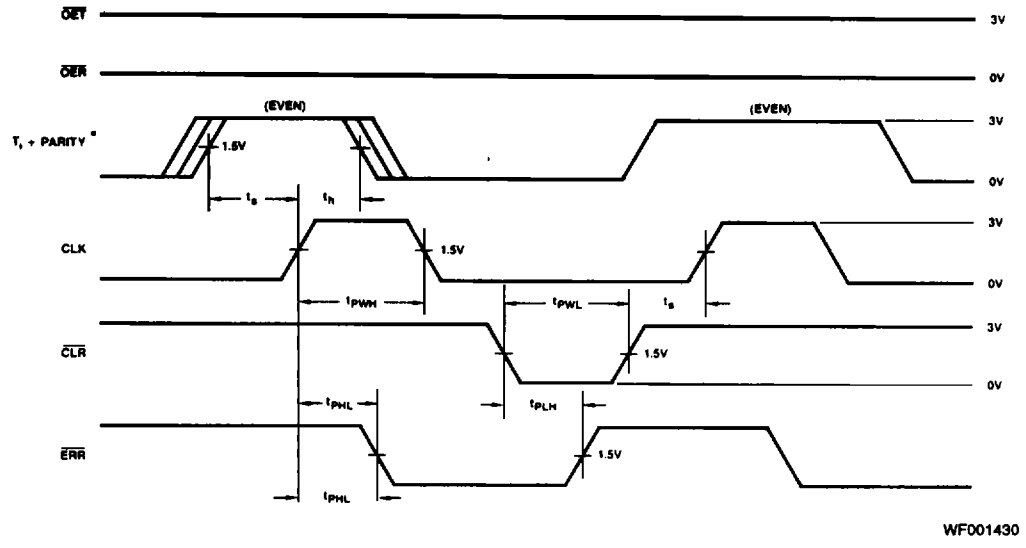
WF001350

e. $\overline{OER}$ to PARITY

00370B

Refer to Page 13-1 for Essential Information on Military Devices

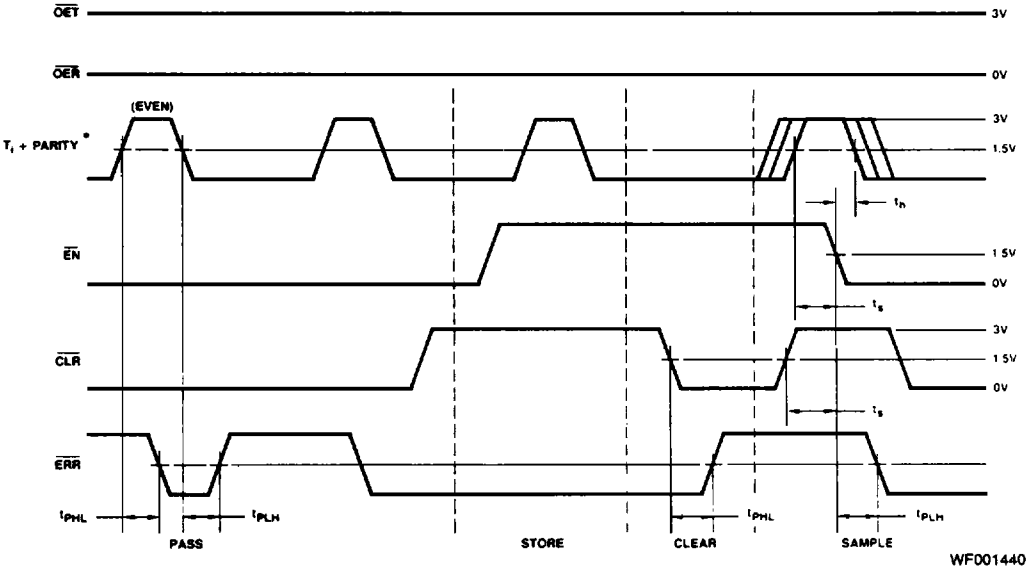
SWITCHING WAVEFORMS (REGISTER OPTION, Am29833/34)



WF001430

a. CLK, $\overline{CLR}$ to $\overline{ERR}$

SWITCHING WAVEFORMS (LATCH OPTION, Am29853/54)



WF001440

b. T_I, PARITY, $\overline{EN}$, $\overline{CLR}$ to $\overline{ERR}$

*Calculation must be done from last arriving signal.

8

00370B

Refer to Page 13-1 for Essential Information on Military Devices