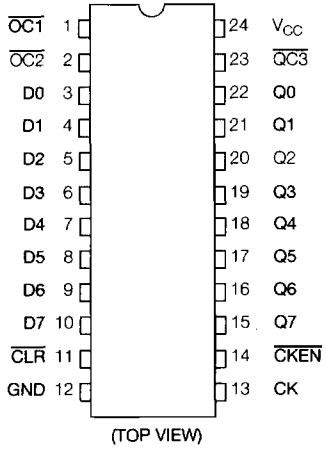
TC74ACT825 Octal D-Type Flip-Flop with 3-State Output

Features:

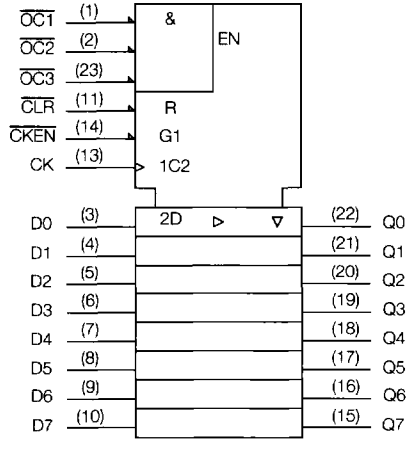
- **High Speed:** f_{MAX} = 160MHz (typ.) at V_{CC} = 5V
- **Low Power Dissipation:** I_{CC} = 8μA (max.) at Ta = 25°C
- **High Noise Immunity:** V_{IL} = 0.8V (max.); V_{IH} = 2.0V (min.)
- **Symmetrical Output Impedance:** $|I_{OH}| = I_{OL}$ = 24mA (min.). Capability of driving 50Ω transmission lines.
- **Balanced Propagation Delays:** $t_{pLH} = t_{pHL}$
- **Pin and Function Compatible with 74F825**
- **Available in DIP Package**

Pin Assignment



(TOP VIEW)

IEC Logic Symbol



The TC74ACT825 is an advanced high speed CMOS OCTAL D-TYPE FLIP-FLOP with 3-STATE OUTPUT fabricated with silicon gate and double-layer metal wiring C^2MOS technology.

It achieves the high speed operation similar to equivalent Bipolar Schottky TTL, while maintaining the CMOS low power dissipation.

This device can be used as a level convertor for interfacing TTL input level of TTL or NMOS device to CMOS input level of Advanced High Speed CMOS. The inputs can be connected to outputs of TTL, NMOS and CMOS devices directly.

It consists of eight D-TYPE edge-triggered flip-flops. The Clock ($\overline{CK}$), Clock Enable ($\overline{CKEN}$), Clear ($\overline{CLR}$) and Enable ($\overline{OC1}$, $\overline{OC2}$, $\overline{OC3}$) are common to all flip-flops.

When the $\overline{CKEN}$ is LOW, signals applied to D inputs are transferred to the Q outputs on the positive going edge of the clock signal.

With the $\overline{CLR}$ LOW all Q outputs are at low level independent of the other inputs.

When one of $\overline{OC1}$, $\overline{OC2}$, or $\overline{OC3}$ is HIGH, the outputs go to the high impedance state.

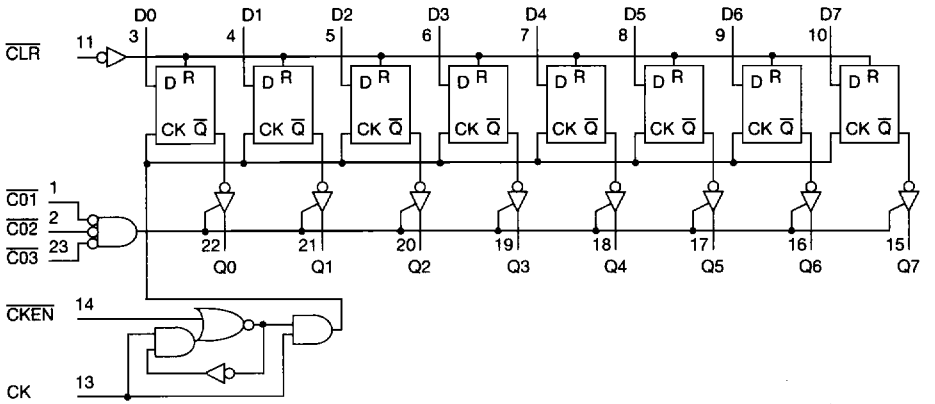
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

Truth Table

INPUTS					OUTPUTS
$\overline{OC}$	$\overline{CLR}$	$\overline{CKEN}$	CK	D	Q
L	L	X	X	X	L
L	H	L	↑	H	H
L	H	L	↑	L	L
L	H	H	X	X	Qn
H	X	X	X	X	Z

X: Don't Care
Z: High Impedance
Q: No Change
$\overline{OC} = \overline{OC1} + \overline{OC2} + \overline{OC3}$

System Diagram



Absolute Maximum Ratings

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5~7.0	V
DC Input Voltage	V_{IN}	-0.5~V_{CC} + 0.5	V
DC Output Voltage	V_{OUT}	-0.5~V_{CC} + 0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±50	mA
DC Output Current	I_{OUT}	±50	mA
DC V_{CC}/Ground Current	I_{CC}	±200	mA
Power Dissipation	P_D	500 (DIP) *	mW
Storage Temperature	T_{stg}	-65~150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta = -40°C~65°C. From Ta = 65°C to 85°C a derating factor of -10mW/°C should be applied up to 300mW.

Recommended Operating Conditions

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	4.5~5.5	V
Input Voltage	V_{IN}	0~V_{CC}	V
Output Voltage	V_{OUT}	0~V_{CC}	V
Operating Temperature	T_{opr}	-40~85	°C
Input Rise and Fall Time	dt/dv	0~10	ns/v

DC Electrical Characteristics

PARAMETER	SYMBOL	TEST CONDITION			Ta = 25°C			Ta = -40~85°C		UNIT
				V_{CC}	Min.	Typ.	Max.	Min.	Max.	
High-Level Input Voltage	V_{IH}	—		4.5~5.5	2.0	—	—	2.0	—	V
Low-Level Input Voltage	V_{IL}	—		4.5~5.5	—	—	0.8	—	0.8	V
High-Level Output Voltage	V_{OH}	$V_{IN} = V_{IH}$ or V_{IL}	I_{OH} = -50μA	4.5	4.4	4.5	—	4.4	—	V
			I_{OH} = -24mA	4.5	3.94	—	—	3.80	—	
			I_{OH} = -75mA*	5.5	—	—	—	3.85	—	
Low-Level Output Voltage	V_{OL}	$V_{IN} = V_{IH}$ or V_{IL}	I_{OL} = 50μA	4.5	—	0.0	0.1	—	0.1	V
			I_{OL} = 24mA	4.5	—	—	0.36	—	0.44	
			I_{OL} = 75mA*	5.5	—	—	—	—	1.65	
3-State Output Off-State Current	I_{OZ}	$V_{IN} = V_{IH}$ or V_{IL} $V_{OUT} = V_{CC}$ or GND		5.5	—	—	±0.5	—	±5.0	μA
Input Leakage Current	I_{IN}	$V_{IN} = V_{CC}$ or GND		5.5	—	—	±0.1	—	±1.0	
Quiescent Supply Current	I_{CC}	$V_{IN} = V_{CC}$ or GND		5.5	—	—	8.0	—	80.0	
	I_C	Per input: V_{CC} = 3.4V Other input: V_{CC} or GND		5.5	—	—	1.35	—	1.5	mA

* This spec indicates the capability of driving 50Ω transmission lines.
One output should be tested at a time for a 10ms maximum duration.

Timing Requirements (Input $t_r = t_f$ = 3n)

PARAMETER	SYMBOL	TEST CONDITION	Ta=25°C		Ta= -40~85°	UNIT
			V_{CC}	Typ.	Limit	Limit	
Minimum Pulse Width (CK)	$t_{W(H)}$ $t_{W(L)}$	—	5.0±0.5	—	5.0	5.0	ns
Minimum Pulse Width ($\overline{CLR}$)	$t_{W(L)}$	—	5.0±0.5	—	5.0	5.0	
Minimum Set-up Time (DATA–CK)	t_s	—	5.0±0.5	—	3.0	3.0	
Minimum Set-up Time ($\overline{CKEN}$–CK)	t_s	—	5.0±0.5	—	4.0	4.0	
Minimum Hold Time (DATA–CK)	t_h	—	5.0±0.5	—	2.0	2.0	
Minimum Hold Time ($\overline{CKEN}$–CK)	t_h	—	5.0±0.5	—	2.0	2.0	
Minimum Removal Time ($\overline{CLR}$)	t_{rem}	—	5.0±0.5	—	2.0	2.0	

AC Electrical Characteristics (C_L = 50pF, R_L = 500Ω, Input $t_r = t_f$ = 3ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta = 25°C			Ta = -40~85°C		UNIT
			V_{CC}	Min.	Typ.	Max.	Min.	Max.	
Propagation Delay Time (CK–Q)	t_{pLH} t_{pHL}	—	5.0±0.5	—	6.9	11.0	—	12.5	ns
Propagation Delay Time ($\overline{CLR}$–Q)	t_{pHL}	—	5.0±0.5	—	7.4	12.0	—	13.5	
Output Enable Time	t_{pZL} t_{pZH}	—	5.0±0.5	—	6.9	11.0	—	12.5	
Output Disable Time	t_{pLZ} t_{pHZ}	—	5.0±0.5	—	6.8	9.5	—	11.0	
Maximum Clock Frequency	f_{MAX}	—	5.0±0.5	90	140	—	80	—	MHz
Input Capacitance	C_{IN}	—	—	—	5	10	—	10	pF
Output Capacitance	C_{OUT}	—	—	—	10	—	—	—	
Power Dissipation Capacitance	C_{PD} [1]	—	—	—	56	—	—	—	

Note (1): C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC\ (opr)} = C_{PD} \bullet V_{CC} \bullet f_{IN} + I_{CC}/8$ (per F/F). And the total C_{PD} when n pcs. of Flip-Flop operate can be gained by the following equation: C_{PD} (total) = 43 + 13 • n.