FUJITSU SEMICONDUCTOR
DATA SHEET

DS04-29146-1E

ASSP

Spread Spectrum Clock Generator

MB88R157A

■ DESCRIPTION

MB88R157A is a clock generator for EMI (Electro Magnetic Interference) reduction. The peak of unnecessary radiation noise (EMI) can be attenuated by making the oscillation frequency slightly modulate periodically with the internal modulator.
This product has a built-in non-volatile memory, so its frequency setting can memorize each system or application. Also the product has a built-in oscillation stabilization circuit, so it is not necessary to use the external oscillation stabilization capacitance.

■ FEATURES

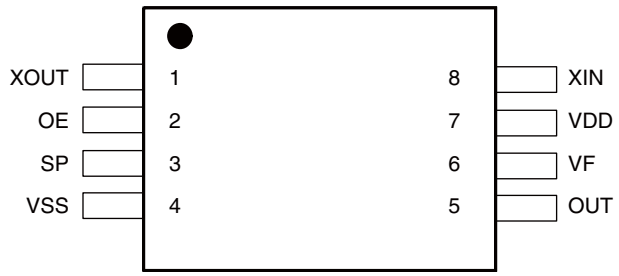
- Input frequency : 10 MHz to 50 MHz
- Output frequency : 1 MHz to 134 MHz
  Programmable of the parameter of N divider, M divider, K divider
  (N divider : 11-bit, M divider : 12-bit, K divider : 7-bit)
- Modulation rate : no modulation, ±0.125%, ±0.25%, ±0.5%, ±0.75%, ±1.0%, ±1.25%, ±1.5%, ±1.75%
- Variable function pin
  It is possible to switch the VF pin function by setting to a non-volatile memory.
  Modulation enabled: It is possible to turn on/off the modulation operation.
  Power down control
  Output setting selection: It is possible to save two types of frequency setting into a non-volatile memory, and to select the type to operate.
- Equipped with a crystal oscillation circuit
- Built-in oscillation stabilization capacitance : 5 pF to 10 pF (0.039 pF step range)
- Clock output Duty : 45% to 55%
- Clock Cycle-Cycle Jitter : Less than 100 ps (Output clock is over 3 MHz)
- Low power consumption by CMOS process 5 mA (24 MHz, Typ-sample, no load) [Target value]
  (Input frequency : 24 MHz, N divider parameter : 200, M divider parameter : 200, K divider parameter : 1)
- At power down: 5 μA (Power supply voltage = 3.3 V, at room temperature) [Target value]
- Power supply voltage : 3.3 V ± 0.3 V
- Operating temperature –20 °C to + 85 °C
- Package : 8-pin plastic TSSOP

2010.7

FUJITSU

■ PIN ASSIGNMENT

TOP VIEW

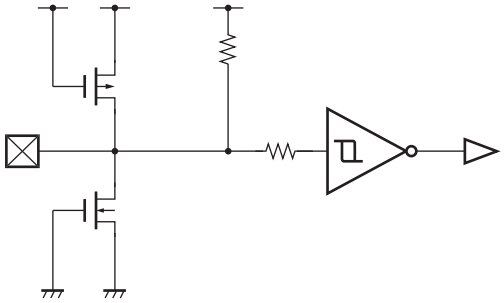
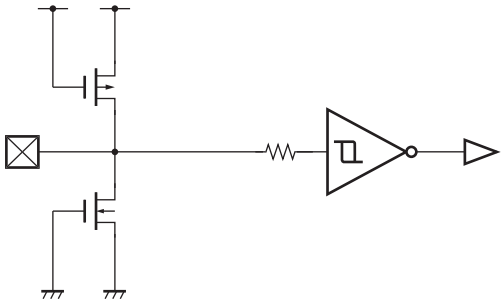
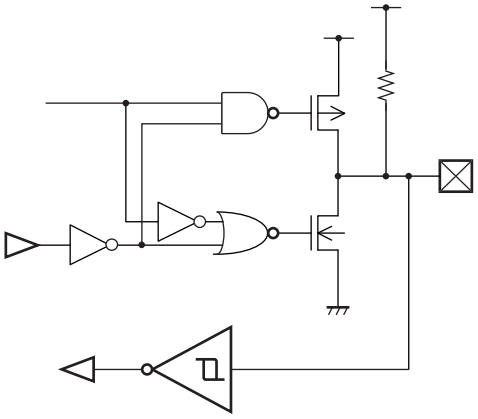
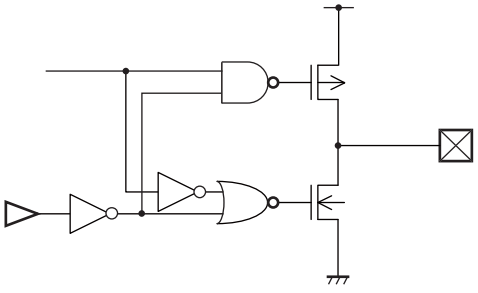


(FPT-8P-M07)

■ PIN DESCRIPTION

Pin name	I/O	Pin no.	Description
XOUT	O	1	Resonator connection pin
OE	I	2	Clock output enable pin L : output disable, H : output enable
SP	I/O	3	Serial program pin
VSS	—	4	GND pin
OUT	O	5	Clock output pin
VF	I	6	Variable function pin It is possible to set the pin function to one of the followings by setting to a memory. <Modulation enable> L : Modulation disable, H: Modulation enable <Power down control> Power down by the “L” input <Output setting select> L : 1 setting, H : 2 setting
VDD	—	7	Power supply voltage pin
XIN	I	8	Resonator connection pin/clock input pin

■ I/O CIRCUIT TYPE

Pin name	Circuit type	Remarks
OE		• CMOS hysteresis input • With pull-up resistor (50 kΩ)
VF		CMOS hysteresis input
SP		With pull-up resistor (50 kΩ) In input mode • CMOS hysteresis input In serial output mode • CMOS output • I_{OL} = 12 mA
OUT		• CMOS output • I_{OL} = 4 mA/8 mA selectable (Selectable by Output driver setting bit) • Hi-Z or “L” output at OE pin = “L” input (Selectable by OUT pin setting bit)

Note : About XIN and XOUT pins, please refer to “■ CRYSTAL OSCILLATION CIRCUIT”.

■ HANDLING DEVICES

1. Preventing Latch-up

A latch-up can occur if, on this device, (a) a voltage higher than power supply voltage or a voltage lower than GND is applied to an input or output pin or (b) a voltage higher than the rating is applied between power supply and GND. The latch-up, if it occurs, significantly increases the power supply current and may cause thermal destruction of an element. When you use this device, be very careful not to exceed the maximum rating.

2. Handling unused pins

Do not leave an unused input pin open, since it may cause a malfunction. Handle by, using a pull-up or pull-down resistor.

3. Notes for when the external clock is used

To use an external clock signal, input the clock signal to the XIN pin with the XOUT pin connected to nothing.

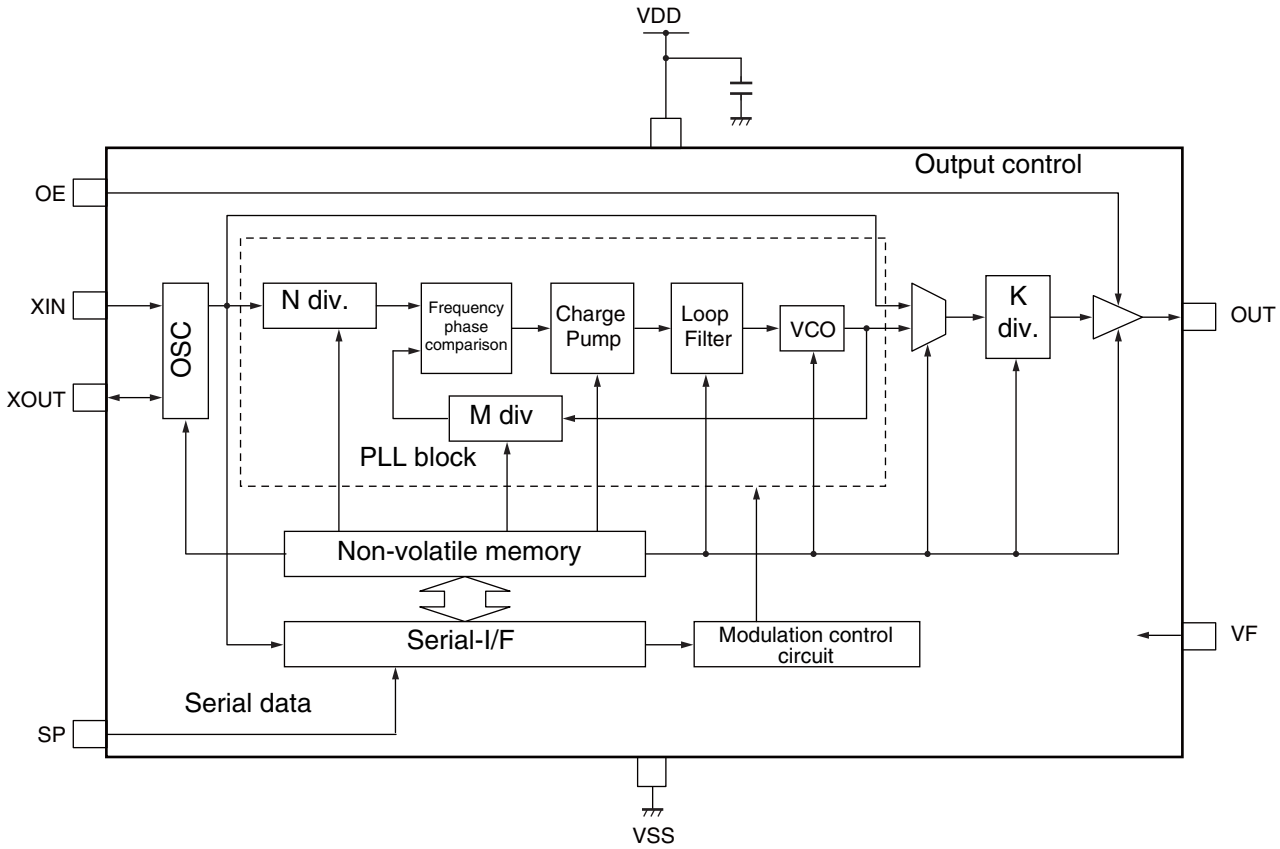
4. Power supply pins

Please design connecting the power supply pin of this device by as low impedance as possible from the current supply source.
We recommend connecting electrolytic capacitor (about 10 μF) and the ceramic capacitor (about 0.01 μF) in parallel between power supply and GND near the device, as a bypass capacitor.

5. Oscillation circuit

Noise near the XIN pin and XOUT pin may cause the device to malfunction. Design printed circuit boards so that electric wiring of the XIN pin or the XOUT pin and the resonator do not intersect other wiring.
Design the printed circuit board that surrounds the XIN pin and XOUT pin with ground in order to stabilize operation.

■ BLOCK DIAGRAM



IDAC (current output D/A converter) provides precise modulation, thereby dramatically reducing EMI.

■ MEMORY MAP

Address		Function	Remarks
	bit0, bit1	VF pin function setting	The function for the VF pin (pin 6) is selectable. 00 : No modulation, 01 : Output selection function, 10 : Modulation control, 11 : Power down control
	bit2 to bit8	XIN oscillation stabilization capacitance setting (7-bit)	Capacitance is selectable from 5 pF to 10 pF by 0.039 pF Step
	bit9 to bit15	XOUT oscillation stabilization capacitance setting (7-bit)	Capacitance is selectable from 5 pF to 10 pF by 0.039 pF Step
Setting 1	bit16 to bit27	M divider setting 1 (12-bit)	Selectable in the range of 2 to 4095
	bit28 to bit38	N divider setting 1 (11-bit)	Selectable in the range of 2 to 2047
	bit39 to bit45	K divider setting 1 (7-bit)	Selectable in the range of 1 to 128
	bit46 to bit48	L divider setting 1 (3-bit)	Modulation frequency setting (the value is due to the input frequency)
	bit49 to bit52	Charge Pump setting 1 (4-bit)	Charge pump current setting due to VCO oscillation frequency
	bit53 to bit57	VCO Gain setting 1 (5-bit)	VCO gain setting due to VCO oscillation frequency
	bit58 to bit61	Modulation rate setting 1 (4-bit)	No modulation, ±0.125%, ±0.25%, ±0.50%, ±0.75%, ±1.00%, ±1.25%, ±1.50%, ±1.75% are selectable
	bit62	Output drive ability setting 1	0: Ability small, 1: Ability large
	bit63	Output slew rate ability setting 1	0 : Slew rate low, 1 : Slew rate high
	bit64	OUT pin setting 1	Selectable OUT pin situation at OE pin = L and power down 0 : L output, 1 : Hi-Z output
	bit65	Source clock dividing mode 1	Source clock for K divider is selectable. 0 : VCO output , 1 : Source clock
	bit66	PLL mode 1	0 : Normal mode, 1 : PLL mode
	bit67	Input clock setting 1	0 : External clock input, 1 : Crystal oscillator
	bit68 to bit71	Reserve	—

(Continued)

(Continued)

Address		Function	Remarks
Setting 2	bit72 to bit83	M divider setting 2 (12-bit)	Selectable in the range of 2 to 4095
	bit84 to bit94	N divider setting 2 (11-bit)	Selectable in the range of 2 to 2047
	bit95 to bit101	K divider setting 2 (7-bit)	Selectable in the range of 1 to 128
	bit102 to bit104	L divider setting 2 (3-bit)	Modulation frequency setting (the value is due to the input frequency)
	bit105 to bit108	Charge Pump setting 2 (4-bit)	Charge pump current setting due to VCO oscillation frequency
	bit109 to bit113	VCO Gain setting 2 (5-bit)	VCO gain setting due to VCO oscillation frequency
	bit114 to bit117	Modulation rate setting 2 (4-bit)	No modulation, ±0.125%, ±0.25%, ±0.50%, ±0.75%, ±1.00%, ±1.25%, ±1.50%, ±1.75% are selectable
	bit118	Output drive ability setting 2	0: Ability small, 1: Ability large
	bit119	Output slew rate ability setting 2	0 : Slew rate low, 1 : Slew rate high
	bit120	OUT pin setting 2	Selectable OUT pin situation at OE pin = L and power down 0 : L output, 1 : Hi-Z output
	bit121	Source clock dividing mode 2	Source clock for K divider is selectable. 0 : VCO output , 1 : Source clock
	bit122	PLL mode 2	0 : Normal mode, 1 : PLL mode
	bit123	Input clock setting 2	0 : External clock input, 1 : Crystal oscillator
	bit124 to bit127	Reserve	—

■ OPERATION SETTING

- **Frequency setting**

Output frequency can be set by writing the internal memory to each divider parameter in the PLL block.
Internal oscillation frequency and output frequency can be calculated by the following expressions :

Internal oscillation frequency (fvco*) = Input frequency (fin) × (M+1) / (N+1)

* : Please set the fvco range from 20 MHz to 134 MHz.

Output frequency (f_{OUT}*) = Input frequency (fin) × (M+1) / ((N+1) × K)

* : Please set the f_{OUT} range from 1 MHz to 134 MHz.

(Setting example)

fin = 27 MHz, f_{OUT} = 60 MHz

M divider parameter : 339 (= 153_H) , N divider parameter : 152 (= 98_H) , K divider parameter : 1 (= 01_H)

$27 \times (339 + 1)/ ((152 + 1) \times 1) = 60$ [MHz], (fvco: $27 \times (339 + 1) / (152 + 1)$ 60 [MHz])

Note: Recommended value of each divider parameter is different at PLL mode and normal mode. Please refer and confirm the recommended value by our support tool. Contact the sales representatives for details on the support tools.

- **Modulation frequency setting**

Modulation frequency can be set by writing L divider parameter to the internal memory.
The average of modulation frequency can be calculated by the following expressions :

$$\frac{\text{Input frequency}}{532 \times (L+1)} \quad (L = 0, 1, 2, 3, 4, 5, 6, 7)$$

Note: Please refer and confirm the recommended value by our support tool. Contact the sales representatives for details on the support tools.

- **Modulation rate setting**

Modulation rate can be selectable from no modulation, ±0.125%, ±0.25%, ±0.50%, ±0.75%, ±1.00%, ±1.25%, ±1.50% and ±1.75%

- **Charge Pump setting, VCO gain setting**

Please refer and confirm the recommended value by our support tool. Contact the sales representatives for details on the support tools.

- **Output drive ability setting**

  The output drive ability of the OUT pin can be selected.

bit62, bit118	OUT pin drive ability
0	Small (I_{OL} = 4 mA)
1	Large (I_{OL} = 8 mA)

- **Output slew rate ability setting**

  The output slew rate ability of the OUT pin can be selected.

bit63, bit119	OUT pin slew rate ability
0	Slew rate low
1	Slew rate high

- **OUT pin setting**

  The OUT pin situation can be selected at OE pin “L” input and power down.

bit64, bit120	OUT pin situation
0	“L” output
1	“Hi-Z” output

Note : Internal oscillation circuit has been operating even if the OE pin is inputting “L”.

- **Source clock dividing setting**

  Source clock for K divider can be selected.
  When “input frequency” is selected, source clock or its divided clock can be output. But modulation setting is not enabled.

bit65, bit121	Source clock for K divider
0	VCO output clock
1	Input clock (Source clock)

- **PLL mode setting**

  It can be selected from normal mode and PLL mode by bit48 setting in the memory map. PLL mode is good jitter specification at non modulation. When the mode is selected, it becomes non modulation setting, the resistance and capacitance value of the loop filter is changed, so oscillation specification will change.

bit66, bit122	Operation mode
0	SSCG mode
1	PLL mode

When PLL mode is selected, the recommended value of M, N, K divider is changed. Please refer and confirm the recommended value by our support tool. Contact the sales representatives for details on the support tools.

• **Input clock setting**

The input type of the source clock is selectable.

bit67, bit123	Input clock
0	External clock input
1	Crystal oscillator

• **VF pin function setting**

The function for the VF pin (pin6) is selectable.

bit1	bit0	VF pin (pin6) function
0	0	No function
0	1	Output selection function
1	0	Modulation control
1	1	Power down control

When setting the output select function, either setting 1 or setting 2 is selected to operate at the input level of pin6 while turning the power on. Even if the input level of pin6 is changed during the operation, the operation cannot be changed.

When setting the output select function, it is recommended to connect pin6 to Pull-up or Pull-down.

Setting 1 is selected to operate when the mode other than the output select function is set.

pin6	Operation at selection function setting
L	Operation in setting 1
H	Operation in setting 2

When setting the modulation control, the modulation function is turned on and off at the input level of pin6.

pin6	Operation at modulation control setting
L	No modulation
H	Execute the modulation operation according to the modulation rate setting

When setting the power down control, the power down control for the whole device is performed at the input level of pin6.

pin6	Operation at power down control setting
L	Power down
H	Clock output operation

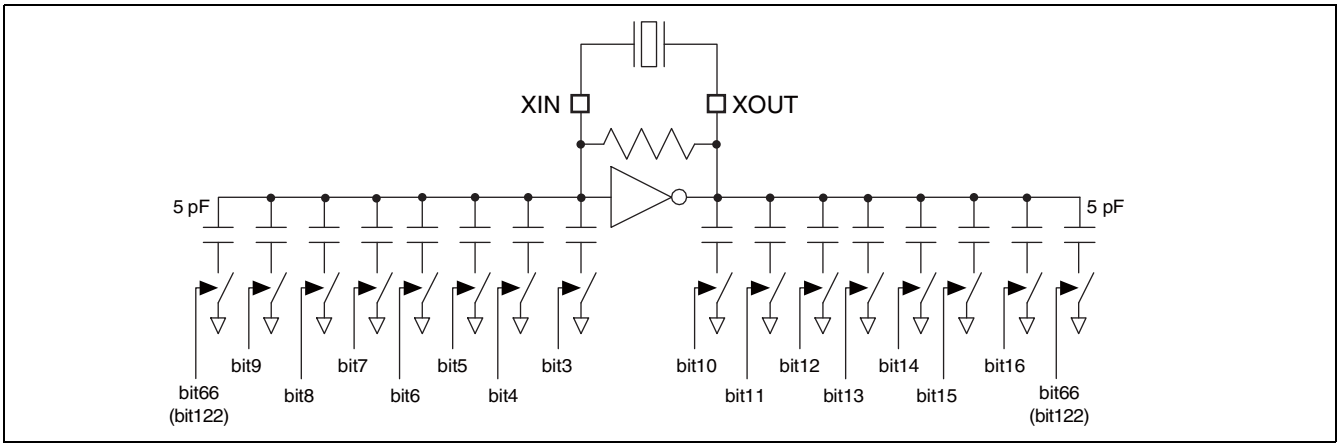
- **Oscillation stabilization capacitance setting**

The capacitance connected to the XIN and the XOUT pins can change from 5 pF to 10 pF by setting bit2 to bit8 and bit9 to bit15 in the memory map (set “1” to bit66 or bit122).

Also, it is possible to cancel the connection whose capacitance is 5 pF for the XIN pin and the XOUT pin by setting bit66 or bit122.

When using the external clock to the clock input, connections for all capacitance need to be cancelled.

XIN	bit67, bit123	bit8	bit7	bit6	bit5	bit4	bit3	bit2	
XOUT		bit15	bit14	bit13	bit12	bit11	bit10	bit9	
Capacitance [pF]	5.000	2.520	1.260	0.630	0.315	0.157	0.079	0.039	Capacitance [pF]
	0	0	0	0	0	0	0	0	0.000
	1	0	0	0	0	0	0	0	5.000
	1	0	0	0	0	0	0	1	5.039
	1	0	0	0	0	0	1	0	5.079
	1	0	0	0	0	0	1	1	5.118
	1	0	0	0	0	1	0	0	5.157
	• • •								—
	1	0	0	0	0	1	1	1	5.275
	1	0	0	0	1	0	0	0	5.315
	• • •								—
	1	0	0	0	1	1	1	1	5.590
	1	0	0	1	0	0	0	0	5.630
	• • •								—
	1	0	0	1	1	1	1	1	6.220
	1	0	1	0	0	0	0	0	6.260
	• • •								—
	1	0	1	1	1	1	1	1	7.480
	1	1	0	0	0	0	0	0	7.520
	• • •								—
	1	1	1	1	1	1	1	1	10.000

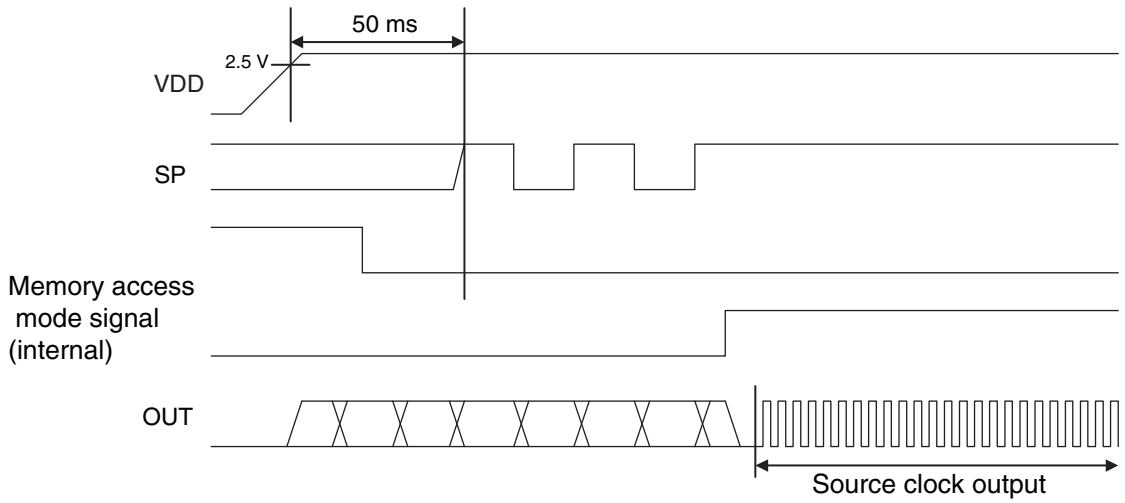


■ MEMORY ACCESS

The non-volatile memory contained in this device can read/write using the serial communication that the SP pin works as the I/O pin.

The communication protocol needs to set LSB first, NRZ format, 8-bit length, no parity and stop bit length 1-bit in the UART asynchronous transfer mode. The transfer speed needs to be set to 1/512 of the device source oscillation.

• **Transfer sequence**



1. More than 50 ms after this device is turned on, input a command from the SP pin and set MB88R157A into memory access mode.(When a command is input by serial communication, data of "FD$_H$" is sent.)

Note: When memory access is available, source clock can be output from the OUT pin.
Fix the SP pin to "H" or "L" until command input.

2. At writing, "00$_H$" is sent serially, and at reading, "40$_H$" is sent serially.

Note: This device needs to stop outputting to the OE pin of the transferred device within 9 µs after transferring "40$_H$" serially at the reading state and place it to a receivable state.

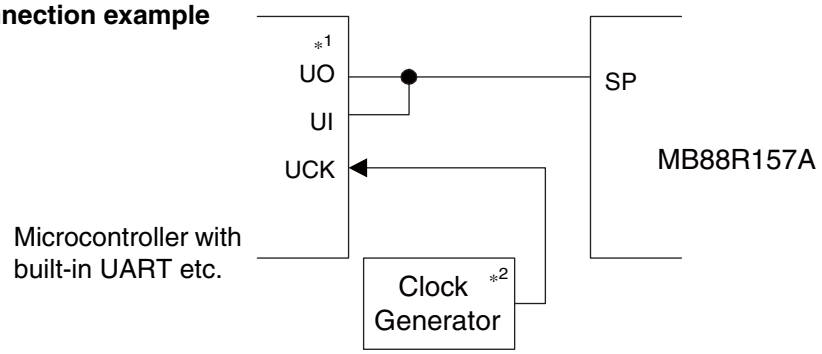
3. At writing : Send 16-byte data blocks from the lower address of the memory map in turn with more than 30 µs between each data block.
At reading : This device outputs 16-byte data blocks from the lower address of the memory map in turn.

Note: 16-byte is required to transfer data even if setting 2 is not used.

4. Repeat the operations of 2. and 3. for re-writing and re-reading.

To operate the device using the written data, turn on the power again.
However, the oscillation stabilization capacitance is set simultaneously with writing to memory. When the oscillation stabilization capacitance and the crystal oscillation frequency are adjusted, change the oscillation stabilization capacitance value so that the clock output from the OUT pin is set to the desired frequency.

• **Interconnection example**



*1: Set the UO pin to Hi-Z to read from memory, as the SP pin serves for serial I/O.
UO : UART serial data output pin
UI : UART serial data input pin
UCK : UART serial synchronous clock I/O pin

*2: Because the transfer rate is set to 1/512 of source oscillation in MB88R157A, the clock generator is used as shown in the figure above. However, the clock generator is not needed if the transfer speed can be maintained from an internal clock of the baud rate generator of the UART.

■ ABSOLUTE MAXIMUM RATINGS

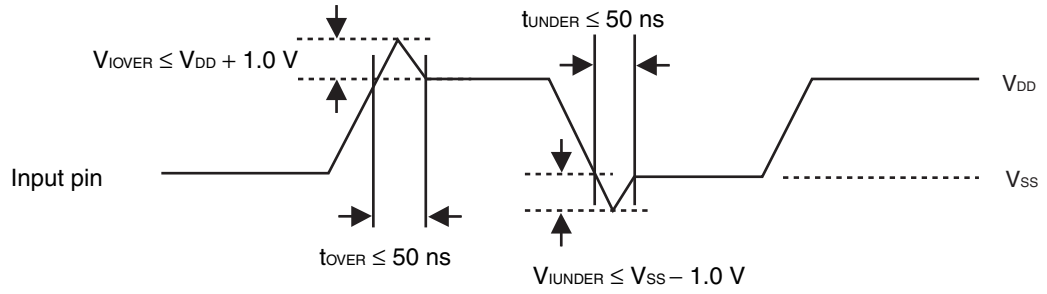
Parameter	Symbol	Rating		Unit
		Min	Max	
Power supply voltage*1	V_{DD}	– 0.5	+ 4.0	V
Input voltage*1	V_I	V_{SS} – 0.5	V_{DD} + 0.5	V
Output voltage*1	V_O	V_{SS} – 0.5	V_{DD} + 0.5	V
Storage temperature*2	T_{ST}	– 55	+ 125	°C
Operation junction temperature*2	T_J	– 40	+ 125	°C
Output current	I_O	– 10	+ 10	mA
Overshoot	V_{IOVER}	—	V_{DD} + 1.0 (t_{OVER} ≤ 50 ns)	V
Undershoot	V_{IUNDER}	V_{SS} – 1.0 (t_{UNDER} ≤ 50 ns)	—	V

*1: This parameter is based on V_{SS} = 0.0 V

*2: Even if the maximum ratings for storage temperature and operation junction temperature are within the temperature conditions, saved data in FRAM is not necessarily guaranteed. Contact the sales representatives for details on data's guarantee outside of the recommended operating conditions.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

Overshoot/Undershoot



■ RECOMMENDED OPERATING CONDITONS

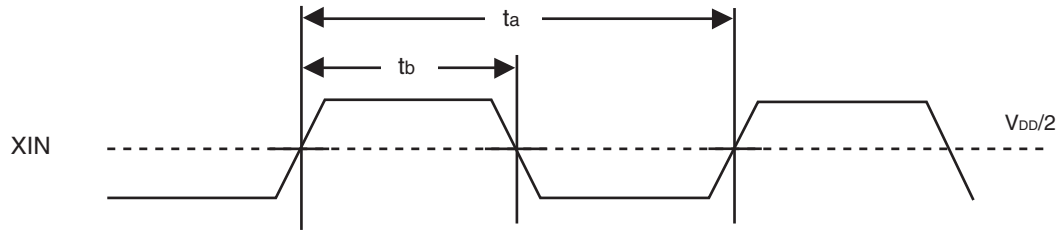
Parameter	Symbol	Pin name	Conditions	Value			Unit
				Min	Typ	Max	
Power supply voltage	V_{DD}	VDD	—	3.0	3.3	3.6	V
"H" level input voltage	V_{IH}	OE, SP, VP	—	$V_{DD} \times 0.8$	—	$V_{DD} + 0.3$	V
"L" level input voltage	V_{IL}			$V_{SS} - 0.3$	—	$V_{DD} \times 0.2$	V
Input clock duty cycle	t_{DCI}	XIN	10 MHz to 50 MHz	40	50	60	%
Operating temperature	T_j	—	Write to the internal non-volatile memory	0	—	+ 50	°C
			First access after the re-flow				
			Other than those above	–20	—	+ 85	

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

Input clock duty cycle ($t_{DCI} = t_b / t_a$)



■ ELECTRICAL CHARACTERISTICS

• **DC Characteristics**

(T_a = − 20 °C to + 85 °C, V_{DD} = 3.3 V ± 0.3 V)

Parameter	Symbol	Pin name	Conditions	Value			Unit
				Min	Typ	Max	
Power supply current	I_{CC}	VDD	24 MHz input (Crystal) , 24 MHz internal oscillation, 24 MHz output no load capacitance	—	5	TBD	mA
	I_{CC2}		Source oscillation 50 MHz input clock, 134 MHz internal oscillation, 134 MHz output 15 pF load capacitance	—	—	TBD	mA
	I_{CCH}		At power down	—	5	TBD	µA
Output voltage	V_{OH}	OUT	"H" level output Driving voltage (low) I_{OH} = –4 mA, Driving voltage (high) I_{OH} = –8 mA	V_{DD} – 0.5	—	V_{DD}	V
	V_{OL}		"L" level output Driving voltage (low) I_{OL} = 4 mA, Driving voltage (high) I_{OL} = 8 mA	V_{SS}	—	0.4	V
Pull-up resistance	R_{PU}	OE, SP	—	20	50	150	kΩ
Input capacitance	C_{IN}	XIN, OE, SP, VF	T_a = + 25 °C, V_{DD} = V_I = 0.0 V, f = 1 MHz	—	—	10	pF

• **AC characteristics (1)**

(T_a = − 20 °C to + 85 °C, V_{DD} = 3.3 V ± 0.3 V)

Parameter	Symbol	Pin name	Conditions	Value			Unit
				Min	Typ	Max	
Crystal oscillation frequency	fx	XIN, XOUT	Fundamental oscillation	10	—	40	MHz
			3rd over-tone	40	—	48	
Input frequency	f_{in}	XIN	—	10	—	50	MHz
Internal oscillation frequency	f_{VCO}	—	—	20	—	134	MHz
Output frequency	f_{OUT}	OUT	—	1	—	134	MHz
Output slewing rate*2	SR		Slewing rate low, Driving ability small, Load capacitance 15pF	0.44	—	—	V/ns
			Slewing rate high, Driving ability small, Load capacitance 15pF	0.47	—	—	
			Slewing rate low, Driving ability large, Load capacitance 15pF	0.79	—	—	
			Slewing rate high, Driving ability large, Load capacitance 15pF	0.90	—	—	
Output impedance	Z_O		Driving ability small	—	58	—	Ω
			Driving ability large	—	29	—	
Output clock duty cycle	t_{DCC}		VCO clock output	40	—	60	%
	t_{DCR}		At reference clock output	T_{DCI} − 10*1	—	T_{DCI} + 10*1	
Modulation frequency (number of input clocks per one modulation)	F_{MOD} (N_{MOD})		—	$f_{in}/(448 \times (L + 1))$ ($448 \times (L + 1)$)	$f_{in}/(532 \times (L + 1))$ ($532 \times (L + 1)$)	$f_{in}/(616 \times (L + 1))$ ($616 \times (L + 1)$)	kHz (clks)
Power supply time	t_R	VDD	0.2 V to 3.0 V	0.05	—	20	ms
Lock-up time	t_{LK}	OUT	At power on, SSCG mode	—	400/fin+6	TBD	ms
			At power on, PLL mode	—	400/fin+2	TBD	
			At power down release, SSCG mode	—	7	TBD	
			At power down release, PLL mode	—	3	TBD	
Cycle-cycle jitter	t_{JC}		No load capacitance, $f_{OUT} \geq 3$ MHz	—	—	TBD	ps-rms
			No load capacitance, $f_{OUT} < 3$ MHz	—	—	TBD	
Output stop time from OE exit.	t_{OD}		$t_a = 1/f_{OUT}$	—	—	$2 \times t_a$	ns
Output start time after OE entry	t_{OE}		$t_a = 1/f_{OUT}$	—	—	$2 \times t_a$	ns

(Continued)

(Continued)

*1: The REFOUT output duty cycle value depends on the duty cycle of input clock t_{DCI}. Either case of A or B will be guaranteed.
A. Resonator : Oscillating correctly with the resonator connected with XIN, XOUT
B. External clock input : The input level is Full - swing (V_{SS} - V_{DD}).

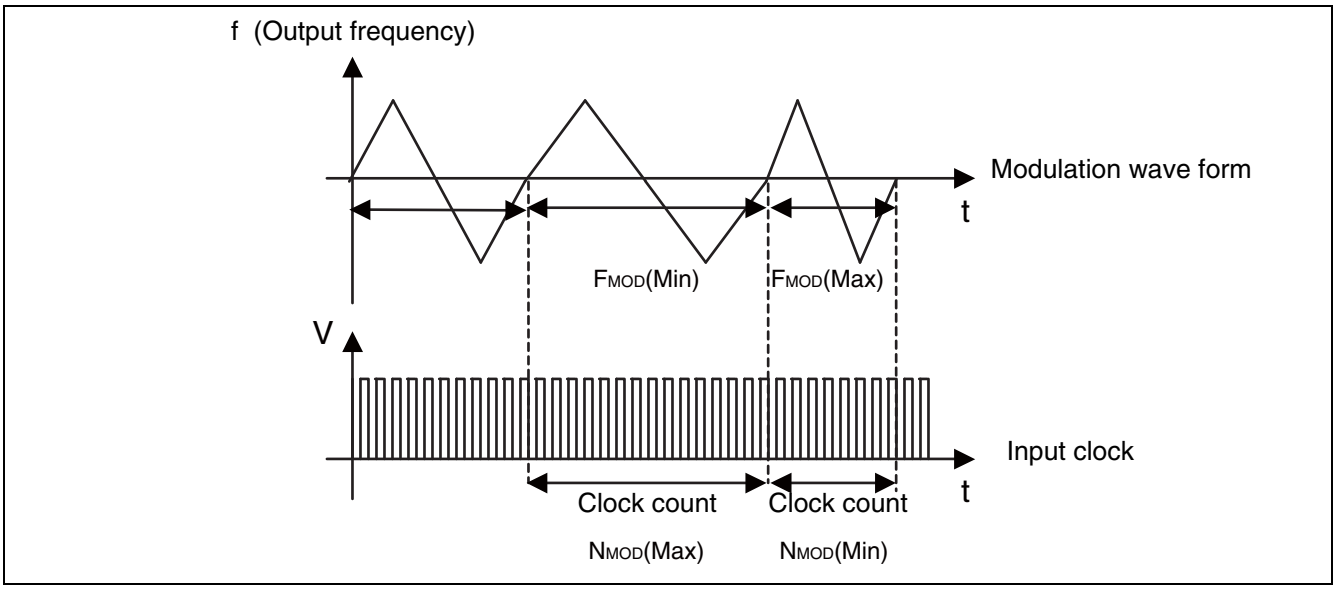
*2: The condition for slew rate measurement is the average value between 0.2 × V_{DD} and 0.8 × V_{DD} when the pin load is 15 pF.

- **AC characteristics (2) (t_r/t_f)**

(Ta = − 20 °C to + 85 °C, V_{DD} = 3.3 V ± 0.3 V)

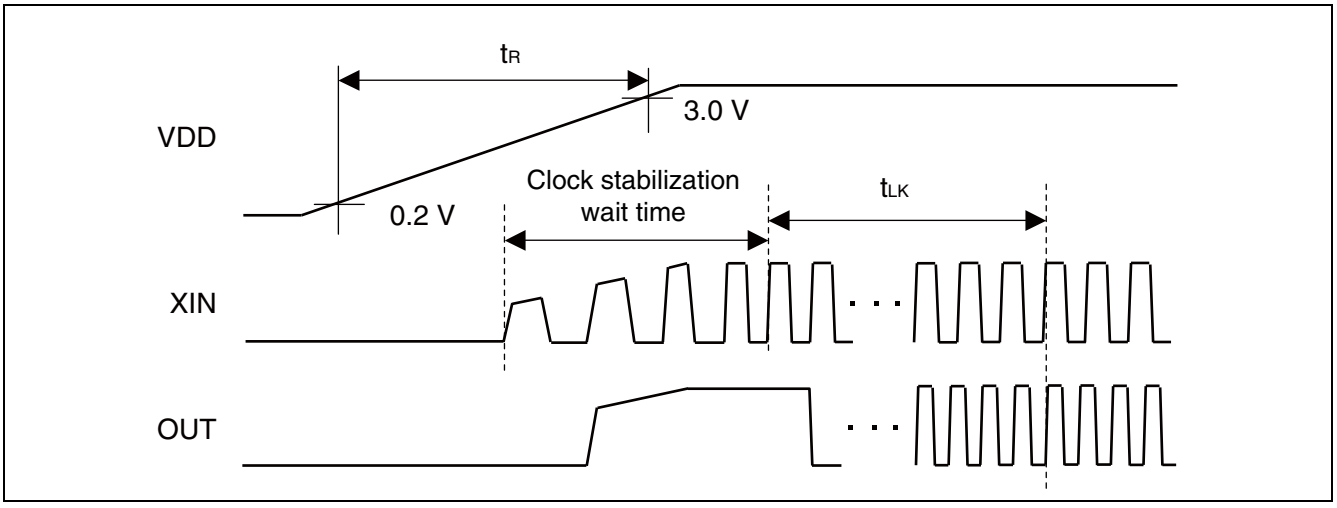
Parameter	Symbol	Pin name	Conditions	Value			Unit
				Min	Typ	Max	
Output clock rising time	t_r	OUT	Slewing rate low, Driving ability small, Load capacitance 15 pF, 0.4 V to 2.4 V	—	—	4.6	ns
			Slewing rate high, Driving ability small, Load capacitance 15 pF, 0.4 V to 2.4 V	—	—	4.3	
			Slewing rate low, Driving ability large, Load capacitance 15 pF, 0.4 V to 2.4 V	—	—	2.6	
			Slewing rate high, Driving ability large, Load capacitance 15 pF, 0.4 V to 2.4 V	—	—	2.3	
Output clock falling time	t_f	OUT	Slewing rate low, Driving ability small, Load capacitance 15 pF, 0.4 V to 2.4 V	—	—	4.6	ns
			Slewing rate high, Driving ability small, Load capacitance 15 pF, 0.4 V to 2.4 V	—	—	4.3	
			Slewing rate low, Driving ability large, Load capacitance 15 pF, 0.4 V to 2.4 V	—	—	2.6	
			Slewing rate high, Driving ability large, Load capacitance 15 pF, 0.4 V to 2.4 V	—	—	2.3	

■ DEFINITION of MODULATION FREQUENCY and NUMBER of INPUT CLOCKS PER MODULATION

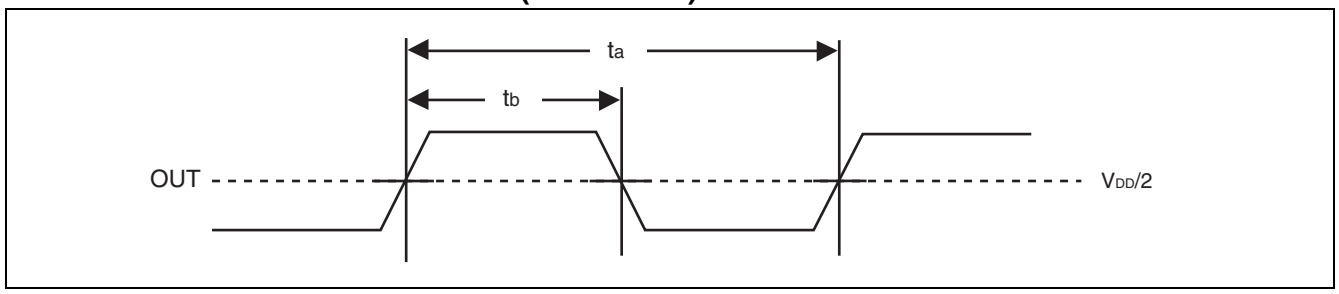


This product contains the modulation period to realize the efficient EMI reduction.
The modulation period F_{MOD} depends on the input frequency and changes between F_{MOD} (Min) and F_{MOD} (Max). Furthermore, the typical value of the electrical characteristics is equivalent to the average value of the modulation period F_{MOD}.

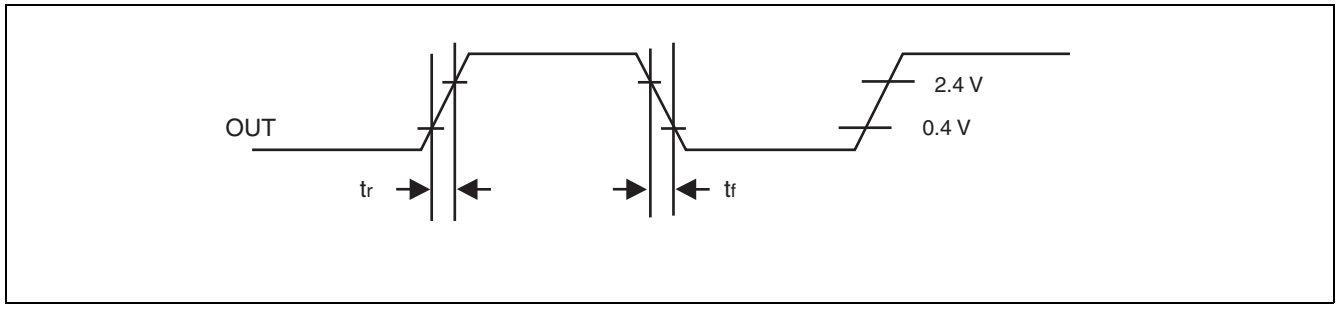
■ TURNING ON POWER SUPPLY AND LOCK-UP TIME



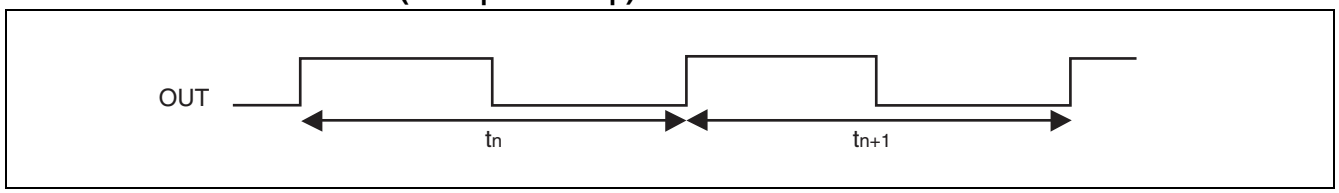
■ OUTPUT CLOCK DUTY CYCLE ($t_{DCC} = t_b / t_a$)



■ RISE AND FALL TIME (t_r/t_f)

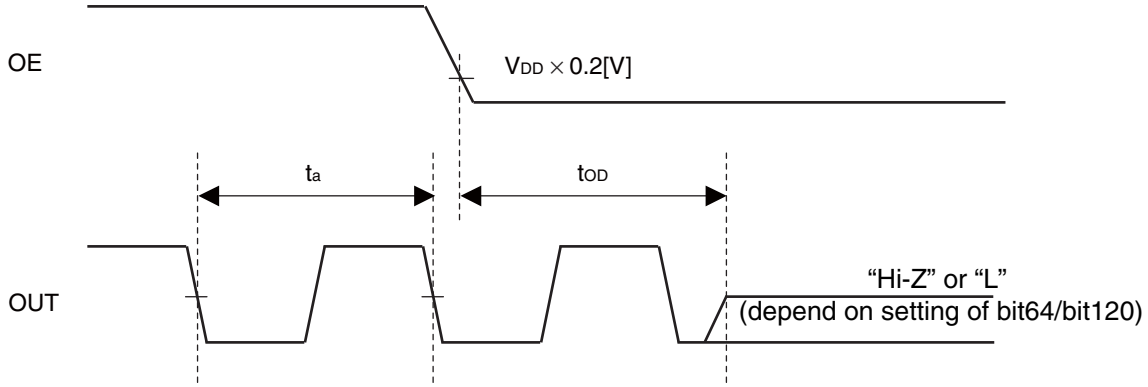


■ CYCLE-CYCLE JITTER ($t_{JC} = | t_n - t_{n+1} |$)

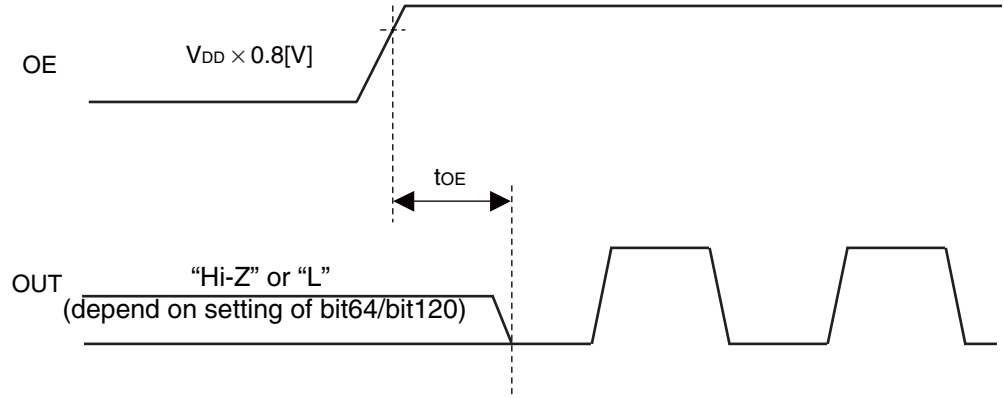


■ OUTPUT TIMING AT OE CHANGE

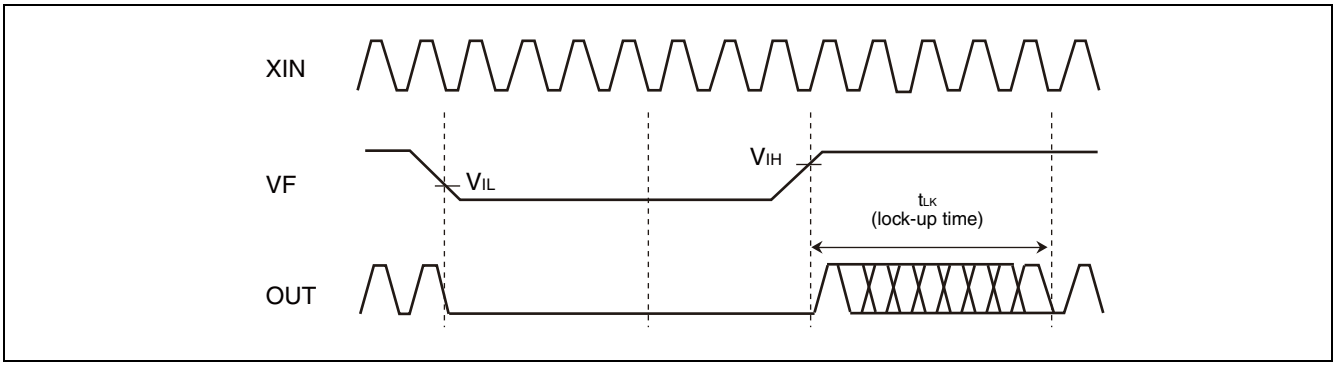
• Output stop time from OE exit



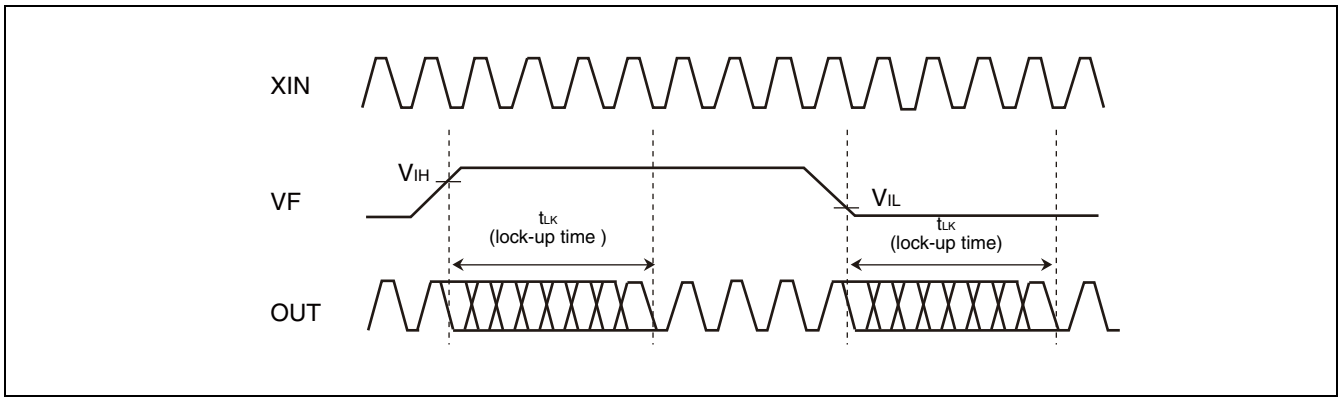
• Output start time after OE entry



■ LOCK-UP TIME



When the power down control by the VF pin is valid and the power down is controlled, the desired clock frequency can be gained once the lock up time t_{LK} has elapsed up to its maximum after the VF pin gets to the H level.



When the modulation control by the VF pin is valid and the modulation is controlled, the frequency set by the OUT pin output can be set once the lock up time t_{LK} has elapsed up to its maximum after the level for the VF pin is decided.

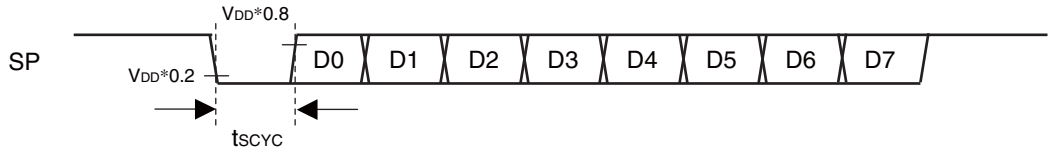
Note: The output frequency, the output clock duty cycle, the modulation cycle and the cycle-cycle jitter cannot be guaranteed until the lock up time has fully elapsed. Therefore, it is recommended to cancel the late reset of the device or execute other means after the lock up time elapses.

- **AC characteristics (3) (Serial interface timing)**

(Ta = − 20 °C to + 85 °C, V_{DD} = 3.3 V ± 0.3 V)

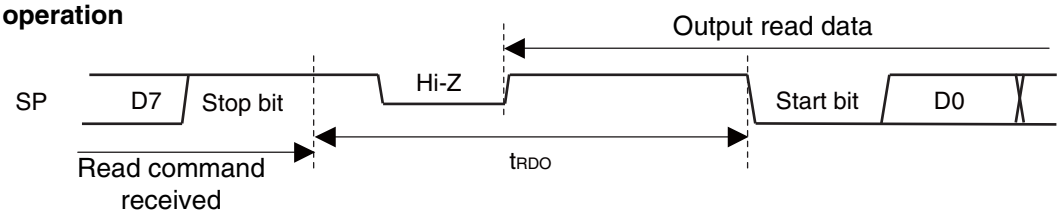
Parameter	Symbol	Pin name	Condi-tions	Value			Unit
				Min	Typ	Max	
Cycle time of transfer and receiver	t_{SCYC}	SP	—	$(t_{in} \times 512) \times 0.95$	$t_{in} \times 512$	$(t_{in} \times 512) \times 1.06$	µs
Command / write data receiver interval	t_{DD}			30	—	—	µs
Read operation Read command receive → SP pin read data output	t_{RDO}			9	—	—	µs
Read operation Final read data output → SP pin input mode exchanged	t_{OTI}			—	—	60	µs

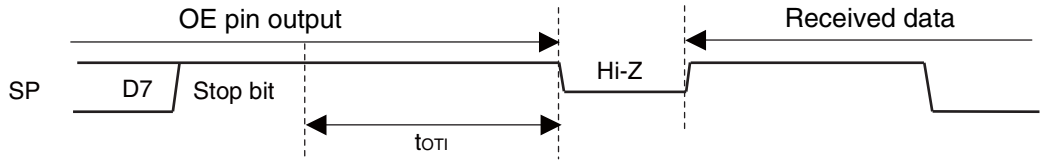
- **Cycle of transfer and receiver**



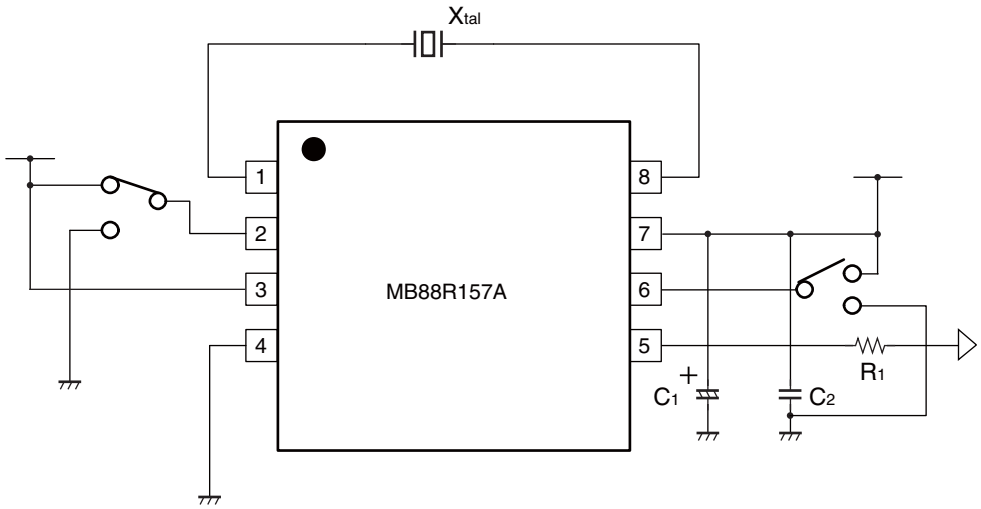
- **Command / write data receiver interval**

- **Read operation**





■ INTERCONNECTION CIRCUIT EXAMPLE



C1 : Tantalum or electrolytic capacitor of 10 μF or higher
C2 : Capacitor of about 0.01 μF (connect a capacitor of good high frequency property (ex. laminated ceramic capacitor) to close to this device)
R1 : Impedance matching resistor for board pattern

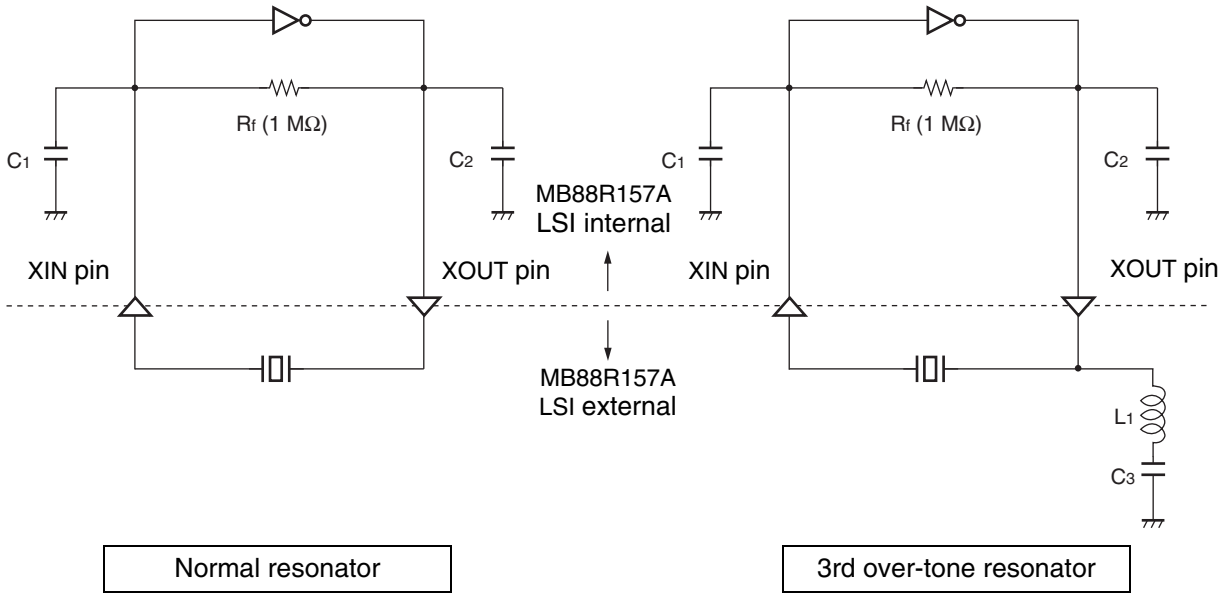
■ CRYSTAL OSCILLATION CIRCUIT

The left hand side figure below shows the connection example about general resonator. The oscillation circuit has the built-in feedback resistor (1 MΩ) and oscillation stabilization capacitance (C_1 and C_2).
C_1 and C_2 value can be changeable by setting bit2 to bit8 and bit9 to bit15 in memory. It is necessary to set suitable parameter for each resonator.

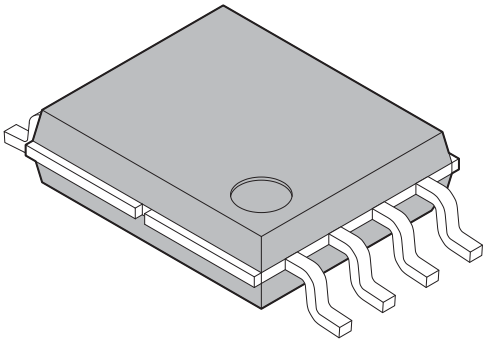
The right hand side figure below shows the connection example for the 3rd overtone oscillation crystal. It is necessary to set the value for capacitance (C_1,C_2,C_3) and inductance (L_1) to suitable parameter for each resonator.

To use an external clock signal (without using the resonator), input the clock signal to the XIN pin with the XOUT pin connected to nothing.

- **When using a resonator**

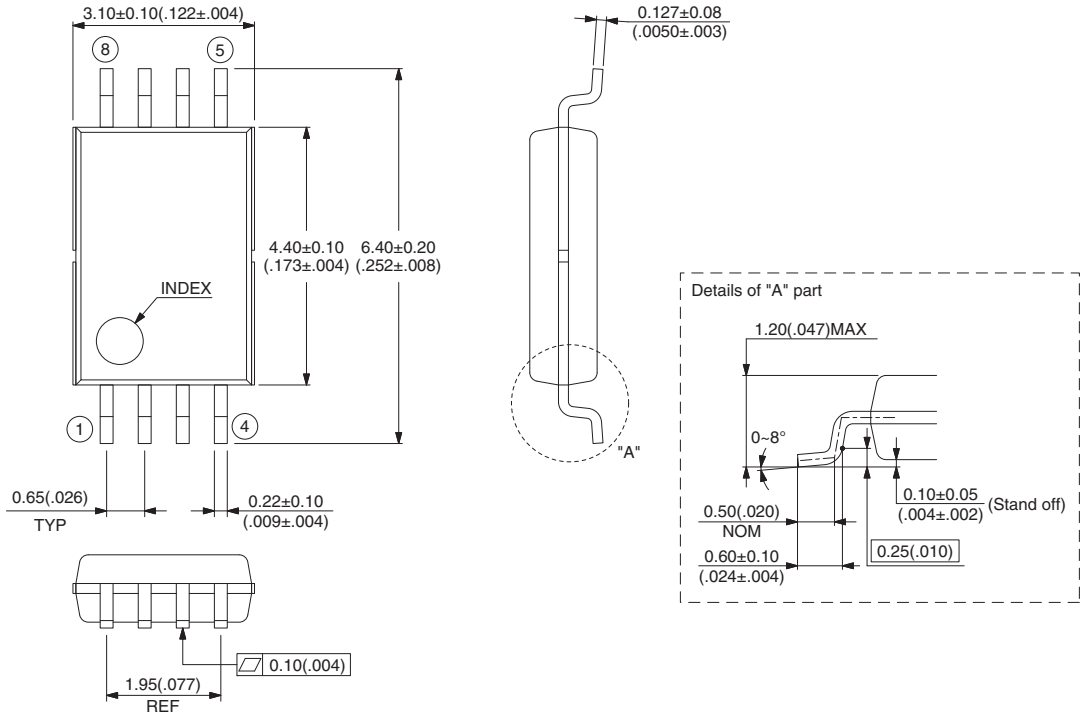


■ PACKAGE DIMENSION

8-pin plastic TSSOP		
 (FPT-8P-M07)	Lead pitch	0.65 mm
	Package width × package length	4.40 mm × 3.10 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.20 mm Max

8-pin plastic TSSOP
(FPT-8P-M07)

Note) Pins width and pins thickness include plating thickness.



Dimensions in mm (inches).
Note: The values in parentheses are reference values

Please check the latest package dimension at the following URL.
http://edevice.fujitsu.com/package/en-search/

MEMO

FUJITSU SEMICONDUCTOR LIMITED

Nomura Fudosan Shin-yokohama Bldg. 10-23, Shin-yokohama 2-Chome,
Kohoku-ku Yokohama Kanagawa 222-0033, Japan
Tel: +81-45-415-5858
http://jp.fujitsu.com/fsl/en/

For further information please contact:

North and South America
FUJITSU SEMICONDUCTOR AMERICA, INC.
1250 E. Arques Avenue, M/S 333
Sunnyvale, CA 94085-5401, U.S.A.
Tel: +1-408-737-5600 Fax: +1-408-737-5999
http://us.fujitsu.com/micro/

Europe
FUJITSU SEMICONDUCTOR EUROPE GmbH
Pittlerstrasse 47, 63225 Langen, Germany
Tel: +49-6103-690-0 Fax: +49-6103-690-122
http://emea.fujitsu.com/semiconductor/

Korea
FUJITSU SEMICONDUCTOR KOREA LTD.
206 Kosmo Tower Building, 1002 Daechi-Dong,
Gangnam-Gu, Seoul 135-280, Republic of Korea
Tel: +82-2-3484-7100 Fax: +82-2-3484-7111
http://kr.fujitsu.com/fmk/

Asia Pacific
FUJITSU SEMICONDUCTOR ASIA PTE. LTD.
151 Lorong Chuan,
#05-08 New Tech Park 556741 Singapore
Tel : +65-6281-0770 Fax : +65-6281-0220
http://www.fujitsu.com/sg/services/micro/semiconductor/

FUJITSU SEMICONDUCTOR SHANGHAI CO., LTD.
Rm. 3102, Bund Center, No.222 Yan An Road (E),
Shanghai 200002, China
Tel : +86-21-6146-3688 Fax : +86-21-6335-1605
http://cn.fujitsu.com/fmc/

FUJITSU SEMICONDUCTOR PACIFIC ASIA LTD.
10/F., World Commerce Centre, 11 Canton Road,
Tsimshatsui, Kowloon, Hong Kong
Tel : +852-2377-0226 Fax : +852-2376-3269
http://cn.fujitsu.com/fmc/en/

Edited: Sales Promotion Department