512Kx32 SRAM MODULE *PRELIMINARY**

FEATURES

- Access Times of 70, 85, 100 and 120nS
- Packaging
  - 66-pin, PGA Type, 1.385 inch square, Hermetic Ceramic HIP (Package 402), SMD Number 5962-94611 (Pending)
  - 68 lead, 40mm Hermetic CQFP, 5.1mm (0.200") (Package 501) SMD Number 5962-95624 (Pending)
  - 68 lead, 40mm Hermetic Low Profile CQFP, 3.5mm (0.140"), (Package 502)
  - 68 lead, Hermetic CQFP (G2), 22mm (0.880 inch) square (Package 500). Designed to fit JEDEC 68 lead 0.990" CQFJ footprint (Fig. 3)
- Organized as 512Kx32, User Configurable as 1024Kx16 or 2Mx8
- Commercial, Industrial and Military Temperature Ranges
- TTL Compatible Inputs and Outputs
- 5 Volt Power Supply
- Low Power CMOS
- Built in Decoupling Caps and Multiple Ground Pins for Low Noise Operation
- Weight
  WS512K32-XHX - 13 grams typical
  WS512K32-XG4X - 20 grams typical

* *This data sheet describes a product under development and is subject to change, without notice*

FIG. 1 PIN CONFIGURATION FOR WS512K32N-XH2X, SMD 5962-94611 (Pending)

TOP VIEW

1	12	23	34	45	56
I/O8	WE2	I/O15	I/O24	VCC	I/O31
I/O9	CS2	I/O14	I/O25	CS4	I/O30
I/O10	GND	I/O13	I/O26	WE4	I/O29
A13	I/O11	I/O12	A8	I/O27	I/O28
A14	A10	OE	A7	A3	A0
A15	A11	A18	NC	A4	A1
A16	A12	WE1	A6	A5	A2
A17	VCC	I/O7	A9	WE3	I/O23
I/O5	CS1	I/O6	I/O16	CS3	I/O22
I/O1	NC	I/O5	I/O17	GND	I/O21
I/O2	I/O3	I/O4	I/O18	I/O19	I/O20
11	22	33	44	55	66

PIN DESCRIPTION

I/O0-31	Data Inputs/Outputs
A0-18	Address Inputs
$\overline{WE}_{1-4}$	Write Enables
$\overline{CS}_{1-4}$	Chip Selects
$\overline{OE}$	Output Enable
VCC	Power Supply
GND	Ground
NC	Not Connected

BLOCK DIAGRAM

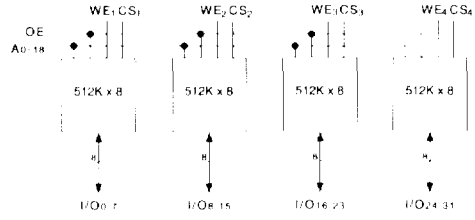
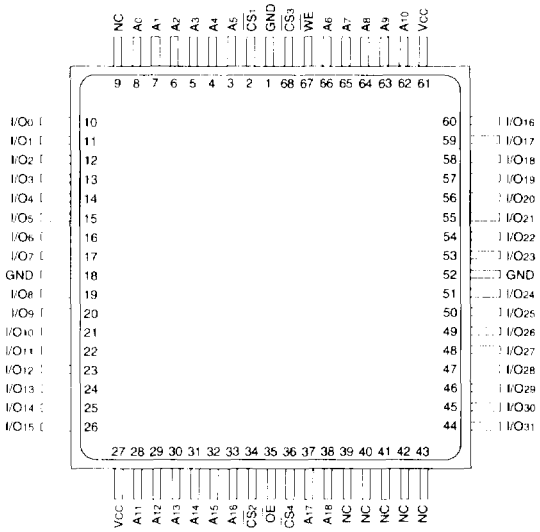


FIG. 2 PIN CONFIGURATION FOR WS512K32-XG4X, SMD 5962-95624 (Pending)

TOP VIEW



PIN DESCRIPTION

I/O0-31	Data Inputs/Outputs
A0-18	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}_{1-4}$	Chip Selects
$\overline{OE}$	Output Enable
V_{CC}	Power Supply
GND	Ground
NC	Not Connected

BLOCK DIAGRAM

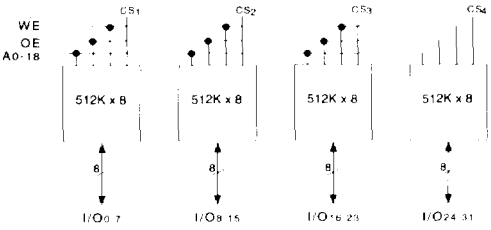
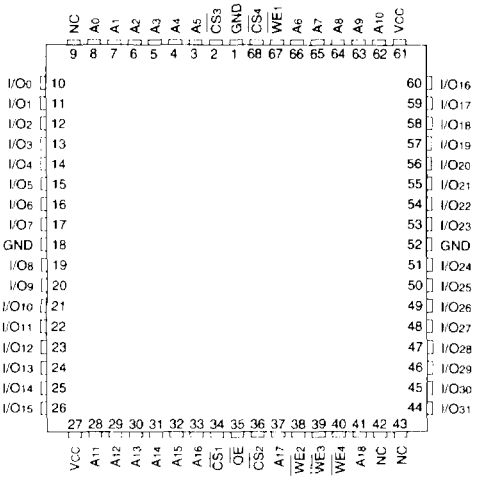
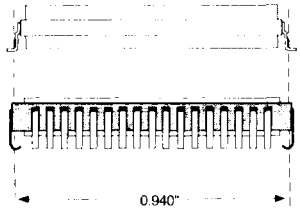


FIG. 3 PIN CONFIGURATION FOR WS512K32-XG2X

TOP VIEW



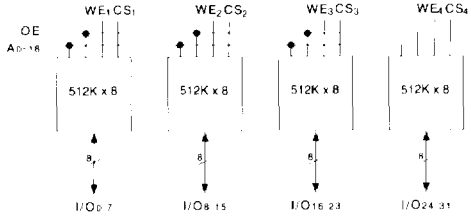


The White 68 lead G2 CQFP fills the same fit and function as the JEDEC 68 lead CQFJ or 68 PLCC. But the G2 has the TCE and lead inspection advantage of the CQFP form.

PIN DESCRIPTION

I/O0-31	Data Inputs/Outputs
A0-18	Address Inputs
$\overline{WE}_{1-4}$	Write Enables
$\overline{CS}_{1-4}$	Chip Selects
$\overline{OE}$	Output Enable
V_{CC}	Power Supply
GND	Ground

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit
Operating Temperature	T_A	-55	+125	°C
Storage Temperature	T_{STG}	-65	+150	°C
Signal Voltage Relative to GND	V_G	-0.5	Vcc+0.5	V
Junction Temperature	T_J		150	°C
Supply Voltage	V_{CC}	-0.5	7.0	V

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{CC}	4.5	5.5	V
Input High Voltage	V_{IH}	2.2	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	-0.5	+0.8	V
Operating Temp (Mil)	T_A	-55	+125	°C

TRUTH TABLE

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	Data I/O	Power
H	X	X	Standby	High Z	Standby
L	L	H	Read	Data Out	Active
L	H	H	Out Disable	High Z	Active
L	X	L	Write	Data In	Active

CAPACITANCE

(T_A = +25°C)

Parameter	Symbol	Conditions	Max	Unit
$\overline{OE}$ capacitance	C_{OE}	V_{IN} = 0 V, f = 1.0 MHz	50	pF
$\overline{WE}_{1-4}$ capacitance	C_{WE}	V_{IN} = 0 V, f = 1.0 MHz		pF
HIP (PGA)			20	
CQFP G4			50	
CQFP G2			20	
$\overline{CS}_{1-4}$ capacitance	C_{CS}	V_{IN} = 0 V, f = 1.0 MHz	20	pF
Data I/O capacitance	$C_{I/O}$	$V_{I/O}$ = 0 V, f = 1.0 MHz	20	pF
Address input capacitance	C_{AD}	V_{IN} = 0 V, f = 1.0 MHz	50	pF

This parameter is guaranteed by design but not tested.

DC CHARACTERISTICS

(V_{CC} = 5.0V, V_{SS} = 0V, T_A = -55°C to +125°C)

Parameter	Symbol	Conditions	Min	Max	Units
Input Leakage Current	I_{LI}	V_{CC} = 5.5, V_{IN} = GND to V_{CC}		10	µA
Output Leakage Current	I_{LO}	$\overline{CS}$ = V_{IH}, $\overline{OE}$ = V_{IH}, V_{OUT} = GND to V_{CC}		10	µA
Operating Supply Current x 32 Mode	$I_{CC \times 32}$	$\overline{CS}$ = V_{IL}, $\overline{OE}$ = V_{IH}, f = 5MHz, V_{CC} = 5.5		200	mA
Standby Current	I_{SB}	$\overline{CS}$ = V_{IH}, $\overline{OE}$ = V_{IH}, f = 5MHz, V_{CC} = 5.5		4.0	mA
Output Low Voltage	V_{OL}	I_{OL} = 2.1mA, V_{CC} = 4.5		0.4	V
Output High Voltage	V_{OH}	I_{OH} = -1.0mA, V_{CC} = 4.5	2.4		V

NOTE: DC test conditions: V_{IH} = V_{CC} -0.3V, V_{IL} = 0.3V

DATA RETENTION CHARACTERISTICS

(T_A = -55°C to +125°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Data Retention Supply Voltage	V_{DR}	$\overline{CS}$ ≥ V_{CC} -0.2V	2.0		5.5	V
Data Retention Current	I_{CCDR1}	V_{CC} = 3V		0.4	1.6	mA

AC CHARACTERISTICS

(V_{CC} = 5.0V, V_{SS} =0V, T_A = -55°C to +125°C)

Parameter Read Cycle	Symbol	-70		-85		-100		-120		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	70		85		100		120		nS
Address Access Time	t_{AA}		70		85		100		120	nS
Output Hold from Address Change	t_{OH}	10		10		10		10		nS
Chip Select Access Time	t_{ACS}		70		85		100		120	nS
Output Enable to Output Valid	t_{OE}		35		35		50		50	nS
Chip Select to Output in Low Z	t_{CLZ}	10		10		10		10		nS
Output Enable to Output in Low Z	t_{OLZ}[1]	5		5		5		5		nS
Chip Disable to Output in High Z	t_{CHZ}		25		25		35		35	nS
Output Disable to Output in High Z	t_{OHZ}[1]		25		25		35		35	nS

1. This parameter is guaranteed by design but not tested.

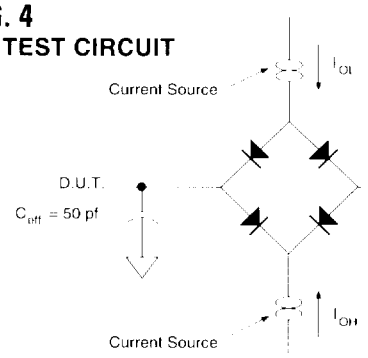
AC CHARACTERISTICS

(V_{CC} = 5.0V, V_{SS} =0V, T_A = -55°C to +125°C)

Parameter Write Cycle	Symbol	-70		-85		-100		-120		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	70		85		100		120		nS
Chip Select to End of Write	t_{CW}	60		60		80		80		nS
Address Valid to End of Write	t_{AW}	60		70		80		80		nS
Data Valid to End of Write	t_{DW}	30		30		40		40		nS
Write Pulse Width	t_{WP}	50		50		60		60		nS
Address Setup Time	t_{AS}	0		0		0		0		nS
Address Hold Time	t_{AH}	5		5		5		5		nS
Output Active from End of Write	t_{OW}	5		5		5		5		nS
Write Enable to Output in High Z	t_{WHZ}		25		25		35		35	nS
Data Hold from Write Time	t_{DH}	0		0		0		0		nS

1. This parameter is guaranteed by design but not tested.

FIG. 4
AC TEST CIRCUIT



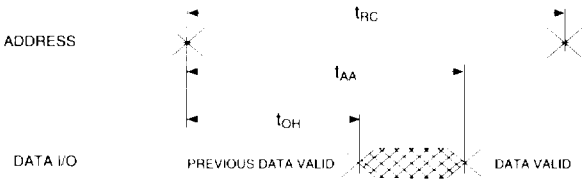
V_Z = 1.5V
(Bipolar Supply)

AC TEST CONDITIONS

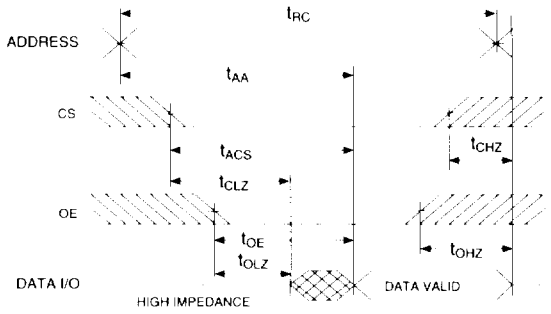
Parameter	Typ	Unit
Input Pulse Levels	V_{IL} = 0, V_{IH} = 3.0	V
Input Rise and Fall	5	nS
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

NOTES:
V_Z is programmable from -2V to +7V.
I_{OL} & I_{OH} programmable from 0 to 16mA
Tester Impedance: Z_0 = 75 Ω
V_Z is typically the midpoint of V_{OH} and V_{IH}
I_{OL} & I_{OH} are adjusted to simulate a typical resistive load circuit.
ATE tester includes jig capacitance.

FIG. 5
TIMING WAVEFORM - READ CYCLE



READ CYCLE 1 (CS = OE = V_{IL}, WE = V_{IH})



READ CYCLE 2 (WE = V_{IH})

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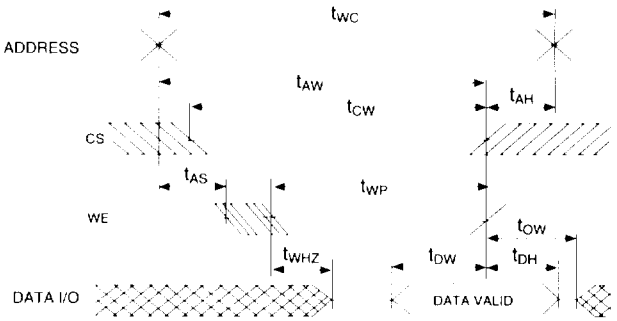
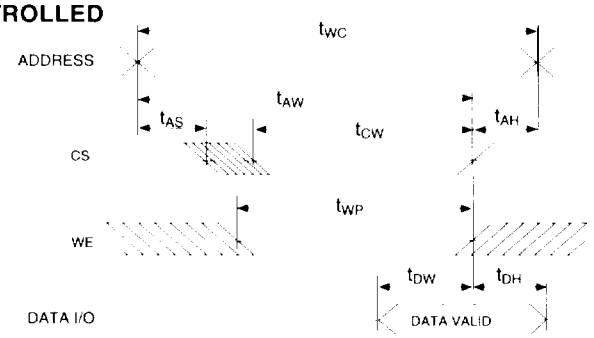
FIG. 6
WRITE CYCLE - $\overline{WE}$ CONTROLLED



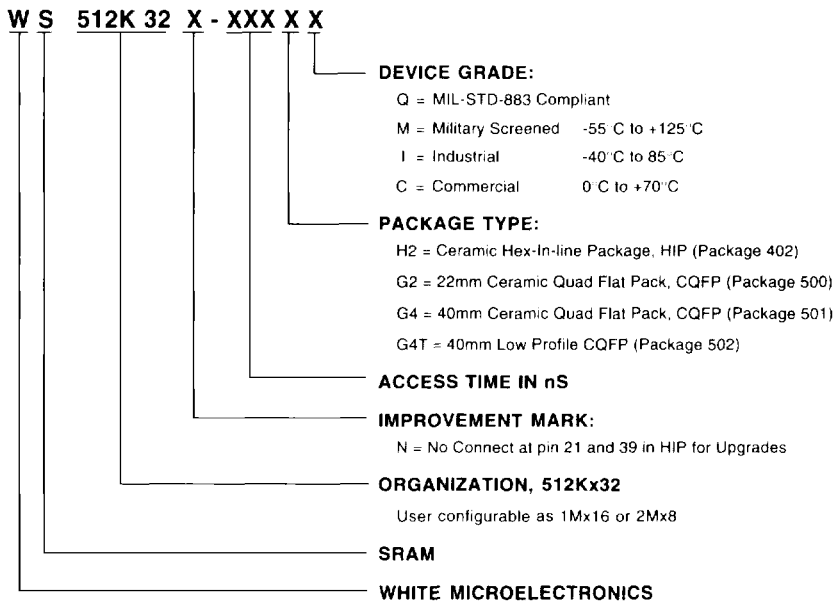
WRITE CYCLE 1, WE CONTROLLED (OE = V_{IH})

FIG. 7
WRITE CYCLE - $\overline{CS}$ CONTROLLED



WRITE CYCLE 2, CS CONTROLLED (OE = V_{IH})

ORDERING INFORMATION



Device Type	Speed	Package	SMD Number
512K x 32 SRAM Module	120nS	66 pin HIP	5962-94611 01HXX*
512K x 32 SRAM Module	**100nS**	**66 pin HIP**	**5962-94611 02HXX***
512K x 32 SRAM Module	85nS	66 pin HIP	5962-94611 03HXX*
512K x 32 SRAM Module	70nS	66 pin HIP	5962-94611 04HXX*
512K x 32 SRAM Module	120nS	68 pin CQFP	5962-95624 01HXX*
512K x 32 SRAM Module	**100nS**	**68 pin CQFP**	**5962-95624 02HXX***
512K x 32 SRAM Module	85nS	68 pin CQFP	5962-95624 03HXX*
512K x 32 SRAM Module	70nS	68 pin CQFP	5962-95624 04HXX*

* Pending