

Document Title

8Mb SyncBurst Pipelined SRAM

Revision History

<u>Revision No</u>	<u>History</u>	<u>Draft Date</u>	<u>Remark</u>
0A	Initial Draft	September 24,2001	
0B	1. Move the \overline{FT} pin for user-configurable Flow through or pipelined operation, That pin can be NC or connected to Vcc for pipelined operation. Refer to Pin configuration. 2. Revise the power supply characteristics at page 12 3. Revise the t_{kq} of 250 MHZ from 2.5ns to 3ns. 4. Move the 100 MHZ speed grade.	August 13,2002	

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256K x 32, 256K x 36, 512K x 18 8Mb S/DCD SYNCBURST Pipelined SRAMs

FEATURES

- Pipeline Mode operation
- Single/Dual Cycl Deselect
- User-selectable Output Drive Strength with XQ Mode
- Internal self-timed write cycle
- Individual Byte Write Control and Global Write
- Clock controlled, registered address, data and control
- Pentium™ or linear burst sequence control using MODE input
- Common data inputs and data outputs
- JEDEC 100-Pin TQFP and 119-pin PBGA package
- Single +3.3V, +10%, -5% core power supply
- Power-down snooze mode
- 2.5V or 3.3V I/O Supply
- Snooze MODE for reduced-power standby
- T version (three chip selects)
- D version (two chip selects)

DESCRIPTION

ICSI's 8Mb SyncBurst Pipelined SRAMs integrate a 512k x 18, 256k x 32, or 256k x 36 SRAM core with advanced synchronous peripheral circuitry and a 2-bit burst counter.

Applications

The ICSI SyncBurst Pipelined SRAM family employs high-speed, low-power CMOS designs that are fabricated using an advanced CMOS process to provide Level 2 Cache applications supporting Pentium and PowerPC microprocessors originally, the device now finds application ranging from DSP main store to networking chip set support.

FAST ACCESS TIME

	Symbol	-250	-200	-166	-133	Units
Pipeline	tkq	3	3.1	3.5	4	ns
3-1-1-1	tkc	4	5	6	7.5	ns
	lcc1	390	360	330	300	mA

Controls

All synchronous inputs pass through registers controlled by a positive-edge-triggered single clock input. Bursts can be initiated with either ADSP (Address Status Processor) or ADSC (Address Status Cache Controller) input pins. Subsequent burst addresses can be generated internally and controlled by the ADV (burst address advance) input pin. The mode pin is used to select the burst sequence order, Linear burst is achieved when this pin is tied LOW. Interleave burst is achieved when this pin is tied HIGH or left floating.

SCD and DCD Pipelined Reads

The device is a SCD (Single Cycle Deselect) and DCD (Dual Cycle Deselect) pipelined synchronous SRAM. DCD SRAMs pipeline disable commands to the same degree as read commands. SCD SRAMs pipeline deselect commands one stage less than read commands. SCD RAMs begin turning off their outputs immediately after the deselect command has been captured in the input registers. DCD RAMs hold the deselect command for one full cycle and then begin turning off their outputs just after the second rising edge of clock. The user may configure this SRAM for either mode of operation using the SCD mode input on Bump 4L.

Byte Write and Global Write

Write cycles are internally self-timed and are initiated by the rising edge of the clock input. Write cycles can be from one to four bytes wide as controlled by the write control inputs. Separate byte enables allow individual bytes to be written. Byte write operation is performed by using byte write enable (\overline{BWE}) input combined with one or more individual byte write signals (BWx). In addition, Global Write (\overline{GW}) is available for writing all bytes at one time, regardless of the byte write controls.

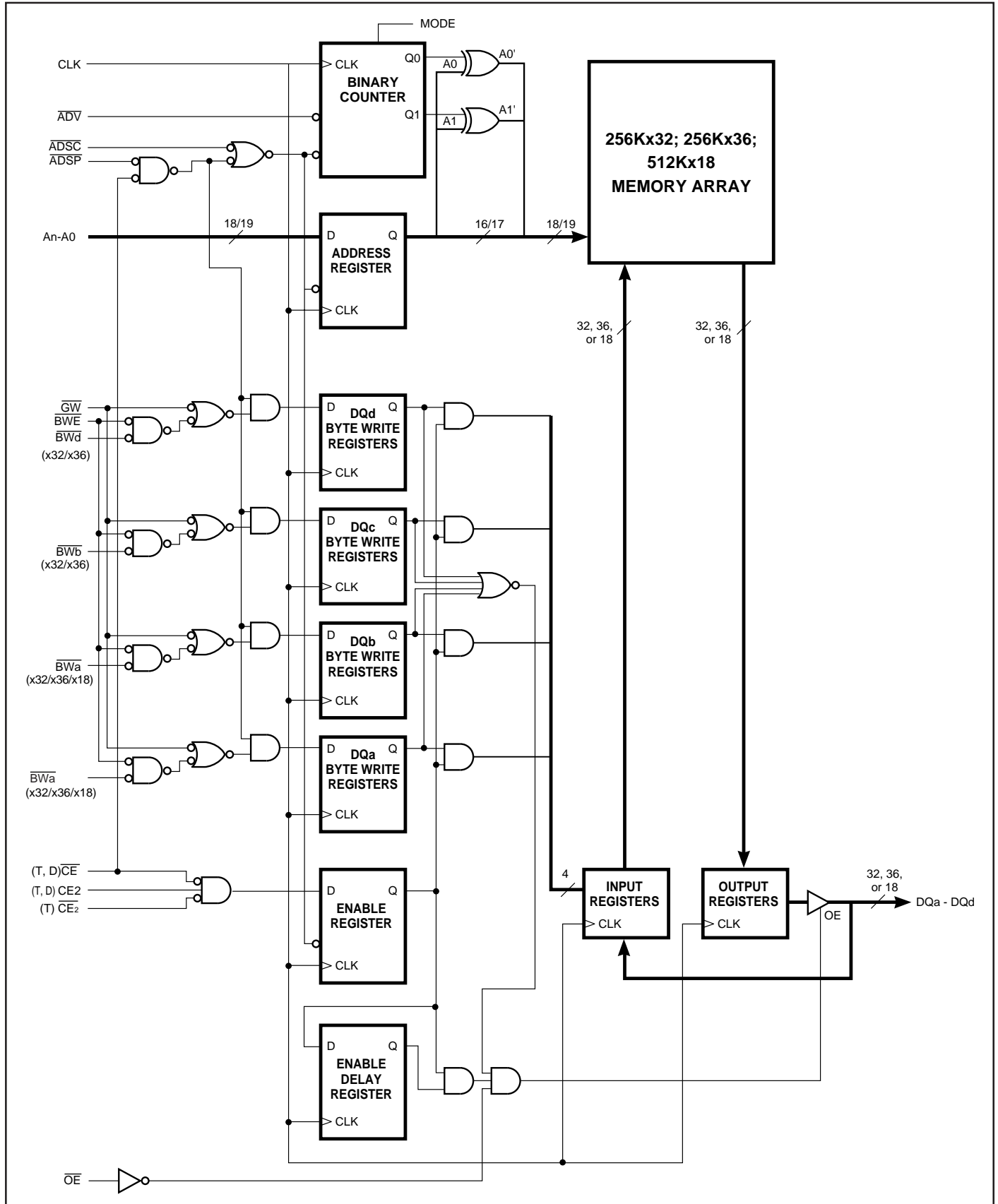
IOL/IOH Drive strength Options

The XQ pin allows selection between high drive strength (XQ low) for multi-drop bus applications and normal drive strength (XQ floating or high) point-to-point applications. See the Output Driver Characteristics chart for details.

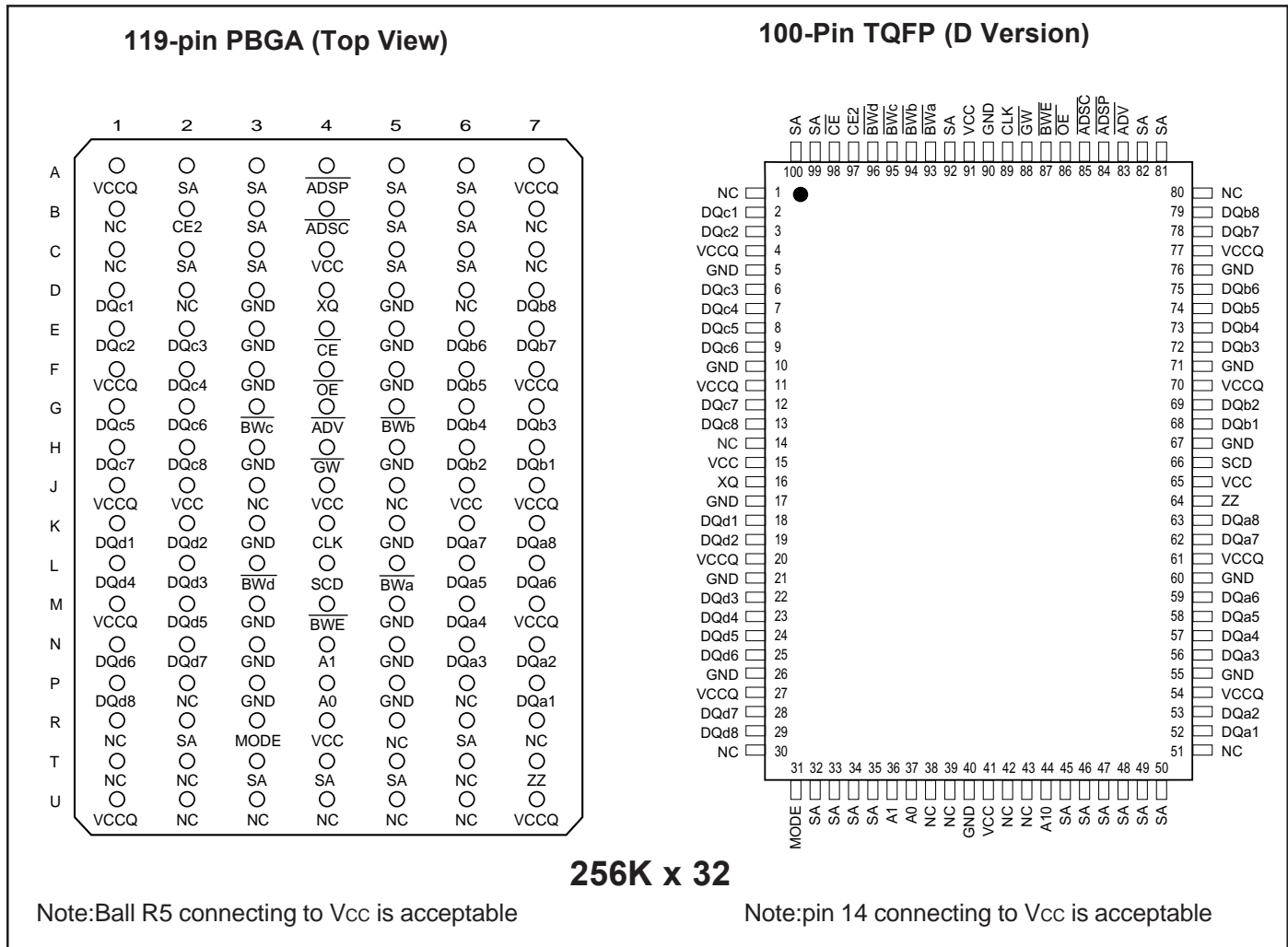
Snooze Mode

Low power (Snooze mode) is attained through the assertion (High) of the ZZ signal, or by stopping the clock (CK). Memory data is retained during Snooze mode.

BLOCK DIAGRAM



PIN CONFIGURATION

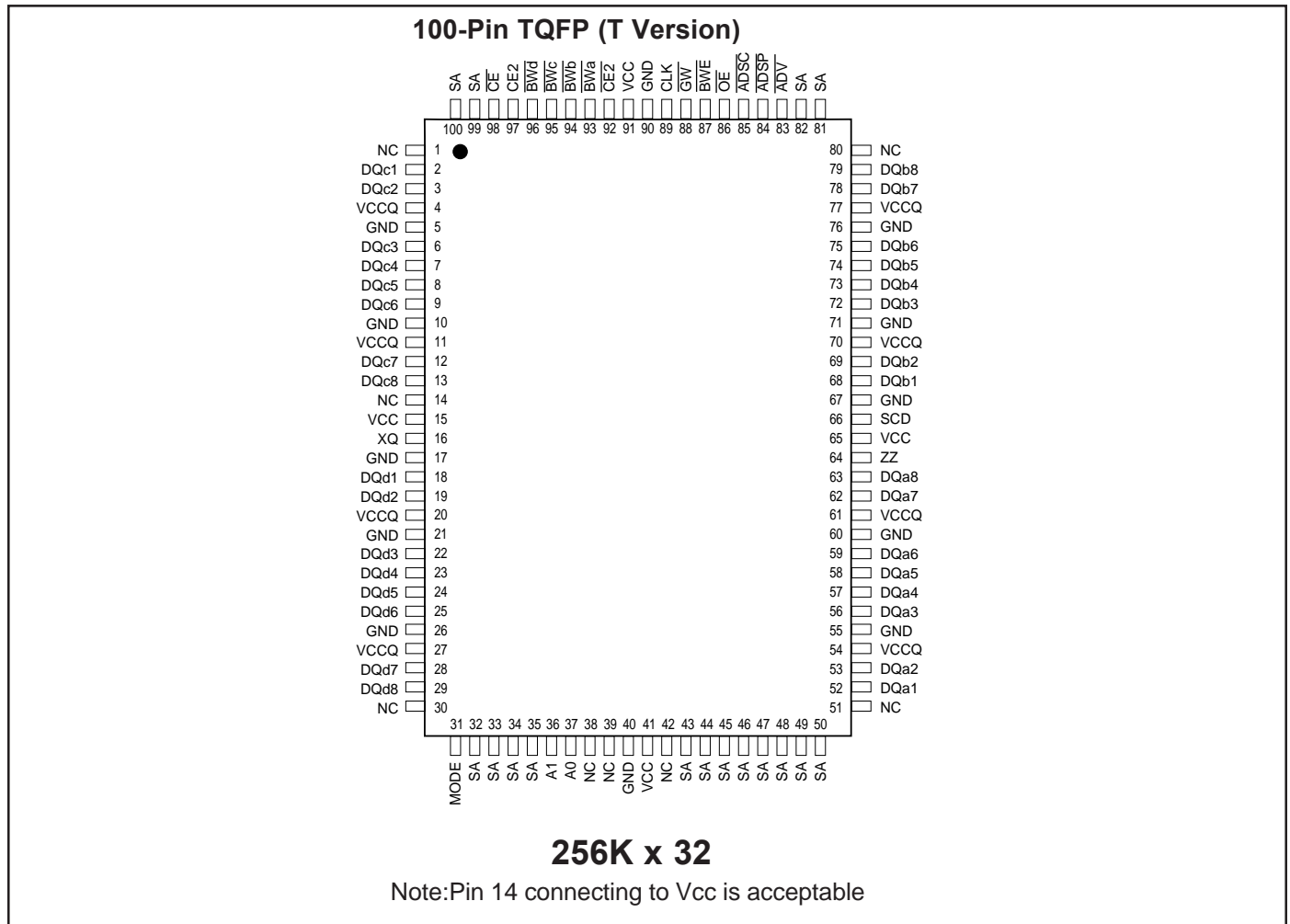


PIN DESCRIPTIONS

A0, A1	Synchronous Address Inputs. These pins must tied to the two LSBs of the address bus.
A2-A17	Synchronous Address Inputs
CLK	Synchronous Clock
ADSP	Synchronous Processor Address Status
ADSC	Synchronous Controller Address Status
ADV	Synchronous Burst Address Advance
BWa -BWd	Synchronous Byte Write Enable
BWE	Synchronous Byte Write Enable
GW	Synchronous Global Write Enable
CE , CE2	Synchronous Chip Enable
OE	Output Enable

DQa-DQd	Synchronous Data Input/Output
MODE	Burst Sequence Mode Selection
SCD	Single Cycle Deselect/Dual Cycle Deselect Mode Control
XQ	Output Drive Control
Vcc	+3.3V Power Supply
GND	Ground
Vccq	Isolated Output Buffer Supply : +3.3V or 2.5V
ZZ	Snooze Enable

PIN CONFIGURATION

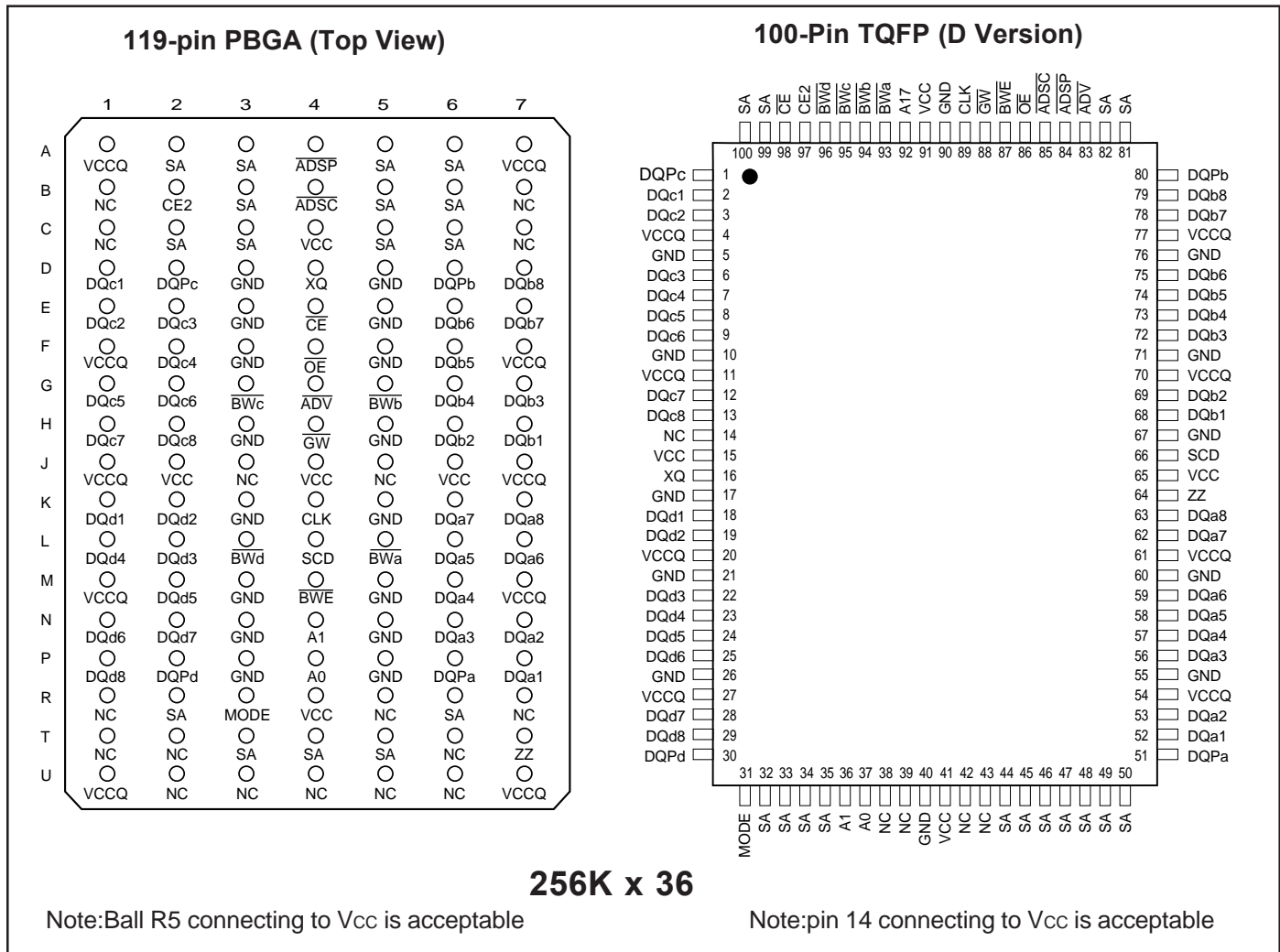


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GW	Synchronous Global Write Enable
CE,CE2,CE2	Synchronous Chip Enable
OE	Output Enable

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SCD	Single Cycle Deselect/Dual Cycle Deselect Mode Control
XQ	Output Drive Control
Vcc	+3.3V Power Supply
GND	Ground
Vccq	Isolated Output Buffer Supply : +3.3V or 2.5V
ZZ	Snooze Enable

PIN CONFIGURATION

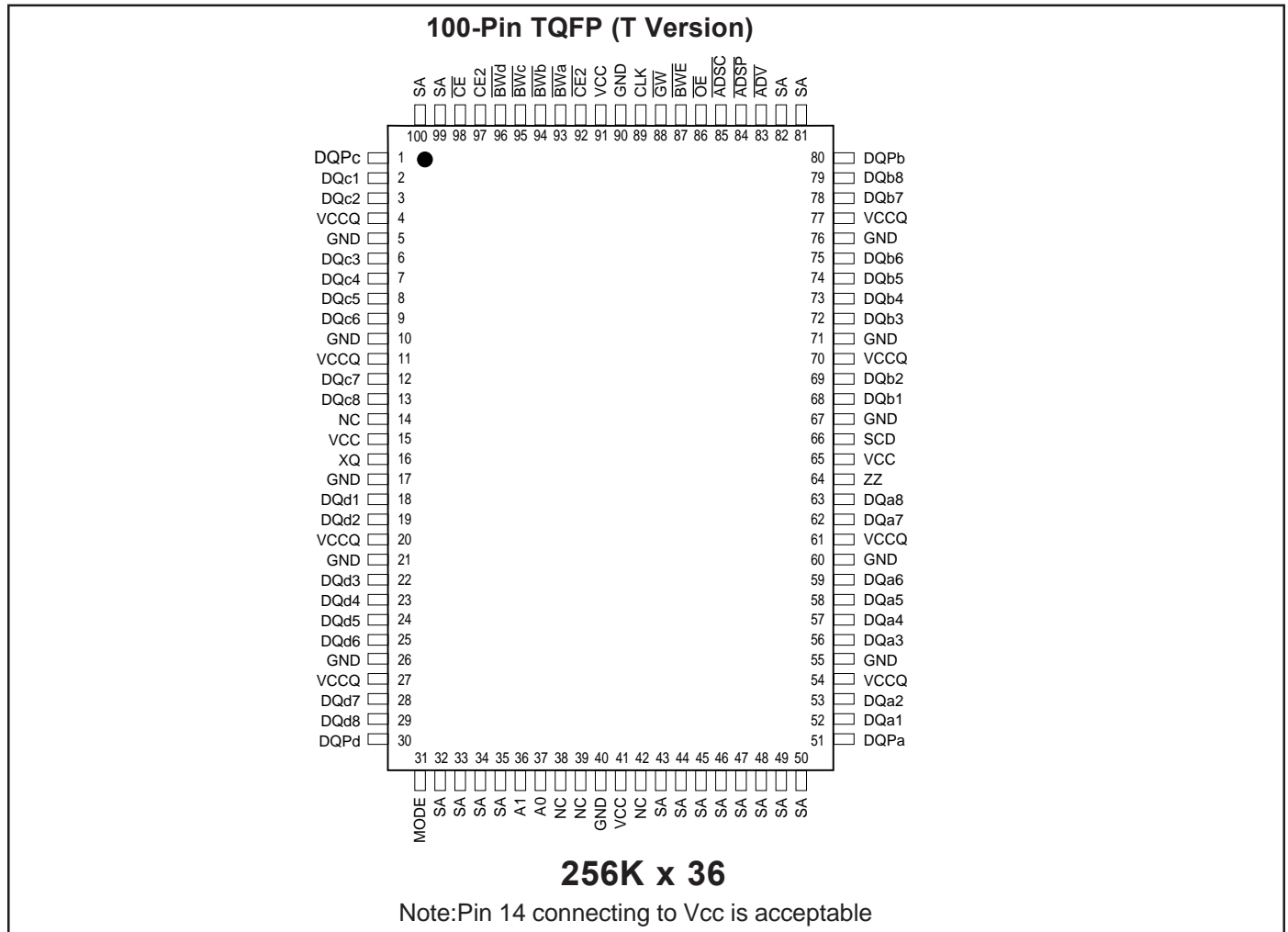


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SCD	Single Cycle Deselect/Dual Cycle Deselect Mode Control
XQ	Output Drive Control
Vcc	+3.3V Power Supply
GND	Ground
Vccq	Isolated Output Buffer Supply : +3.3V or 2.5V
ZZ	Snooze Enable
DQPd-DQPd	Parity Data I/O

PIN CONFIGURATION

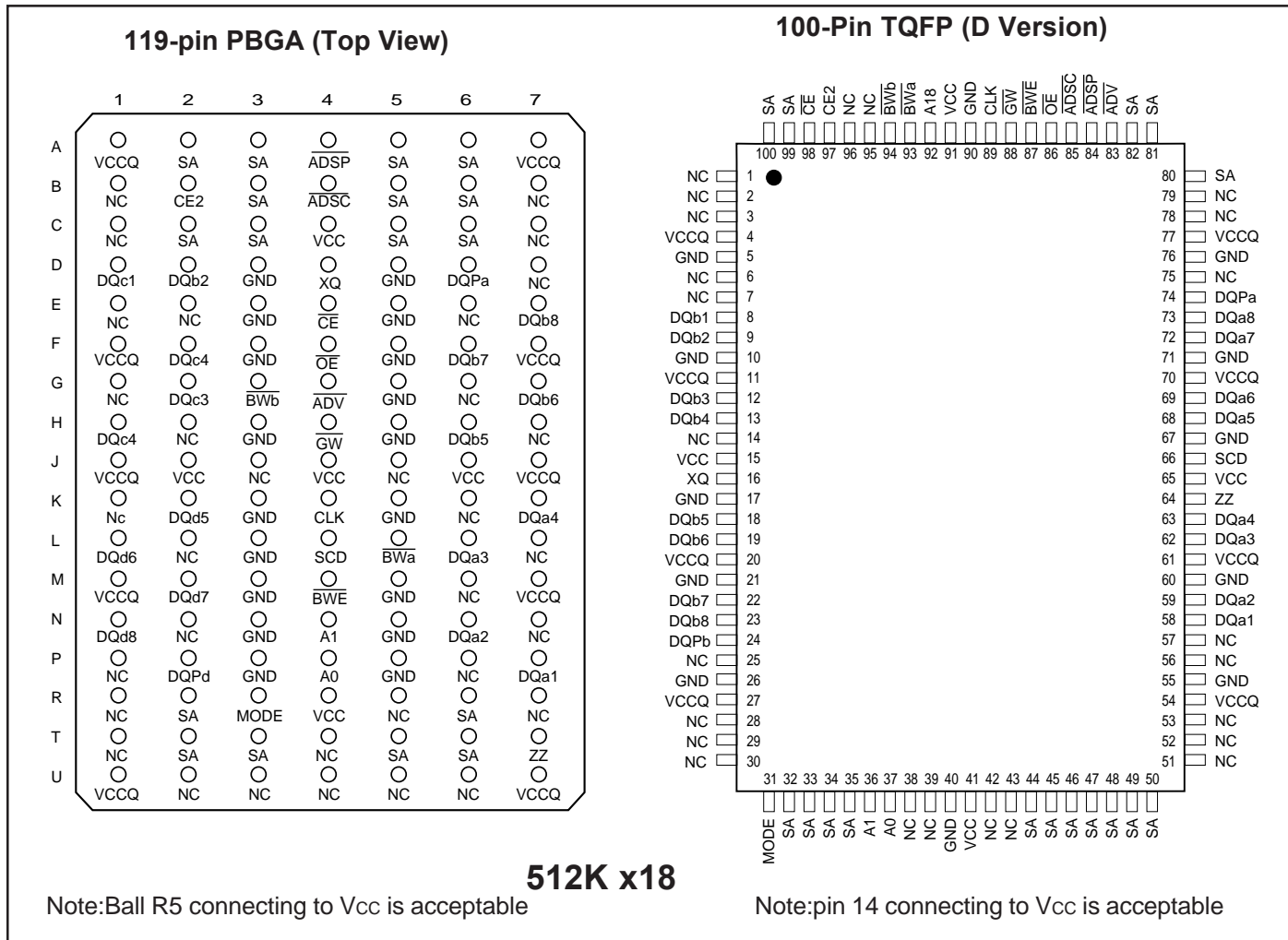


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BWE	Synchronous Byte Write Enable
GW	Synchronous Global Write Enable
CE,CE2,CE2	Synchronous Chip Enable
OE	Output Enable

DQa-DQd	Synchronous Data Input/Output
MODE	Burst Sequence Mode Selection
SCD	Single Cycle Deselect/Dual Cycle Deselect Mode Control
XQ	Output Drive Control
Vcc	+3.3V Power Supply
GND	Ground
Vccq	Isolated Output Buffer Supply : +3.3V or 2.5V
ZZ	Snooze Enable
DQPa-DQPd	Parity Data I/O

PIN CONFIGURATION

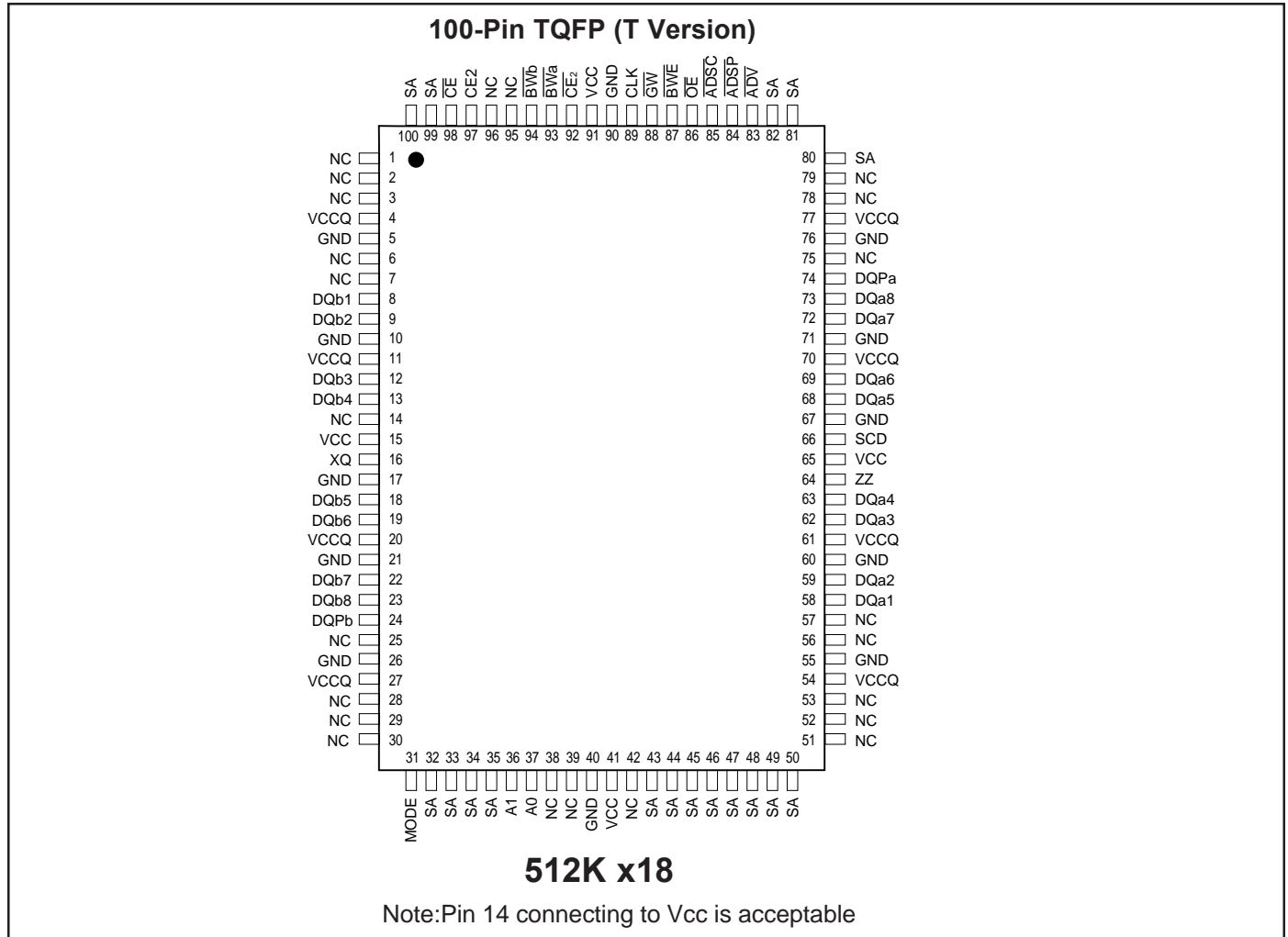


PIN DESCRIPTIONS

A0, A1	Synchronous Address Inputs. These pins must tied to the two LSBs of the address bus.
A2-A18	Synchronous Address Inputs
CLK	Synchronous Clock
ADSP	Synchronous Processor Address Status
ADSC	Synchronous Controller Address Status
ADV	Synchronous Burst Address Advance
BW _a -BW _b	Synchronous Byte Write Enable
BWE	Synchronous Byte Write Enable
GW	Synchronous Global Write Enable
CE , CE2	Synchronous Chip Enable
OE	Output Enable

DQ _a -DQ _b	Synchronous Data Input/Output
MODE	Burst Sequence Mode Selection
SCD	Single Cycle Deselect/Dual Cycle Deselect Mode Control
XQ	Output Drive Control
V _{cc}	+3.3V Power Supply
GND	Ground
V _{ccq}	Isolated Output Buffer Supply : +3.3V or 2.5V
ZZ	Snooze Enable
DQP _a -DQP _b	Parity Data I/O DQP _a is parity for DQ _a 1-8;DQP _b is parity for DQ _b 1-8

PIN CONFIGURATION



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BWa -BWb	Synchronous Byte Write Enable
BWE	Synchronous Byte Write Enable
GW	Synchronous Global Write Enable
CE,CE2,CE2	Synchronous Chip Enable
OE	Output Enable

DQa-DQb	Synchronous Data Input/Output
MODE	Burst Sequence Mode Selection
SCD	Single Cycle Deselect/Dual Cycle Deselect Mode Control
XQ	Output Drive Control
Vcc	+3.3V Power Supply
GND	Ground
Vccq	Isolated Output Buffer Supply : +3.3V or 2.5V
ZZ	Snooze Enable
DQPa-DQ Pb	Parity Data I/O DQPa is parity for DQa1-8;DQ Pb is parity for DQb1-8

Mode Pin Functions

Mode Name	Pin Name	State	Function
Burst Order Control	MODE	L	Linear Burst
		H or NC	Interleaved Burst
Power Down Control	ZZ	L or NC	Active
		H	Standby
Single/Dual Cycle Deselect Control	SCD	L	Dual Cycle Deselect
		H or NC	Single Cycle Deselect
Output Drive Control	XQ	L	High Drive (Low Impedance)
		H	Low Drive (High Impedance)

Note:
There are pull-up devices on the MODE, XQ, and SCD pins and a pull down device on the ZZ pin, so those input pins can be unconnected and the chip will operate in the default states as specified in the above table.

TRUTH TABLE

Operation	Address									
	Used	\overline{CE}	CE2	$\overline{CE2}$	\overline{ADSP}	\overline{ADSC}	\overline{ADV}	\overline{WRITE}	\overline{OE}	DQ
Deselected, Power-down	None	H	X	X	X	L	X	X	X	High-Z
Deselected, Power-down	None	L	X	H	L	X	X	X	X	High-Z
Deselected, Power-down	None	L	L	X	L	X	X	X	X	High-Z
Deselected, Power-down	None	L	X	H	H	L	X	X	X	High-Z
Deselected, Power-down	None	L	L	X	H	L	X	X	X	High-Z
Read Cycle, Begin Burst	External	L	H	L	L	X	X	X	X	Q
Read Cycle, Begin Burst	External	L	H	L	H	L	X	Read	X	Q
Write Cycle, Begin Burst	External	L	H	L	H	L	X	Write	X	D
Read Cycle, Continue Burst	Next	X	X	X	H	H	L	Read	L	Q
Read Cycle, Continue Burst	Next	X	X	X	H	H	L	Read	H	High-Z
Read Cycle, Continue Burst	Next	H	X	X	X	H	L	Read	L	Q
Read Cycle, Continue Burst	Next	H	X	X	X	H	L	Read	H	High-Z
Write Cycle, Continue Burst	Next	X	X	X	H	H	L	Write	X	D
Write Cycle, Continue Burst	Next	H	X	X	X	H	L	Write	X	D
Read Cycle, Suspend Burst	Current	X	X	X	H	H	H	Read	L	Q
Read Cycle, Suspend Burst	Current	X	X	X	H	H	H	Read	H	High-Z
Read Cycle, Suspend Burst	Current	H	X	X	X	H	H	Read	L	Q
Read Cycle, Suspend Burst	Current	H	X	X	X	H	H	Read	H	High-Z
Write Cycle, Suspend Burst	Current	X	X	X	H	H	H	Write	X	D
Write Cycle, Suspend Burst	Current	H	X	X	X	H	H	Write	X	D

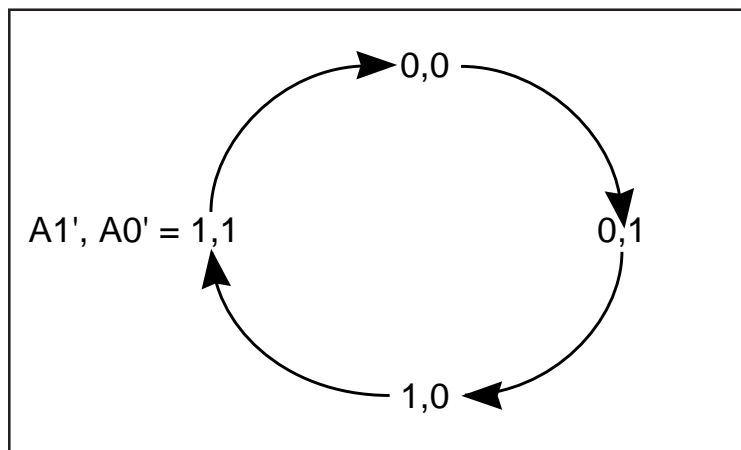
PARTIAL TRUTH TABLE

Function	GW	BWE	BW _a	BW _b	BW _c	BW _d
Read	H	H	X	X	X	X
Read	H	L	H	H	H	H
Write Byte 1	H	L	L	H	H	H
Write All Bytes	H	L	L	L	L	L
Write All Bytes	L	X	X	X	X	X

INTERLEAVED BURST ADDRESS TABLE (MODE = VCC or No Connect)

External Address	1st Burst Address	2nd Burst Address	3rd Burst Address
A1 A0	A1 A0	A1 A0	A1 A0
00	01	10	11
01	00	11	10
10	11	00	01
11	10	01	00

LINEAR BURST ADDRESS TABLE (MODE = GND)



ABSOLUTE MAXIMUM RATINGS ⁽¹⁾

Symbol	Parameter	Value	Unit
T _{BIAS}	Temperature Under Bias	-40 to +85	°C
T _{STG}	Storage Temperature	-55 to +150	°C
P _D	Power Dissipation	1.6	W
I _{OUT}	Output Current (per I/O)	100	mA
V _{IN} , V _{OUT}	Voltage Relative to GND for I/O Pins	-0.5 to V _{CCQ} + 0.5	V
V _{IN}	Voltage Relative to GND for for Address and Control Inputs	-0.5 to V _{CC} + 0.5	V
V _{CC}	Voltage on V _{CC} Supply Relative to GND	-0.5 to 4.6	V

Notes:

1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, precautions may be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.
3. This device contains circuitry that will ensure the output devices are in High-Z at power up.

OPERATING RANGE

Range	Ambient Temperature	V _{CC}	V _{CCQ}
Commercial	0°C to +70°C	3.3V, +10%, -5%	2.375–3.6V
Industrial	-40°C to +85°C	3.3V, +10%, -5%	2.375–3.6V

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
V _{OH}	Output HIGH Voltage	I _{OH} = -2.0 mA, V _{CCQ} = 2.5V	1.7	—	V
		I _{OH} = -4.0 mA, V _{CCQ} = 3.3V	2.4	—	V
V _{OL}	Output LOW Voltage	I _{OL} = 2.0 mA, V _{CCQ} = 2.5V	—	0.7	V
		I _{OL} = 8.0 mA, V _{CCQ} = 3.3V	—	0.4	V
V _{IH}	Input HIGH Voltage	V _{CCQ} = 2.5V	1.7	V _{CCQ} + 0.3	V
		V _{CCQ} = 3.3V	2.0	V _{CCQ} + 0.3	V
V _{IL}	Input LOW Voltage	V _{CCQ} = 2.5V	-0.3	0.7	V
		V _{CCQ} = 3.3V	-0.3	0.8	V
I _{LI}	Input Leakage Current	GND ≤ V _{IN} ≤ V _{CC} (1)	-2	2	μA
I _{LO}	Output Leakage Current	GND ≤ V _{OUT} ≤ V _{CCQ} , OE = V _{IH}	-2	2	μA

Notes:

1. The MODE, ZZ, SCD, XQ, pin has an internal pullup. and input leakage = ±10 μA .

POWER SUPPLY CHARACTERISTICS (Over Operating Range)

Parameter	Test Conditions	Symbol		-250	-200	-166	-133	Unit
				Max.	Max.	Max.	Max.	
AC Operating Supply Current	Device Selected, All Inputs ≤ V _{IL} or ≥ V _{IH} f = 1/t _{kc}	I _{CC1}	Com.	390	360	330	300	mA
			Ind.	410	380	350	320	
Clock Running	Device Deselected, V _{CC} = Max., All Inputs ≤ V _{IL} or ≥ V _{IH} f = 1/t _{kc}	I _{CC2}	Com.	110	100	90	85	mA
			Ind.	130	120	110	105	
COMS Standby	Device Deselected, V _{CC} = Max., All Inputs ≤ 0.2V or ≥ V _{CC} - 0.2V f = 0	I _{SB}	Com.	90	90	90	90	mA
			Ind.	100	100	100	100	
Power Down Mode	V _{CC} = Max ZZ ≥ V _{CC} - 0.2V f = 0 All input ≤ 0.2V or ≥ V _{CC} - 0.2V	I _{ZZ}	Com.	80	80	80	80	mA
			Ind.	90	90	90	90	

CAPACITANCE ^(1,2)

Symbol	Parameter Conditions	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	6 pF
C _{OUT}	Input/Output Capacitance	V _{OUT} = 0V	8 pF

Notes:

1. Tested initially and after any design or process changes that may affect these parameters.
2. Test conditions: T_A = 25°C, f = 1 MHz, V_{CC} = 3.3V.

AC TEST CONDITIONS

Parameter	Unit
Input Pulse Level	0V to 3.0V
Input Rise and Fall Times	1.5 ns
Input and Output Timing and Reference Level	1.5V for 3.3V I/O V _{CCQ} /2V for 2.5V I/O
Output Load	See Figures 1 and 2

AC TEST LOADS

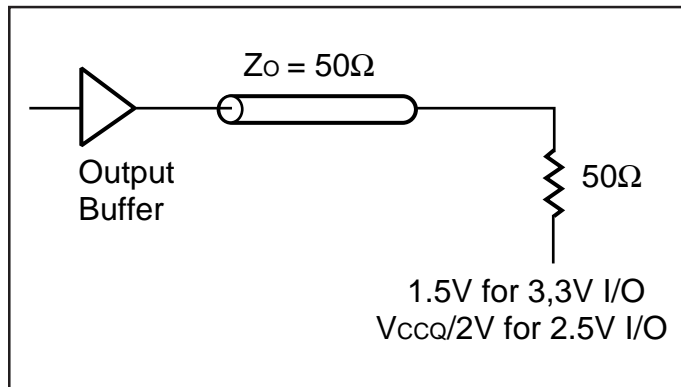


Figure 1

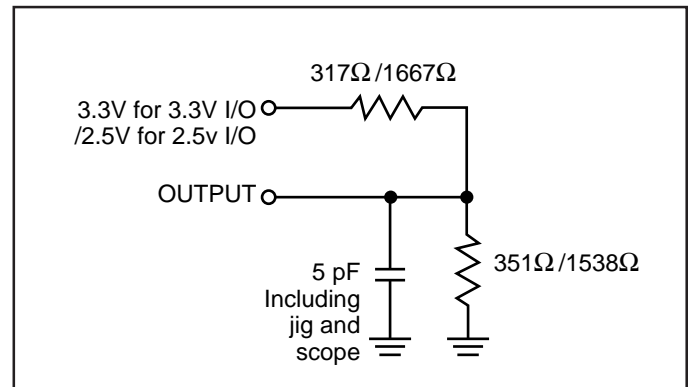


Figure 2

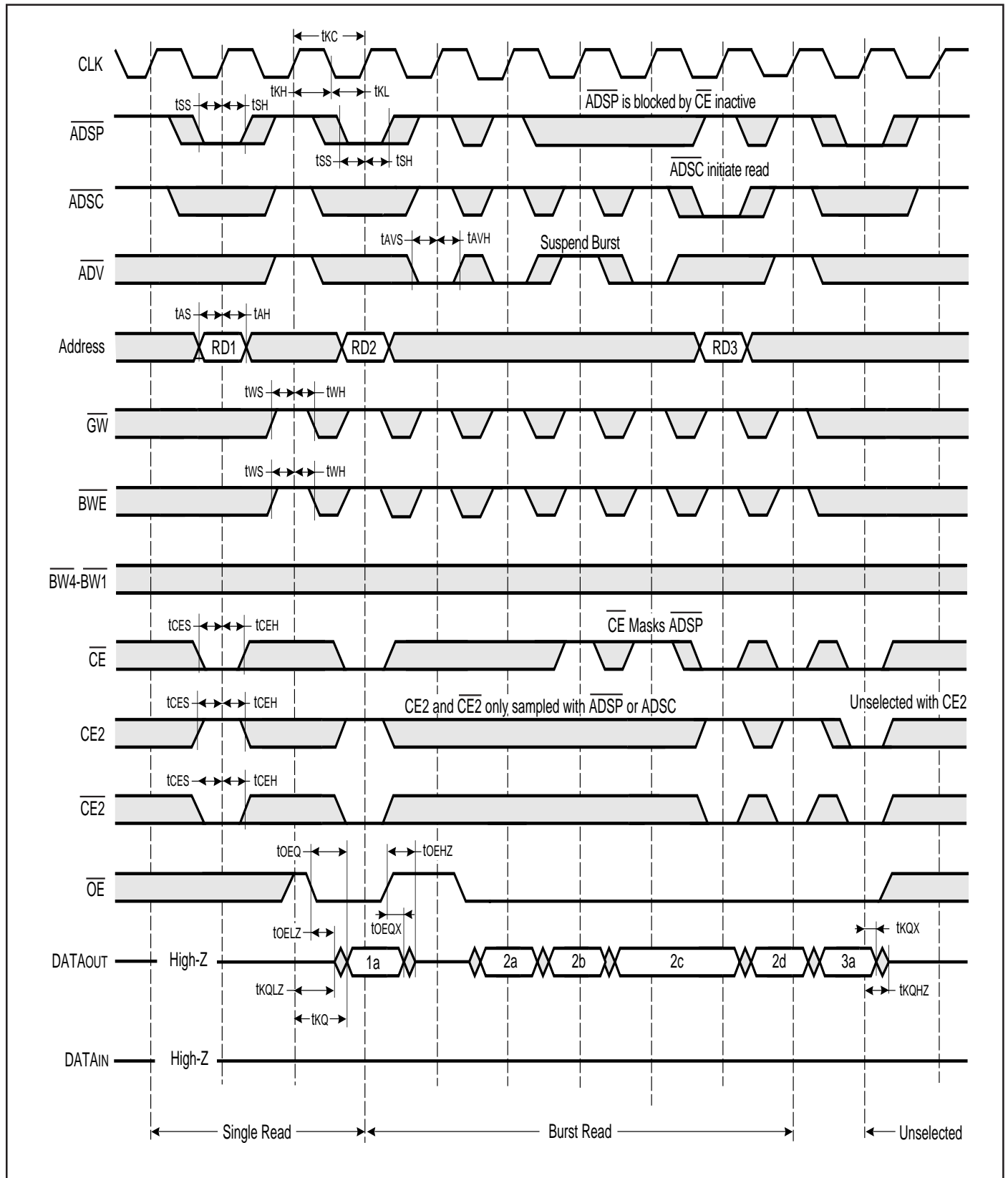
READ/WRITE CYCLE SWITCHING CHARACTERISTICS (Over Operating Range)

	Symbol	Parameter	-250		-200		-166		-133		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Pipeline	t _{kc}	Cycle Time	4	—	5	—	6	—	7.5	—	ns
	t _{kq}	Clock Access Time	—	3	—	3.1	—	3.5	—	4	ns
	t _{kqx} ⁽¹⁾	Clock High to Output Invalid	1.0	—	1.0	—	1.5	—	1.5	—	ns
	t _{kqlz} ^(1,2)	Clock High to Output Low-Z	0	—	0	—	0	—	0	—	ns
	t _{kh}	Clock High Pulse Width	1.6	—	2	—	2.3	—	2.8	—	ns
	t _{kl}	Clock Low Pulse Width	1.6	—	2	—	2.3	—	2.8	—	ns
	t _{kqhz} ^(1,2)	Clock High to Output High-Z	—	3.1	—	3.1	—	3.5	—	4	ns
	t _{oEQ}	Output Enable to Output Valid	—	3.1	—	3.1	—	3.5	—	4	ns
	t _{oELZ} ^(1,2)	Output Enable to Output Low-Z	0	—	0	—	0	—	0	—	ns
	t _{oEHZ} ^(1,2)	Output Enable to Output High-Z	—	3.0	—	3.0	—	3.5	—	4	ns
t _{as}	Address Setup Time	1.5	—	1.5	—	1.5	—	1.5	—	ns	
t _{ss}	Address Status Setup Time	1.5	—	1.5	—	1.5	—	1.5	—	ns	
t _{ws}	Write Setup Time	1.5	—	1.5	—	1.5	—	1.5	—	ns	
t _{ces}	Chip Enable Setup Time	1.5	—	1.5	—	1.5	—	1.5	—	ns	
t _{avs}	Address Advance Setup Time	1.5	—	1.5	—	1.5	—	1.5	—	ns	
t _{ds}	Data Setup time	1.5	—	1.5	—	1.5	—	1.5	—	ns	
t _{dH}	Data Hold time	0.5	—	0.5	—	0.5	—	0.5	—	ns	
t _{aH}	Address Hold Time	0.5	—	0.5	—	0.5	—	0.5	—	ns	
t _{sH}	Address Status Hold Time	0.5	—	0.5	—	0.5	—	0.5	—	ns	
t _{wH}	Write Hold Time	0.5	—	0.5	—	0.5	—	0.5	—	ns	
t _{ceH}	Chip Enable Hold Time	0.5	—	0.5	—	0.5	—	0.5	—	ns	
t _{avH}	Address Advance Hold Time	0.5	—	0.5	—	0.5	—	0.5	—	ns	
t _{zS}	ZZ Setup Time	2	—	2	—	2	—	2	—	cyc	
t _{zREC}	ZZ Recovery Time	2	—	2	—	2	—	2	—	cyc	

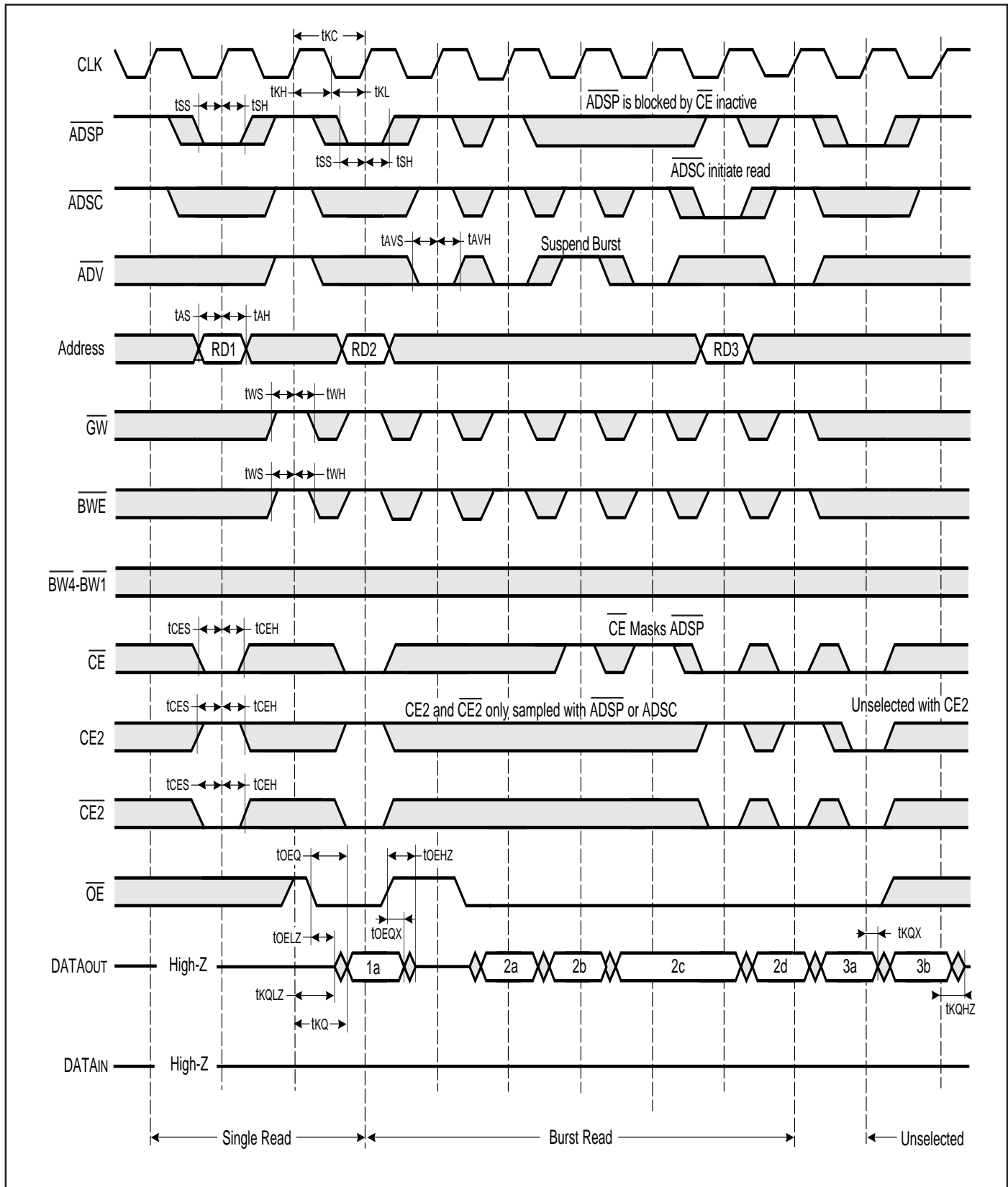
Note:

1. Guaranteed but not 100% tested. This parameter is periodically sampled.
2. Tested with load in Figure 2.

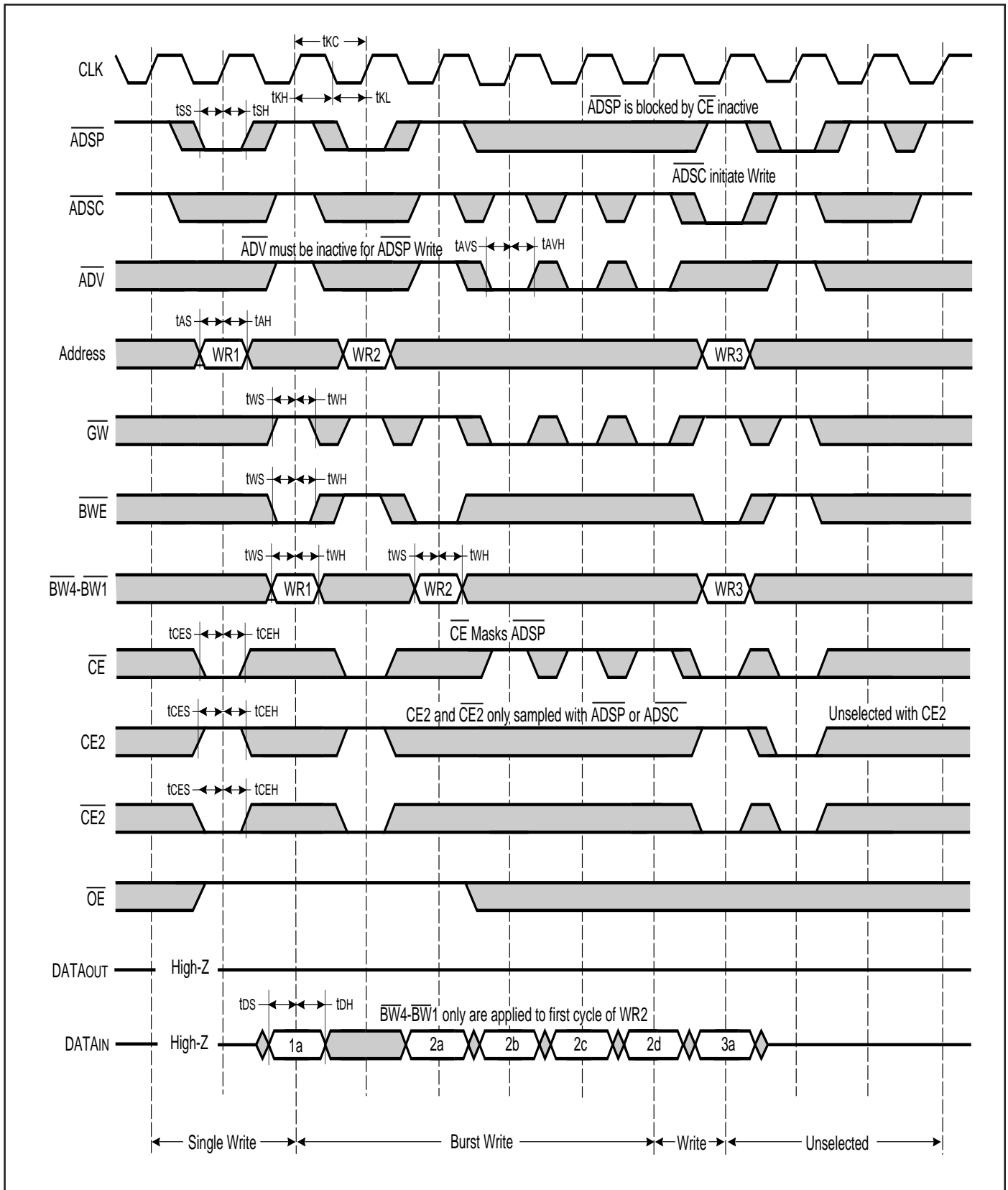
**PIPELINED SCD READ
 CYCLE TIMING**



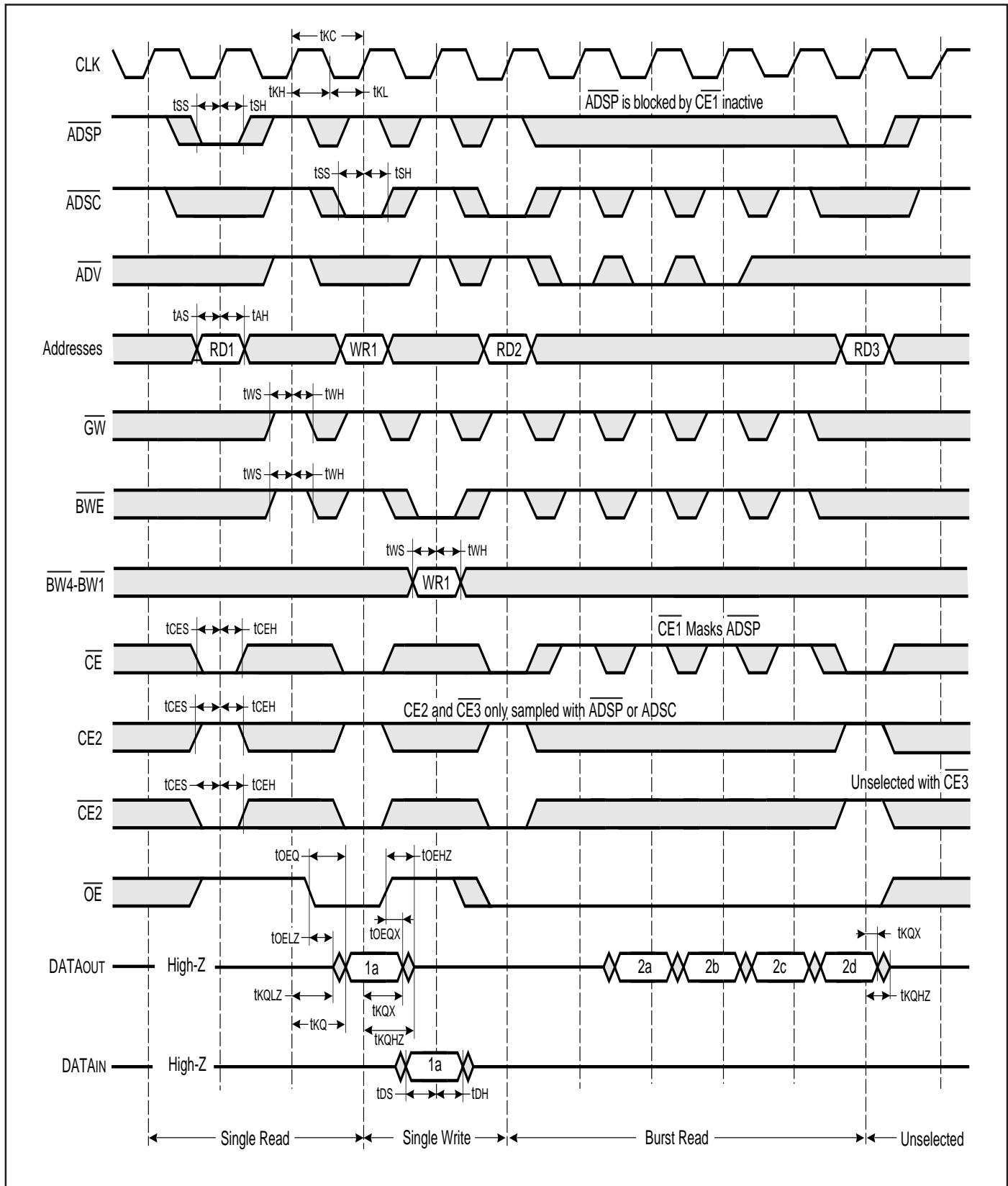
PIPELINED DCD READ CYCLE TIMING



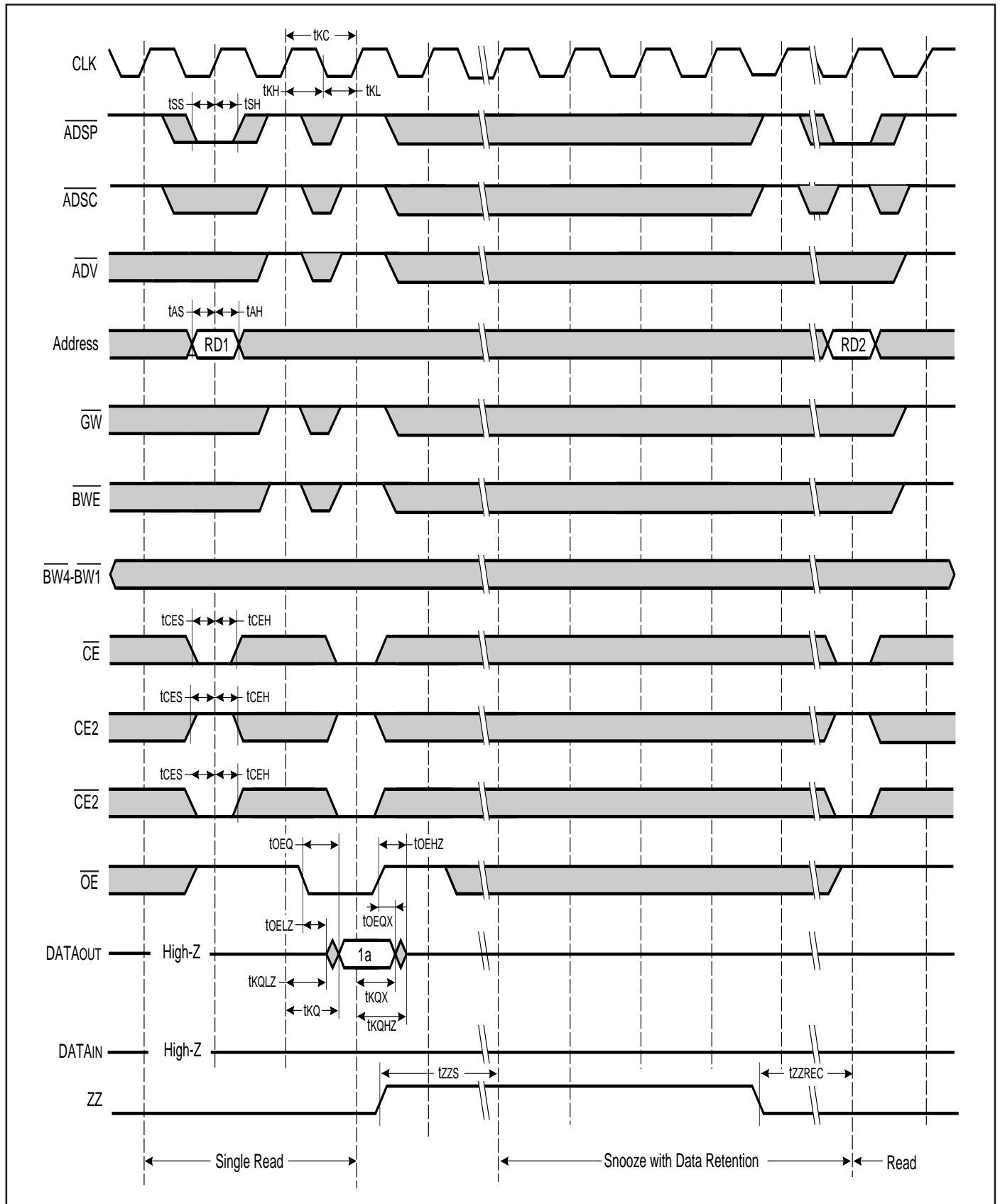
WRITE CYCLE TIMING



READ/WRITE CYCLE TIMING: PIPELINED



SNOOZE AND RECOVERY CYCLE TIMING



ORDERING INFORMATION
Commercial Range: 0°C to +70°C

Speed	Order Part Number	Package
250 MHz	IC61S25632T-250TQ	14*20*1.4mm LQFP
	IC61S25632D-250TQ	14*20*1.4mm LQFP
	IC61S25632D-250B	14*22mm PBGA
200 MHz	IC61S25632T-200TQ	14*20*1.4mm LQFP
	IC61S25632D-200TQ	14*20*1.4mm LQFP
	IC61S25632D-200B	14*22mm PBGA
166 MHz	IC61S25632T-166TQ	14x20x1.4mm LQFP
	IC61S25632D-166TQ	14x20x1.4mm LQFP
	IC61S25632D-166B	14*22mm PBGA
133 MHz	IC61S25632T-133TQ	14x20x1.4mm TQFP
	IC61S25632D-133TQ	14x20x1.4mm TQFP
	IC61S25632D-133B	14*22mm PBGA

Speed	Order Part Number	Package
250 MHz	IC61S25636T-250TQ	14*20*1.4mm LQFP
	IC61S25636D-250TQ	14*20*1.4mm LQFP
	IC61S25636D-250B	14*22mm PBGA
200 MHz	IC61S25636T-200TQ	14*20*1.4mm LQFP
	IC61S25636D-200TQ	14*20*1.4mm LQFP
	IC61S25636D-200B	14*22mm PBGA
166 MHz	IC61S25636T-166TQ	14x20x1.4mm LQFP
	IC61S25636D-166TQ	14x20x1.4mm LQFP
	IC61S25636D-166B	14*22mm PBGA
133 MHz	IC61S25636T-133TQ	14x20x1.4mm TQFP
	IC61S25636D-133TQ	14x20x1.4mm TQFP
	IC61S25636D-133B	14*22mm PBGA

Speed	Order Part Number	Package
250 MHz	IC61S51218T-250TQ	14*20*1.4mm LQFP
	IC61S51218D-250TQ	14*20*1.4mm LQFP
	IC61S51218D-250B	14*22mm PBGA
200 MHz	IC61S51218T-200TQ	14*20*1.4mm LQFP
	IC61S51218D-200TQ	14*20*1.4mm LQFP
	IC61S51218D-200B	14*22mm PBGA
166 MHz	IC61S51218T-166TQ	14x20x1.4mm LQFP
	IC61S51218D-166TQ	14x20x1.4mm LQFP
	IC61S51218D-166B	14*22mm PBGA
133 MHz	IC61S51218T-133TQ	14x20x1.4mm TQFP
	IC61S51218D-133TQ	14x20x1.4mm TQFP
	IC61S51218D-133B	14*22mm PBGA

Industrial Range: -40°C to 85°C

Speed	Order Part Number	Package
250 MHz	IC61S25632T-250TQI	14*20*1.4mm LQFP
	IC61S25632D-250TQI	14*20*1.4mm LQFP
	IC61S25632D-250B	14*22mm PBGA
200 MHz	IC61S25632T-200TQI	14*20*1.4mm LQFP
	IC61S25632D-200TQI	14*20*1.4mm LQFP
	IC61S25632D-200B	14*22mm PBGA
166 MHz	IC61S25632T-166TQI	14x20x1.4mm LQFP
	IC61S25632D-166TQI	14x20x1.4mm LQFP
	IC61S25632D-166B	14*22mm PBGA
133 MHz	IC61S25632T-133TQI	14x20x1.4mm TQFP
	IC61S25632D-133TQI	14x20x1.4mm TQFP
	IC61S25632D-133B	14*22mm PBGA

Speed	Order Part Number	Package
250 MHz	IC61S25636T-250TQI	14*20*1.4mm LQFP
	IC61S25636D-250TQI	14*20*1.4mm LQFP
	IC61S25636D-250B	14*22mm PBGA
200 MHz	IC61S25636T-200TQI	14*20*1.4mm LQFP
	IC61S25636D-200TQI	14*20*1.4mm LQFP
	IC61S25636D-200B	14*22mm PBGA
166 MHz	IC61S25636T-166TQI	14x20x1.4mm LQFP
	IC61S25636D-166TQI	14x20x1.4mm LQFP
	IC61S25636D-166B	14*22mm PBGA
133 MHz	IC61S25636T-133TQI	14x20x1.4mm TQFP
	IC61S25636D-133TQI	14x20x1.4mm TQFP
	IC61S25636D-133B	14*22mm PBGA

Speed	Order Part Number	Package
250 MHz	IC61S51218T-250TQI	14*20*1.4mm LQFP
	IC61S51218D-250TQI	14*20*1.4mm LQFP
	IC61S51218D-250B	14*22mm PBGA
200 MHz	IC61S51218T-200TQI	14*20*1.4mm LQFP
	IC61S51218D-200TQI	14*20*1.4mm LQFP
	IC61S51218D-200B	14*22mm PBGA
166 MHz	IC61S51218T-166TQI	14x20x1.4mm LQFP
	IC61S51218D-166TQI	14x20x1.4mm LQFP
	IC61S51218D-166B	14*22mm PBGA
133 MHz	IC61S51218T-133TQI	14x20x1.4mm TQFP
	IC61S51218D-133TQI	14x20x1.4mm TQFP
	IC61S51218D-133B	14*22mm PBGA



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