RENESAS

RMLV3216A Series

32Mb Advanced LPSRAM (2M word × 16bit / 4M word x 8bit)

Description

The RMLV3216A Series is a family of 32-Mbit static RAMs organized 2,097,152-word × 16-bit, fabricated by Renesas's high-performance Advanced LPSRAM technologies. The RMLV3216A Series has realized higher density, higher performance and low power consumption. The RMLV3216A Series offers low power standby power dissipation; therefore, it is suitable for battery backup systems. It is offered in 48pin TSOP (I), 52pin μTSOP (II) or 48-ball fine pitch ball grid array.
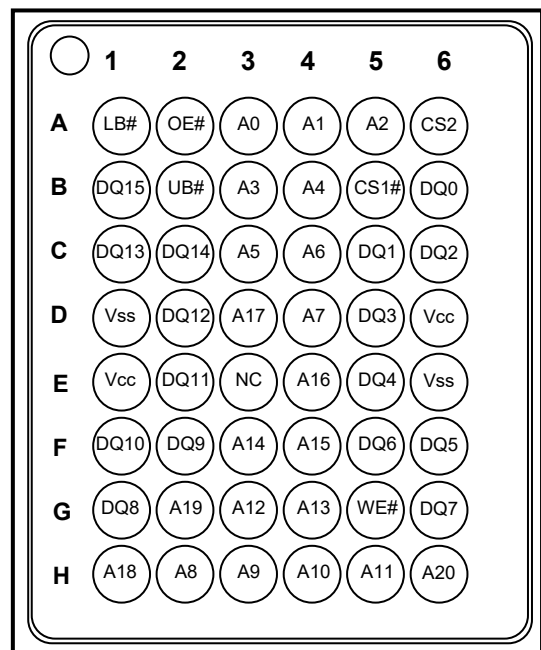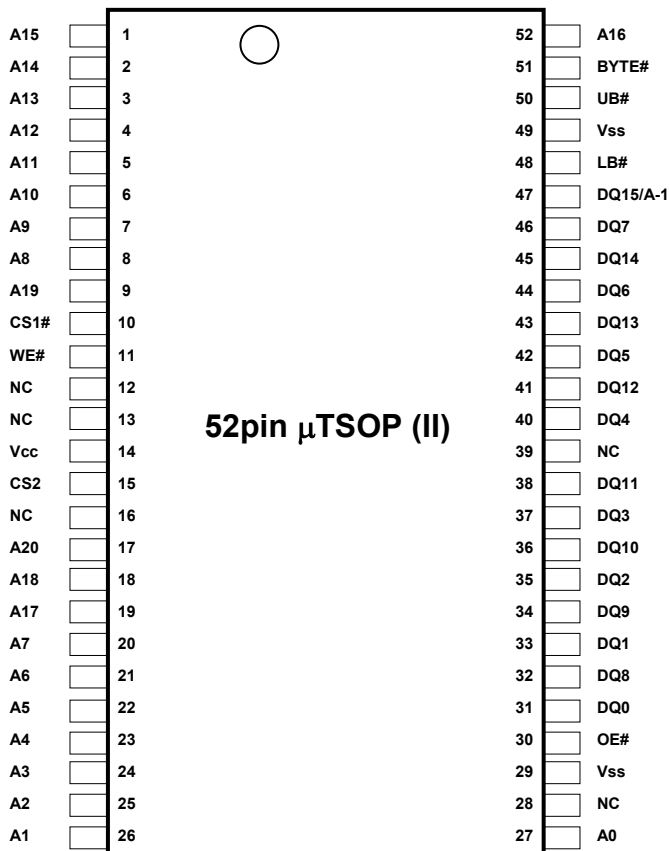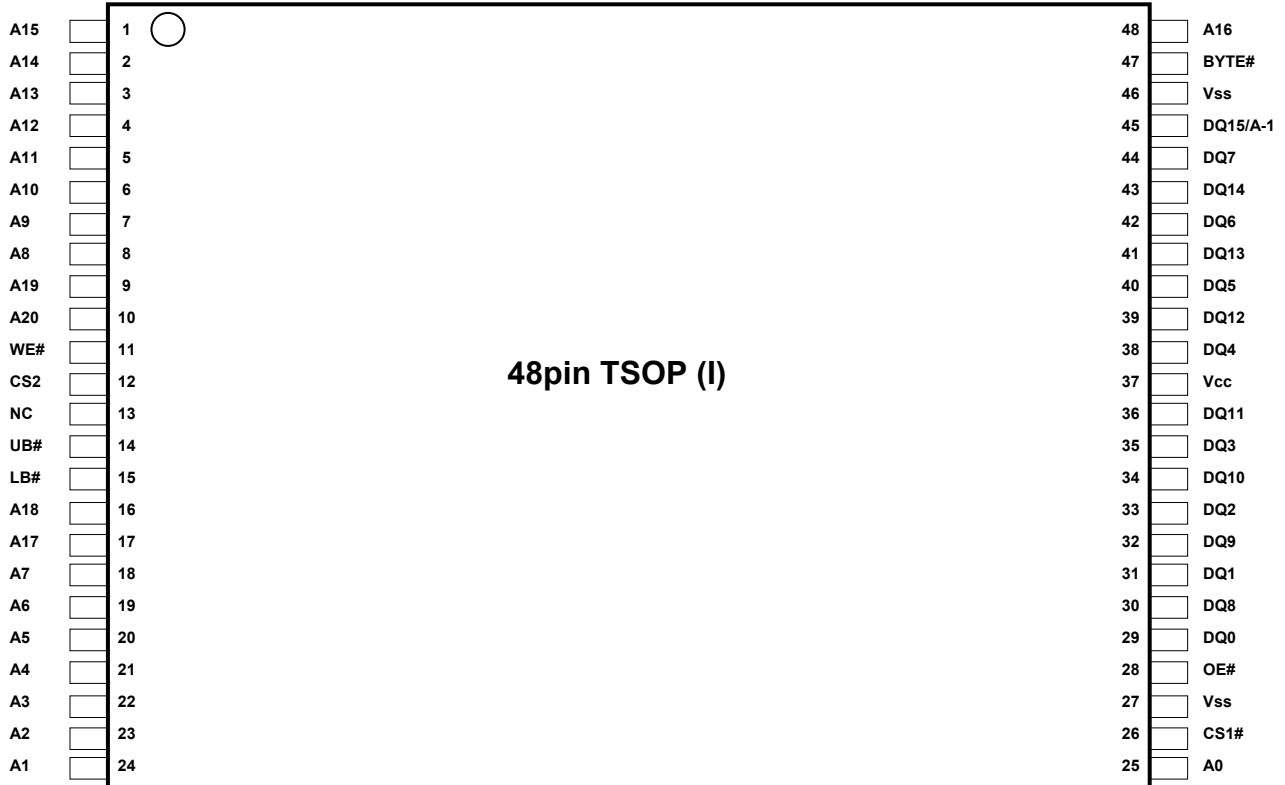
Features

- Single 3V supply: 2.7V to 3.6V
- Access time: 55ns (max.)
- Current consumption:
  ⎯ Standby: 0.6μA (typ.)
- Common data input and output
  ⎯ Three state output
- Directly TTL compatible
  ⎯ All inputs and outputs
- Battery backup operation

Part Name Information

Part Name	Access time	Temperature Range	Package
RMLV3216AGSA-5S2			12mm x 20mm 48pin plastic TSOP (I)
RMLV3216AGSD-5S2	55 ns	-40 ~ +85°C	10.79mm × 10.49mm 52pin plastic μTSOP (II)
RMLV3216AGBG-5S2			48-ball FBGA with 0.75mm ball pitch

Pin Arrangement

48pin TSOP (I)

Pin	Signal		Pin	Signal
1	A15		48	A16
2	A14		47	BYTE#
3	A13		46	Vss
4	A12		45	DQ15/A-1
5	A11		44	DQ7
6	A10		43	DQ14
7	A9		42	DQ6
8	A8		41	DQ13
9	A19		40	DQ5
10	A20		39	DQ12
11	WE#		38	DQ4
12	CS2		37	Vcc
13	NC		36	DQ11
14	UB#		35	DQ3
15	LB#		34	DQ10
16	A18		33	DQ2
17	A17		32	DQ9
18	A7		31	DQ1
19	A6		30	DQ8
20	A5		29	DQ0
21	A4		28	OE#
22	A3		27	Vss
23	A2		26	CS1#
24	A1		25	A0

52pin μTSOP (II)

Pin	Signal		Pin	Signal
1	A15		52	A16
2	A14		51	BYTE#
3	A13		50	UB#
4	A12		49	Vss
5	A11		48	LB#
6	A10		47	DQ15/A-1
7	A9		46	DQ7
8	A8		45	DQ14
9	A19		44	DQ6
10	CS1#		43	DQ13
11	WE#		42	DQ5
12	NC		41	DQ12
13	NC		40	DQ4
14	Vcc		39	NC
15	CS2		38	DQ11
16	NC		37	DQ3
17	A20		36	DQ10
18	A18		35	DQ2
19	A17		34	DQ9
20	A7		33	DQ1
21	A6		32	DQ8
22	A5		31	DQ0
23	A4		30	OE#
24	A3		29	Vss
25	A2		28	NC
26	A1		27	A0

48-ball FBGA (TOP VIEW)

	1	2	3	4	5	6
A	LB#	OE#	A0	A1	A2	CS2
B	DQ15	UB#	A3	A4	CS1#	DQ0
C	DQ13	DQ14	A5	A6	DQ1	DQ2
D	Vss	DQ12	A17	A7	DQ3	Vcc
E	Vcc	DQ11	NC	A16	DQ4	Vss
F	DQ10	DQ9	A14	A15	DQ6	DQ5
G	DQ8	A19	A12	A13	WE#	DQ7
H	A18	A8	A9	A10	A11	A20

Pin Description

Pin name	Function
Vcc	Power supply
Vss	Ground
A0 to A20	Address input (word mode)
A-1 to A20	Address input (byte mode)
DQ0 to DQ15	Data input/output
CS1#	Chip select 1
CS2	Chip select 2
OE#	Output enable
WE#	Write enable
LB#	Lower byte select
UB#	Upper byte select
BYTE#	Byte control mode enable
NC	No connection

Block Diagram
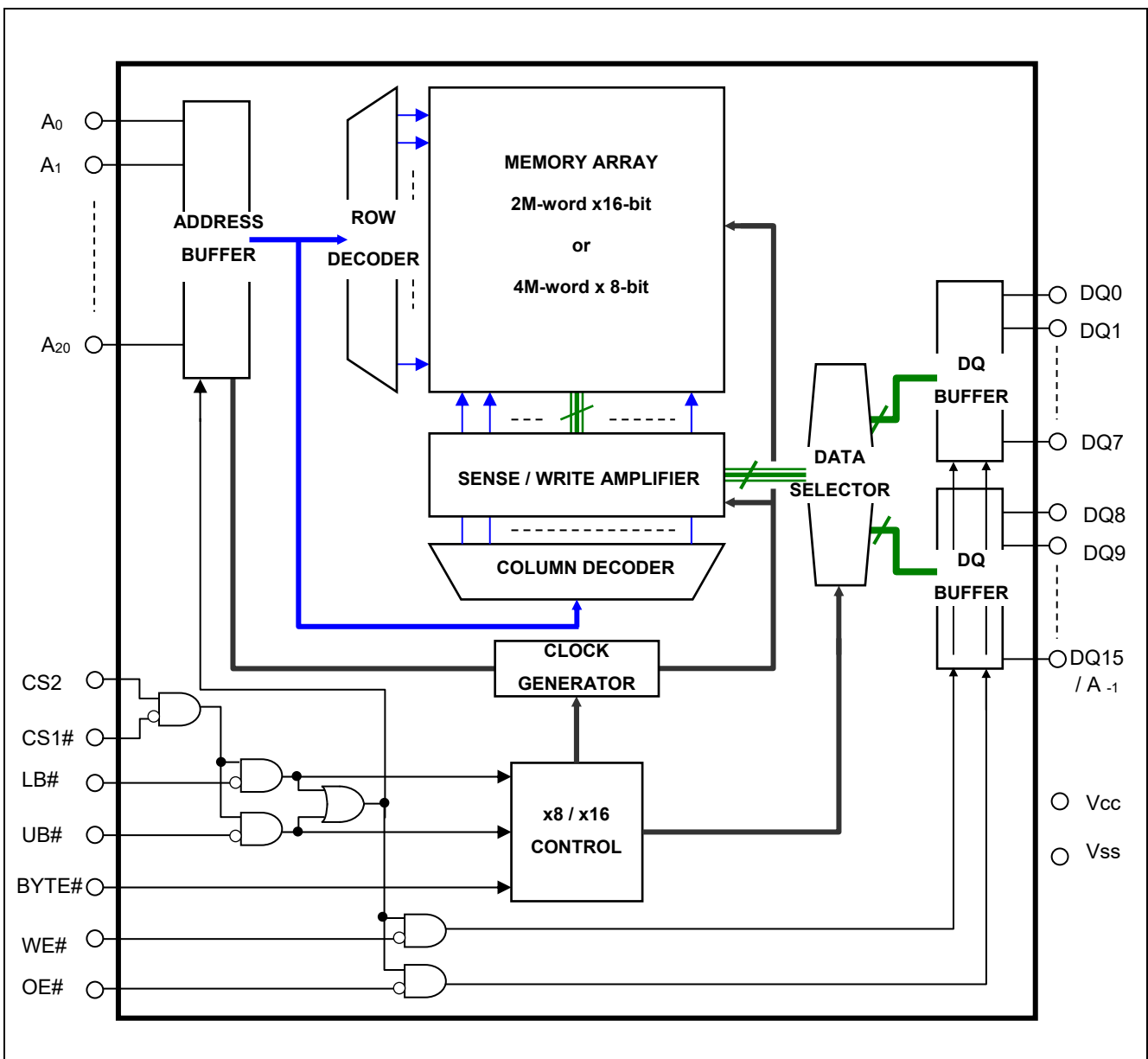
Note 1.   BYTE# pin supported by only 48pin TSOP (I) and 52pin µTSOP (II) types.

Operation Table

CS1#	CS2	BYTE#	UB#	LB#	WE#	OE#	DQ0~7	DQ8~14	DQ15	Operation
H	X	X	X	X	X	X	High-Z	High-Z	High-Z	Stand-by
X	L	X	X	X	X	X	High-Z	High-Z	High-Z	Stand-by
X	X	H	H	H	X	X	High-Z	High-Z	High-Z	Stand-by
L	H	H	H	L	L	X	Din	High-Z	High-Z	Write in lower byte
L	H	H	H	L	H	L	Dout	High-Z	High-Z	Read in lower byte
L	H	H	H	L	H	H	High-Z	High-Z	High-Z	Output disable
L	H	H	L	H	L	X	High-Z	Din	Din	Write in upper byte
L	H	H	L	H	H	L	High-Z	Dout	Dout	Read in upper byte
L	H	H	L	H	H	H	High-Z	High-Z	High-Z	Output disable
L	H	H	L	L	L	X	Din	Din	Din	Word write
L	H	H	L	L	H	L	Dout	Dout	Dout	Word read
L	H	H	L	L	H	H	High-Z	High-Z	High-Z	Output disable
L	H	L	X	X	L	X	Din	High-Z	A-1	Byte write
L	H	L	X	X	H	L	Dout	High-Z	A-1	Byte read
L	H	L	X	X	H	H	High-Z	High-Z	A-1	Output disable

Note   2.   H: V_{IH} L: V_{IL} X: V_{IH} or V_{IL}

3.   BYTE# pin supported by only 48pin TSOP (I) and 52pin µTSOP (II) types.
48-ball FBGA type equals BYTE#=H mode.

Absolute Maximum Ratings

Parameter	Symbol	Value	unit
Power supply voltage relative to V_{SS}	V_{CC}	-0.5 to +4.6	V
Terminal voltage on any pin relative to V_{SS}	V_T	-0.5[4] to V_{CC}+0.3[5]	V
Power dissipation	P_T	0.7	W
Operation temperature	Topr	-40 to +85	°C
Storage temperature range	Tstg	-65 to +150	°C
Storage temperature range under bias	Tbias	-40 to +85	°C

Note   4.   -2.0V for pulse ≤ 30ns (full width at half maximum)

5.   Maximum voltage is +4.6V.

DC Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Supply voltage	V_{CC}	2.7	3.0	3.6	V	
	V_{SS}	0	0	0	V	
Input high voltage	V_{IH}	2.2	—	V_{CC}+0.3	V	
Input low voltage	V_{IL}	-0.3	—	0.6	V	6
Ambient temperature range	Ta	-40	—	+85	°C	

Note   6.   -2.0V for pulse ≤ 30ns (full width at half maximum)

DC Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test conditions[7]
Input leakage current	$|I_{LI}|$	—	—	1	μA	Vin = V_{SS} to V_{CC}
Output leakage current	$|I_{LO}|$	—	—	1	μA	CS1# = V_{IH} or CS2 = V_{IL} or OE# = V_{IH} or WE# = V_{IL} or LB# = UB# = V_{IH}, $V_{I/O}$ = V_{SS} to V_{CC}
Average operating current	I_{CC1}	—	27[8]	35	mA	Cycle = 55ns, duty =100%, $I_{I/O}$ = 0mA, CS1# = V_{IL}, CS2 = V_{IH}, Others = V_{IH}/V_{IL}
	I_{CC2}	—	2[8]	4	mA	Cycle = 1μs, duty =100%, $I_{I/O}$ = 0mA, CS1# ≤ 0.2V, CS2 ≥ V_{CC}-0.2V, V_{IH} ≥ V_{CC}-0.2V, V_{IL} ≤ 0.2V
Standby current	I_{SB}	—	0.1[8]	0.3	mA	CS2 = V_{IL}, Others = V_{SS} to V_{CC}
Standby current	I_{SB1}	—	0.6[8]	4	μA	~+25°C	Vin = V_{SS} to V_{CC}, (1) CS2 ≤ 0.2V or (2) CS1# ≥ V_{CC}-0.2V, CS2 ≥ V_{CC}-0.2V or (3) LB# = UB# ≥ V_{CC}-0.2V, CS1# ≤ 0.2V, CS2 ≥ V_{CC}-0.2V
		—	1[9]	6	μA	~+40°C	
		—	4[10]	17	μA	~+70°C	
		—	8[11]	24	μA	~+85°C	
Output high voltage	V_{OH}	2.4	—	—	V	I_{OH} = -1mA
Output low voltage	V_{OL}	—	—	0.4	V	I_{OL} = 2mA

Note 7. BYTE# pin supported by only 48pin TSOP (I) and 52pin μTSOP (II) types.
BYTE# ≥ Vcc - 0.2V or BYTE# ≤ 0.2V

8. Typical parameter indicates the value for the center of distribution at 3.0V (Ta=25°C), and not 100% tested.
9. Typical parameter indicates the value for the center of distribution at 3.0V (Ta=40°C), and not 100% tested.
10. Typical parameter indicates the value for the center of distribution at 3.0V (Ta=70°C), and not 100% tested.
11. Typical parameter indicates the value for the center of distribution at 3.0V (Ta=85°C), and not 100% tested.

Capacitance

(Ta =25°C, f =1MHz)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test conditions	Note
Input capacitance	C in	—	—	10	pF	Vin =0V	12
Input / output capacitance	C I/O	—	—	10	pF	$V_{I/O}$ =0V	12

Note 12. This parameter is sampled and not 100% tested.

AC Characteristics

Test Conditions (Vcc = 2.7V ~ 3.6V, Ta = -40 ~ +85°C)

- Input pulse levels:
  $V_{IL} = 0.4V$, $V_{IH} = 2.4V$
- Input rise and fall time: 5ns
- Input and output timing reference level: 1.4V
- Output load: See figures (Including scope and jig)
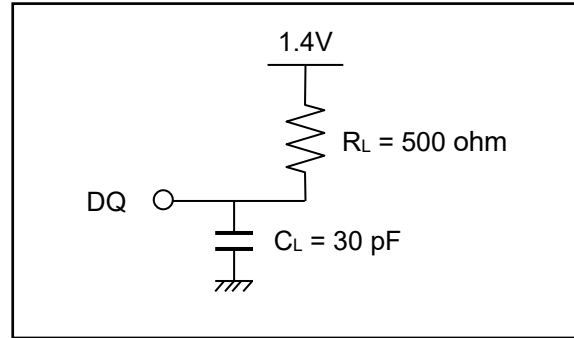
Read Cycle

Parameter	Symbol	Min.	Max.	Unit	Note
Read cycle time	t_{RC}	55		ns	
Address access time	t_{AA}	—	55	ns	
Chip select access time	t_{ACS1}	—	45	ns	
	t_{ACS2}	—	45	ns	
Output enable to output valid	t_{OE}	—	22	ns	
Output hold from address change	t_{OH}	10	—	ns	
LB#, UB# access time	t_{BA}	—	45	ns	
Chip select to output in low-Z	t_{CLZ1}	10	—	ns	13,14
	t_{CLZ2}	10	—	ns	13,14
LB#, UB# enable to low-Z	t_{BLZ}	5	—	ns	13,14
Output enable to output in low-Z	t_{OLZ}	5	—	ns	13,14
Chip deselect to output in high-Z	t_{CHZ1}	0	18	ns	13,14,15
	t_{CHZ2}	0	18	ns	13,14,15
LB#, UB# disable to high-Z	t_{BHZ}	0	18	ns	13,14,15
Output disable to output in high-Z	t_{OHZ}	0	18	ns	13,14,15

Note 13. This parameter is sampled and not 100% tested.

14. At any given temperature and voltage condition, t_{CHZ1} max is less than t_{CLZ1} min, t_{CHZ2} max is less than t_{CLZ2} min, t_{BHZ} max is less than t_{BLZ} min, and t_{OHZ} max is less than t_{OLZ} min, for any device.

15. t_{CHZ1}, t_{CHZ2}, t_{BHZ} and t_{OHZ} are defined as the time when the DQ pins enter a high-impedance state and are not referred to the DQ levels.

Write Cycle

Parameter	Symbol	Min.	Max.	Unit	Note
Write cycle time	t_{WC}	55	—	ns	
Address valid to write end	t_{AW}	35	—	ns	
Chip select to write end	t_{CW}	35	—	ns	
Write pulse width	t_{WP}	35	—	ns	16
LB#,UB# valid to write end	t_{BW}	35	—	ns	
Address setup time to write start	t_{AS}	0	—	ns	
Write recovery time from write end	t_{WR}	0	—	ns	
Data to write time overlap	t_{DW}	25	—	ns	
Data hold from write end	t_{DH}	0	—	ns	
Output enable from write end	t_{OW}	5	—	ns	17
Output disable to output in high-Z	t_{OHZ}	0	18	ns	17,18
Write to output in high-Z	t_{WHZ}	0	18	ns	17,18

Note 16. t_{WP} is the interval between write start and write end.

A write starts when all of (CS1#), (CS2), (WE#) and (one or both of LB# and UB#) become active.

A write is performed during the overlap of a low CS1#, a high CS2, a low WE# and a low LB# or a low UB#.

A write ends when any of (CS1#), (CS2), (WE#) or (one or both of LB# and UB#) becomes inactive.

17. This parameter is sampled and not 100% tested.

18. t_{OHZ} and t_{WHZ} are defined as the time when the DQ pins enter a high-impedance state and are not referred to the DQ levels.

BYTE# Timing Conditions   (BYTE# pin supported by only 48pin TSOP (I) and 52pin µTSOP (II) types)

Parameter	Symbol	Min.	Max.	Unit	Note
Byte setup time	t_{BS}	5	-	ms	
Byte recovery time	t_{BR}	5	-	ms	

BYTE# Timing Waveforms
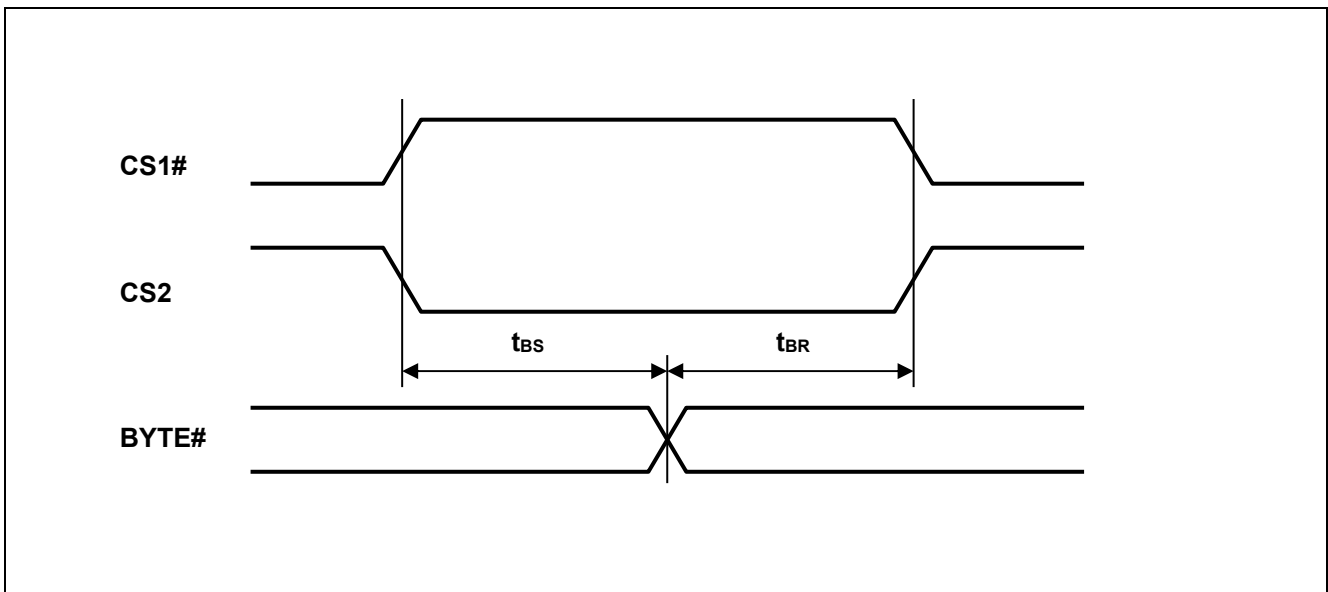
Timing Waveforms

Read Cycle[19]
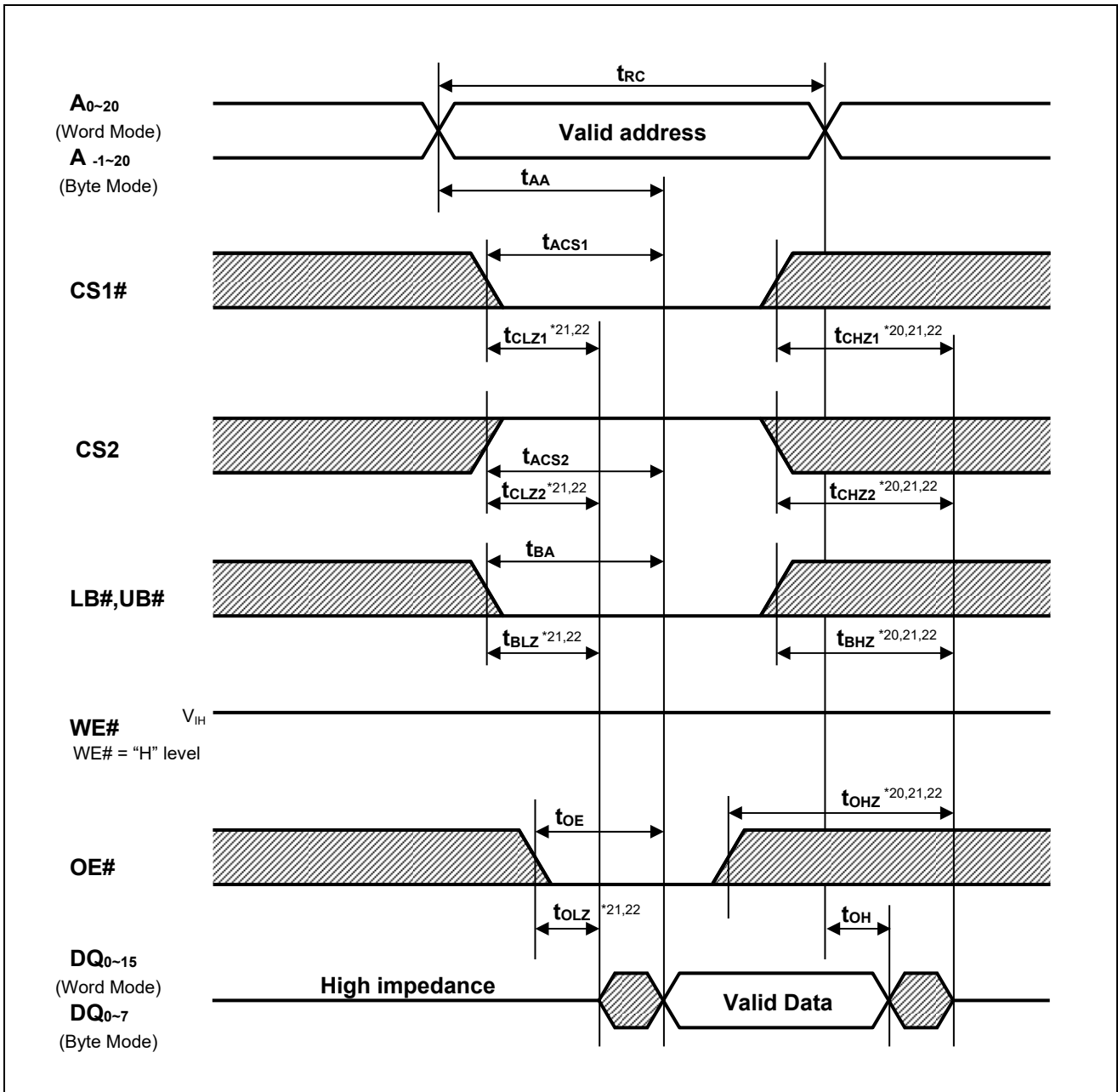
Note 19. BYTE# pin supported by only 48pin TSOP (I) and 52pin µTSOP (II) types.

BYTE# ≥ Vcc - 0.2V (Word mode) or BYTE# ≤ 0.2V (Byte mode)

20. t_{CHZ1}, t_{CHZ2}, t_{BHZ} and t_{OHZ} are defined as the time when the DQ pins enter a high-impedance state and are not referred to the DQ levels.

21. This parameter is sampled and not 100% tested.

22. At any given temperature and voltage condition, t_{CHZ1} max is less than t_{CLZ1} min, t_{CHZ2} max is less than t_{CLZ2} min, t_{BHZ} max is less than t_{BLZ} min, and t_{OHZ} max is less than t_{OLZ} min, for any device.

Write Cycle (1)[*23] (WE# CLOCK, OE#="H" while writing)
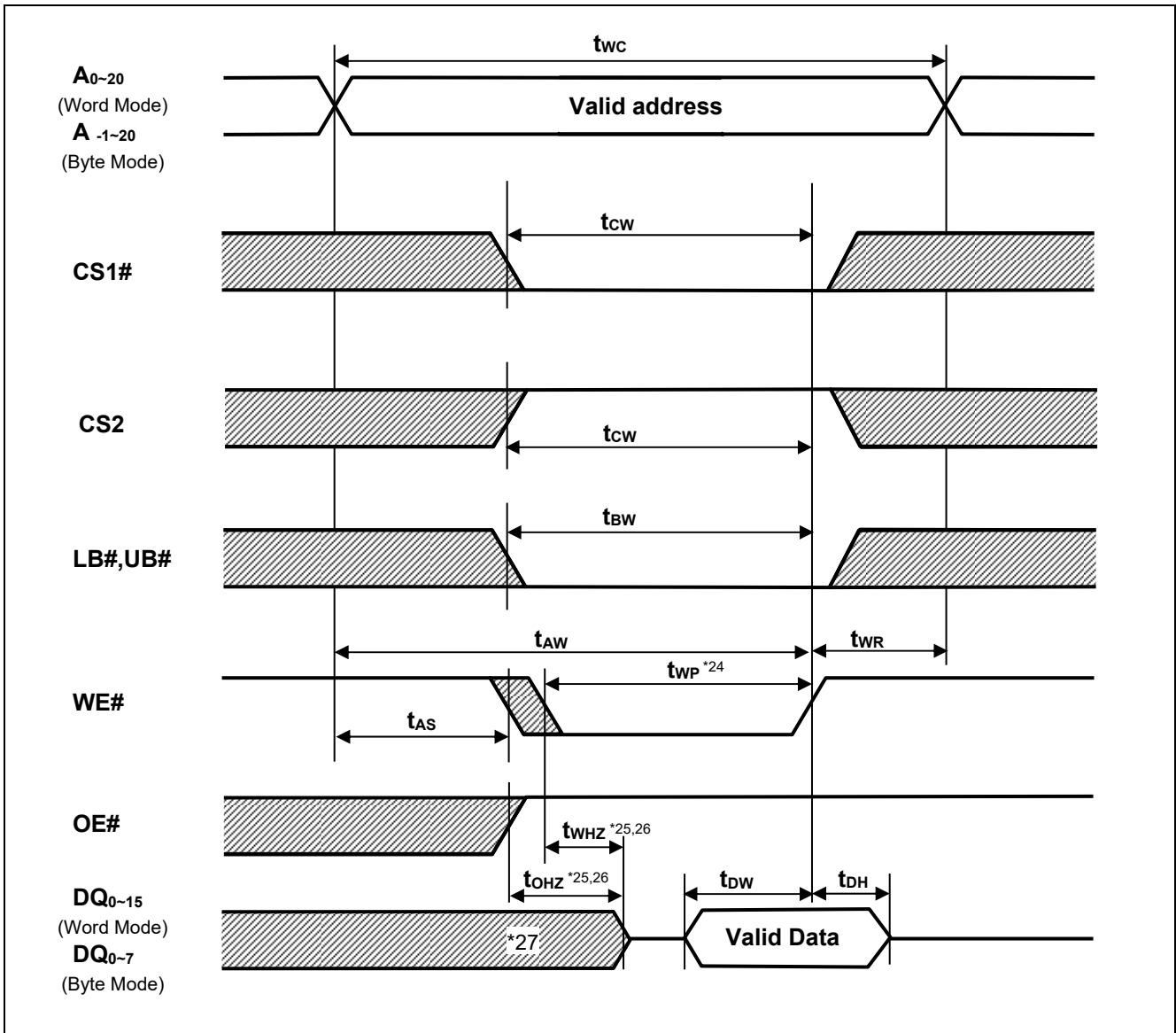
Note 23. BYTE# pin supported by only 48pin TSOP (I) and 52pin µTSOP (II) types.

BYTE# ≥ Vcc - 0.2V (Word mode) or BYTE# ≤ 0.2V (Byte mode)

24. t_{WP} is the interval between write start and write end.

A write starts when all of (CS1#), (CS2), (WE#) and (one or both of LB# and UB#) become active.

A write is performed during the overlap of a low CS1#, a high CS2, a low WE# and a low LB# or a low UB#.

A write ends when any of (CS1#), (CS2), (WE#) or (one or both of LB# and UB#) becomes inactive.

25. t_{OHZ} and t_{WHZ} are defined as the time when the DQ pins enter a high-impedance state and are not referred to the DQ levels.

26. This parameter is sampled and not 100% tested.

27. During this period, DQ pins are in the output state so input signals must not be applied to the DQ pins.

Write Cycle (2)[*28]   (WE# CLOCK, OE# Low Fixed)
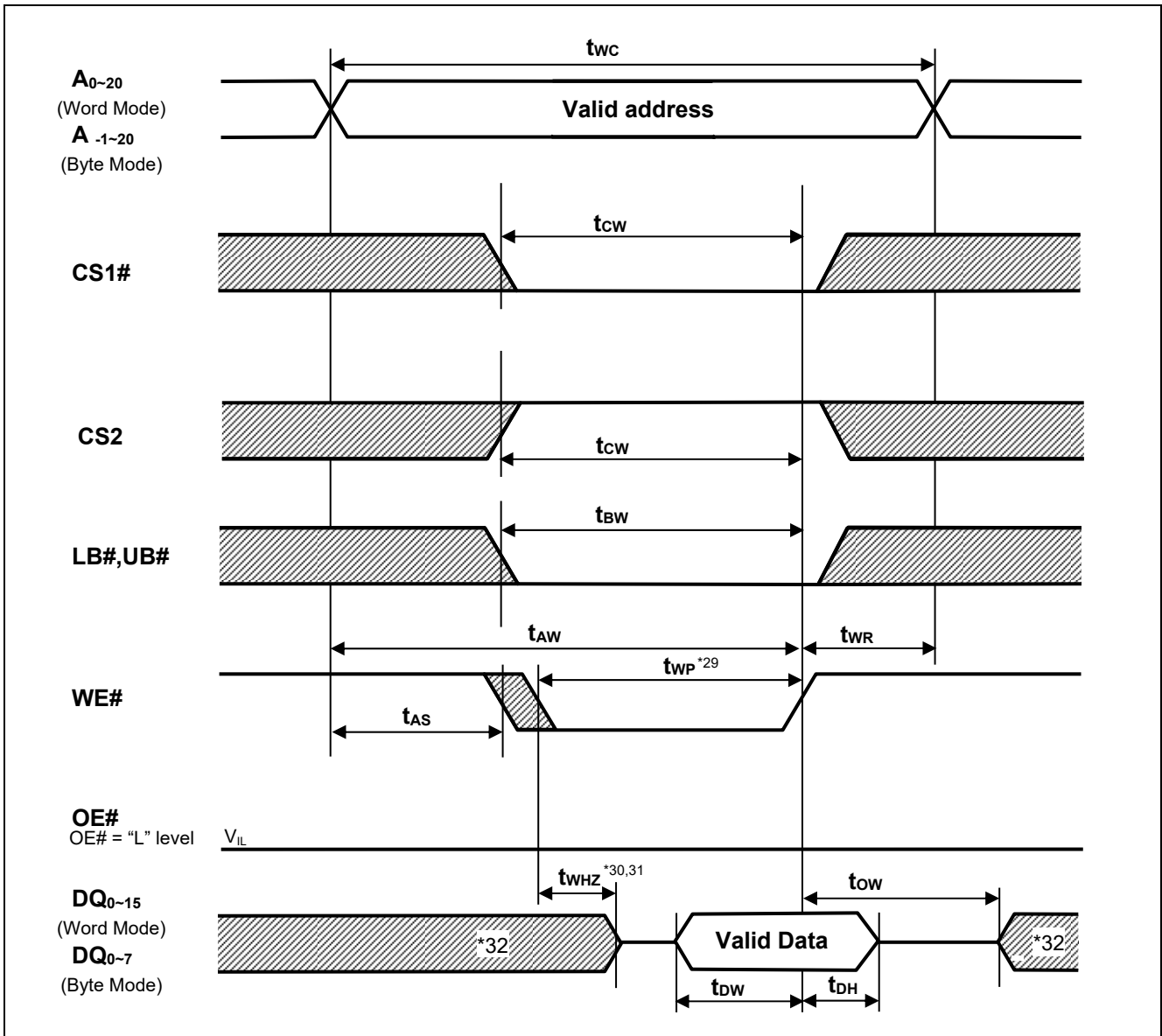
Note 28. BYTE# pin supported by only 48pin TSOP (I) and 52pin µTSOP (II) types.

BYTE# ≥ Vcc - 0.2V (Word mode) or BYTE# ≤ 0.2V (Byte mode)

29. t_{WP} is the interval between write start and write end.

A write starts when all of (CS1#), (CS2), (WE#) and (one or both of LB# and UB#) become active.

A write is performed during the overlap of a low CS1#, a high CS2, a low WE# and a low LB# or a low UB#.

A write ends when any of (CS1#), (CS2), (WE#) or (one or both of LB# and UB#) becomes inactive.

30. t_{WHZ} is defined as the time when the DQ pins enter a high-impedance state and are not referred to the DQ levels.

31. This parameter is sampled and not 100% tested.

32. During this period, DQ pins are in the output state so input signals must not be applied to the DQ pins.

Write Cycle (3)[*33] (CS1#, CS2 CLOCK)
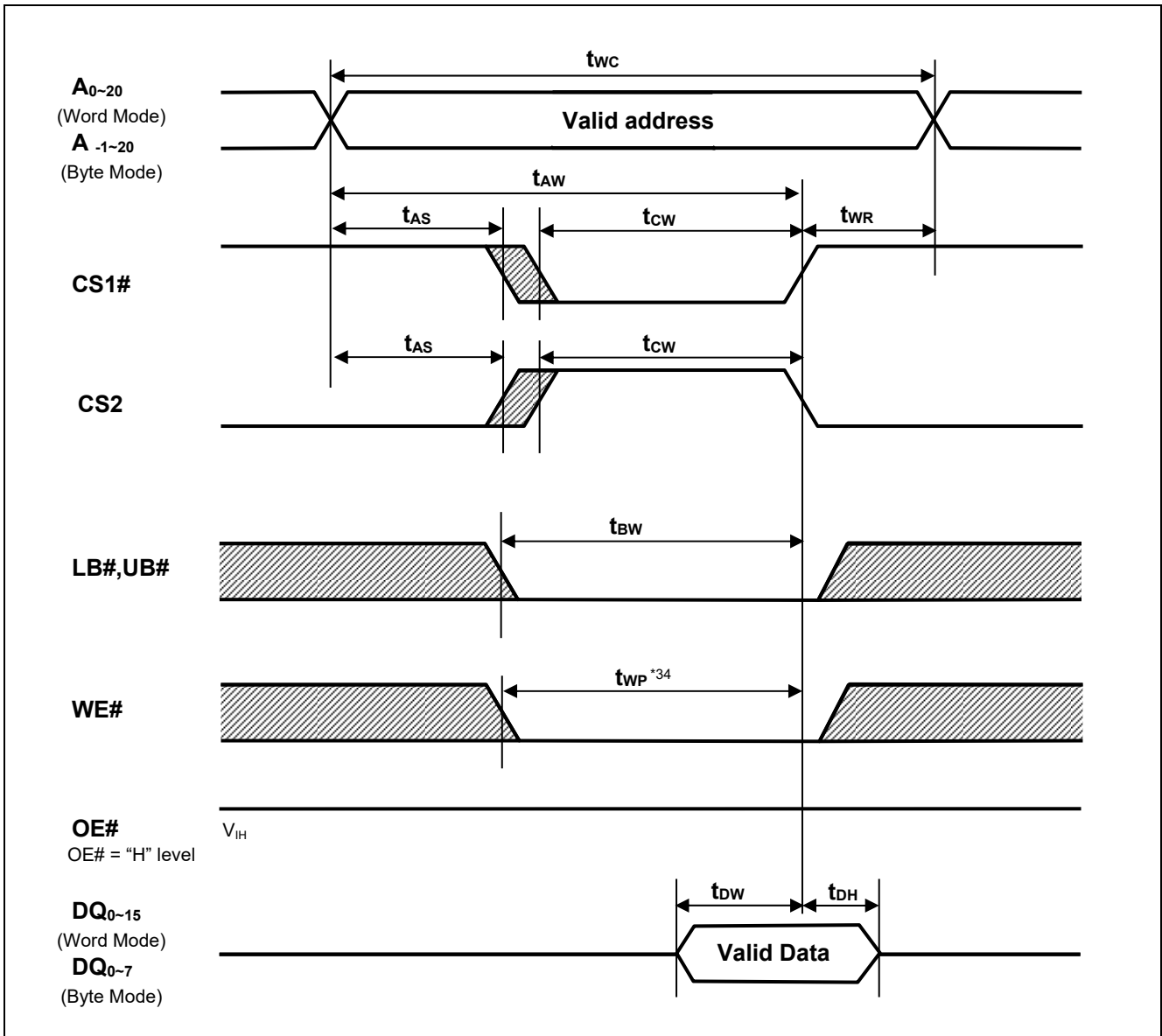
Note 33. BYTE# pin supported by only 48pin TSOP (I) and 52pin μTSOP (II) types.

BYTE# ≥ Vcc - 0.2V (Word mode) or BYTE# ≤ 0.2V (Byte mode)

34. t_{WP} is the interval between write start and write end.

A write starts when all of (CS1#), (CS2), (WE#) and (one or both of LB# and UB#) become active.

A write is performed during the overlap of a low CS1#, a high CS2, a low WE# and a low LB# or a low UB#.

A write ends when any of (CS1#), (CS2), (WE#) or (one or both of LB# and UB#) becomes inactive.

Write Cycle (4)[*35] (LB#, UB# CLOCK, Word Mode)
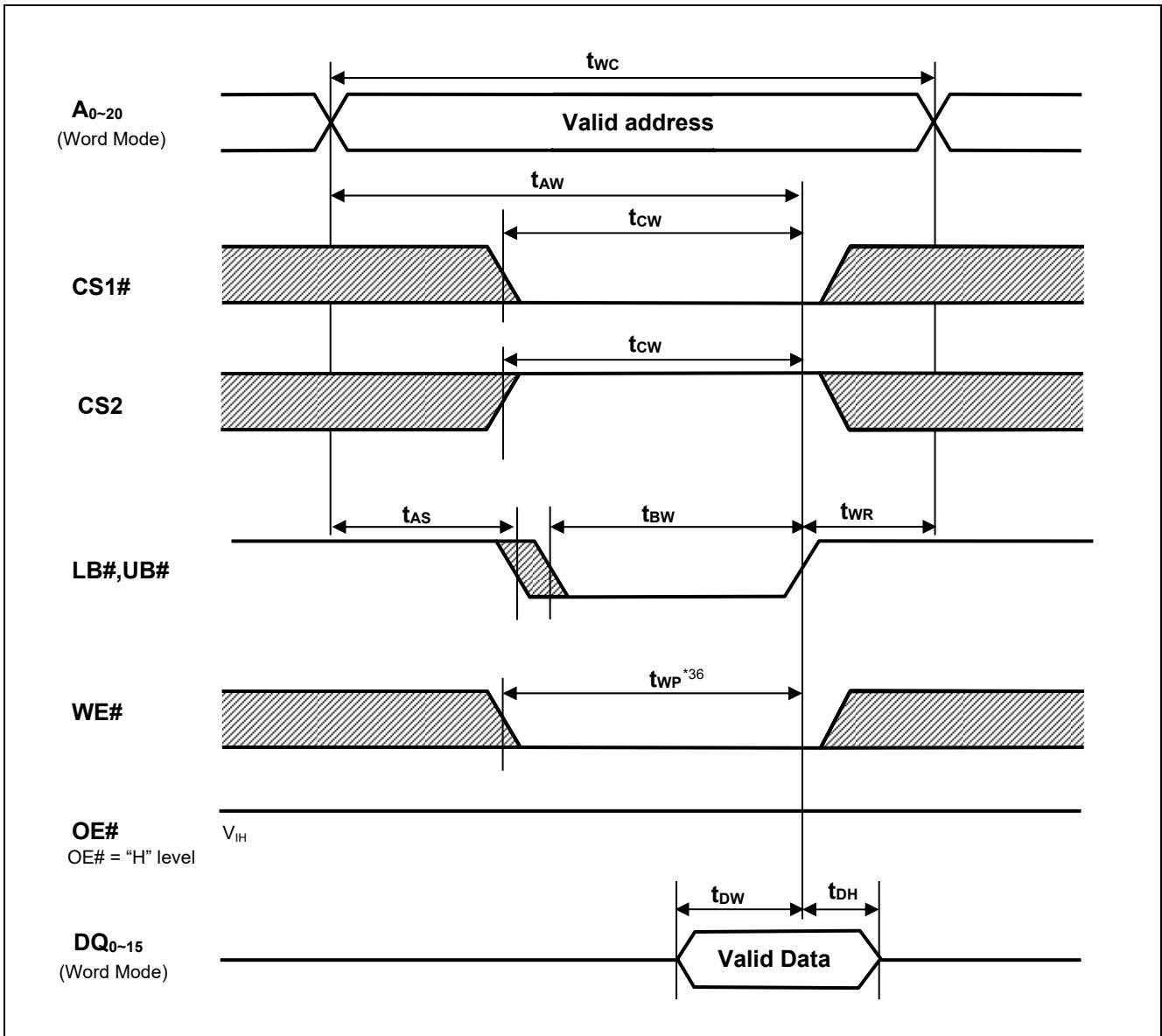
Note 35. BYTE# pin supported by only 48pin TSOP (I) and 52pin µTSOP (II) types.

BYTE# ≥ Vcc - 0.2V (Word mode)

36. t_{WP} is the interval between write start and write end.

A write starts when all of (CS1#), (CS2), (WE#) and (one or both of LB# and UB#) become active.

A write is performed during the overlap of a low CS1#, a high CS2, a low WE# and a low LB# or a low UB#.

A write ends when any of (CS1#), (CS2), (WE#) or (one or both of LB# and UB#) becomes inactive.

Low V$_{CC}$ Data Retention Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test conditions[37,38]	

V$_{CC}$ for data retention	V$_{DR}$	1.5	—	3.6	V	Vin ≥ 0V
						(1) CS2 ≤ 0.2V or
						(2) CS1# ≥ V$_{CC}$-0.2V,
						    CS2 ≥ V$_{CC}$-0.2V or
						(3) LB# = UB# ≥ V$_{CC}$-0.2V,
						    CS1# ≤ 0.2V, CS2 ≥ V$_{CC}$-0.2V	

Data retention current	I$_{CCDR}$	—	0.6[39]	4	µA	~+25°C	Vin ≥ 0V
							(1) CS2 ≤ 0.2V or
							(2) CS1# ≥ V$_{CC}$-0.2V,
							    CS2 ≥ V$_{CC}$-0.2V or
							(3) LB# = UB# ≥ V$_{CC}$-0.2V,
							    CS1# ≤ 0.2V,
							    CS2 ≥ V$_{CC}$-0.2V

		—	1[40]	6	µA	~+40°C	
		—	4[41]	17	µA	~+70°C	
		—	8[42]	24	µA	~+85°C	
Chip deselect time to data retention	t$_{CDR}$	0	—	—	ns	See retention waveform.	
Operation recovery time	t$_R$	5	—	—	ms		

Note 37. BYTE# pin supported by only 48pin TSOP (I) and 52pin µTSOP (II) types.
BYTE# ≥ Vcc - 0.2V or BYTE# ≤ 0.2V

38. CS2 controls address buffer, WE# buffer, CS1# buffer, OE# buffer, LB# buffer, UB# buffer and DQ buffer.
If CS2 controls data retention mode, Vin levels (address, WE#, CS1#, OE#, LB#, UB#, DQ) can be in the high impedance state. If CS1# controls data retention mode, CS2 must be CS2 ≥ V$_{CC}$-0.2V or CS2 ≤ 0.2V.
The other inputs levels (address, WE#, OE#, LB#, UB#, DQ) can be in the high-impedance state.

39. Typical parameter indicates the value for the center of distribution at 3.0V (Ta=25ºC), and not 100% tested.

40. Typical parameter indicates the value for the center of distribution at 3.0V (Ta=40ºC), and not 100% tested.

41. Typical parameter indicates the value for the center of distribution at 3.0V (Ta=70ºC), and not 100% tested.

42. Typical parameter indicates the value for the center of distribution at 3.0V (Ta=85ºC), and not 100% tested.

Low Vcc Data Retention Timing Waveforms (CS1# controlled)[43]
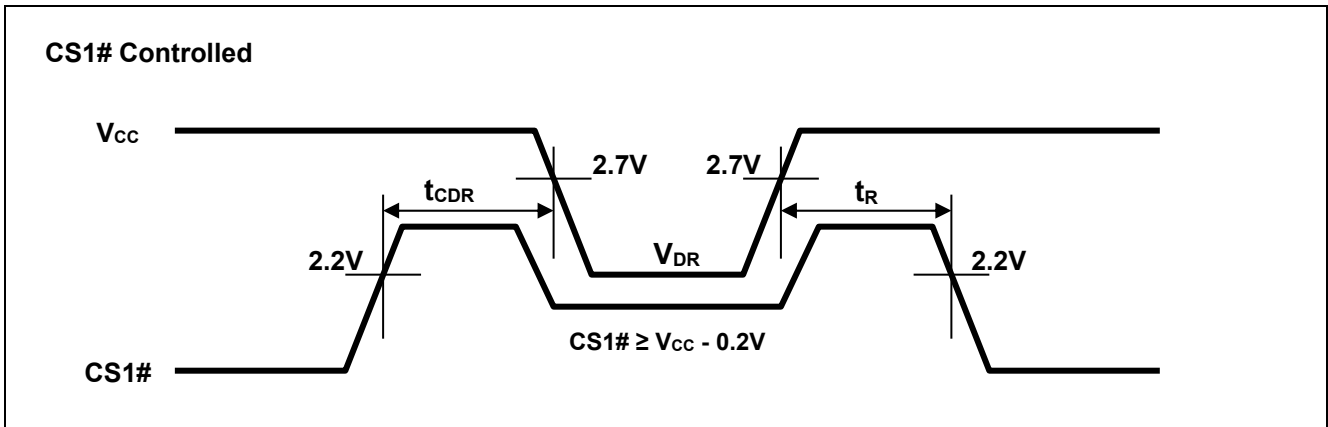
Low Vcc Data Retention Timing Waveforms (CS2 controlled)[43]
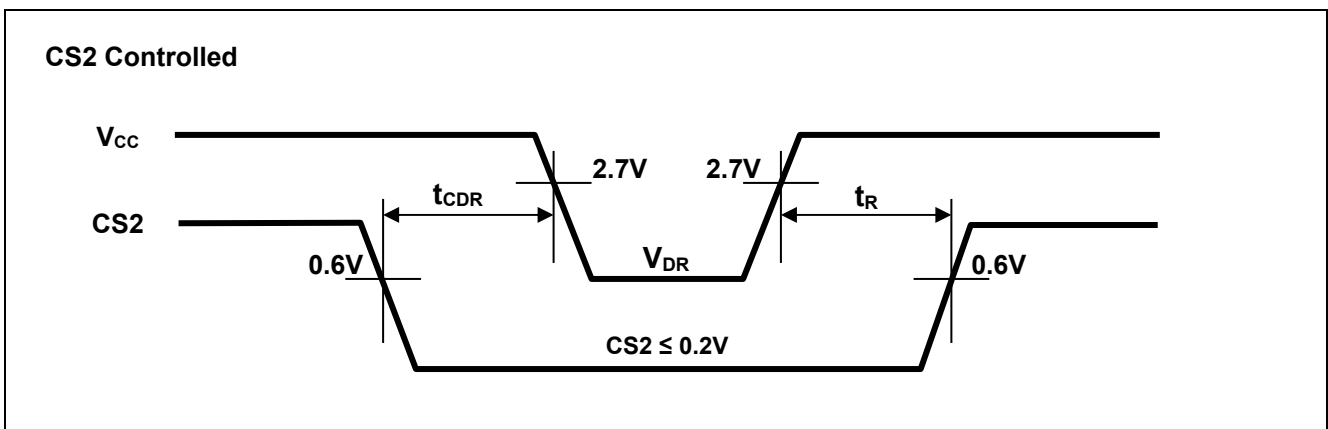
Low Vcc Data Retention Timing Waveforms (LB#,UB# controlled, Word Mode)[44]
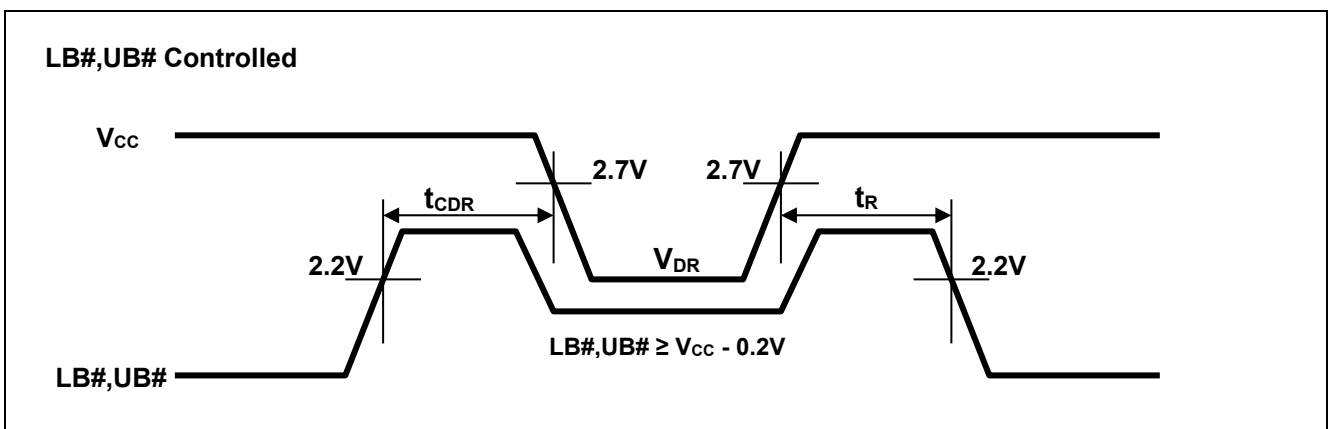
Note 43. BYTE# pin supported by only 48pin TSOP (I) and 52pin µTSOP (II) types.
BYTE# ≥ Vcc - 0.2V or BYTE# ≤ 0.2V

44. BYTE# pin supported by only 48pin TSOP (I) and 52pin µTSOP (II) types.
BYTE# ≥ Vcc - 0.2V (Word mode)

Revision History	RMLV3216A Series Data Sheet

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<tr><td rowspan="2">Rev.</td><td rowspan="2">Date</td><td colspan="2" style="text-align:center">Description</td></tr>
<tr><td>Page</td><td>Summary</td></tr>
<tr><td>1.00</td><td>2018.12.26</td><td>—</td><td>First Edition issued</td></tr>
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