PRELIMINARY

CY2284

100-MHz Clock Synthesizer/Driver for Desktop PCs with Aladdin V Chipset, USB and AGP

Features

- **Mixed 2.5V and 3.3V operation**
- **Clock Generator for AMD K6, Pentium® II, and other similar processor-based motherboards**
  - **Three 2.5V or 3.3V CPU clocks, running at 66.66, 75, 83.33, and 100 MHz**
  - **Five 3.3V PCI clocks**
  - **One 3.3V 48 MHz USB clock**
  - **One 3.3V REF clock at 14.318 MHz**
  - **Two AGP clocks at 60 or 66.66 MHz**
- **Independent power supplies for clock sets, ensuring lowest possible noise and jitter**
- **EMI control with factory EPROM programmable output drive and slew rate**
- **Low skew outputs**
- **Available in space-saving 28-pin SOIC package**

Functional Description

The CY2284 is a clock synthesizer/driver for a AMD K6, Pentium II, or other similar processor-based PCs requiring 100-MHz support. The CY2284 outputs three CPU clocks at 2.5V or 3.3V. There are five PCI clocks to support the chipset and PCI slots. There are two AGP clocks, running at either 60 or 66 MHz, depending on the CPU clock frequency. Additionally, the part outputs one 3.3V USB clock at 48 MHz, and one 3.3V reference clock at 14.318 MHz.

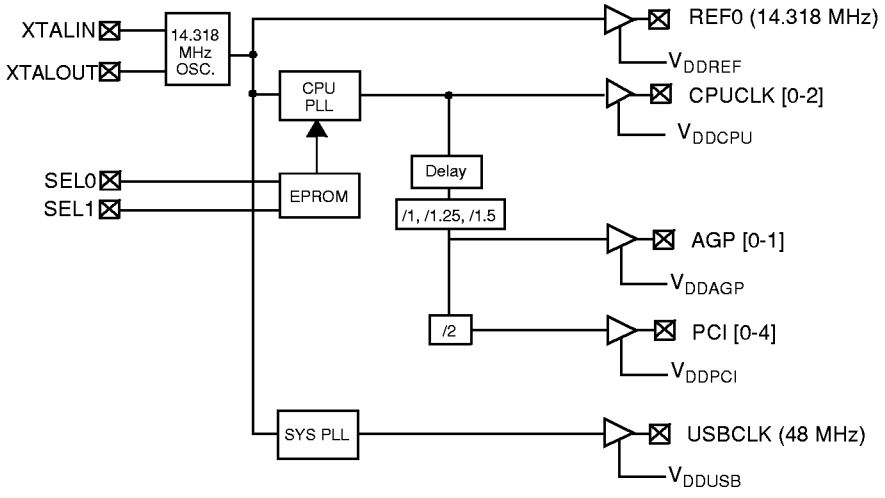
A summary of clock outputs for the device is shown below.

The CY2284 outputs are designed for low EMI emissions. Controlled rise and fall times, unique output driver circuits, and factory-EPROM programmable output drive and slew-rate enable optimal configurations for EMI control.

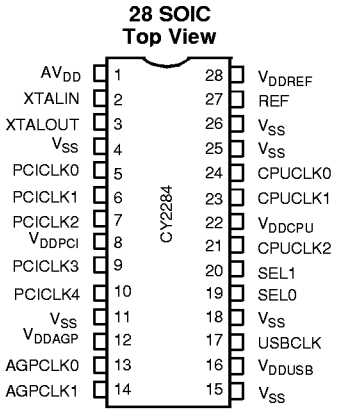
CY2284 Selector Guide

Clock Outputs	CY2284-1
CPU (66.6, 75, 83.33, 100 MHz)	3
PCI (CPU/2, CPU/2.5, CPU/2.5, CPU/3 MHz)	5
AGP (CPU, CPU/1.25, CPU/1.5 MHz)	2
USB (48 MHz)	1
REF (14.318 MHz)	1
CPU-PCI delay	1.5–4.0 ns
AGP clock	In phase with PCI

Logic Block Diagram



Pin Configuration



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Pin Summary

Name	Pins	Description
V_{DDPCI}	8	3.3V Digital voltage supply for PCI clocks
V_{DDUSB}	16	3.3V Digital voltage supply for USB clocks
V_{DDREF}	28	3.3V Digital voltage supply for REF clocks
V_{DDAGP}	12	3.3V Digital voltage supply for AGP clocks
V_{DDCPU}	22	2.5V or 3.3V Digital voltage supply for CPU clocks
AV_{DD}	1	3.3V Analog voltage supply
V_{SS}	4, 11, 15, 18, 25, 26	Ground
XTALIN[1]	2	Reference crystal input
XTALOUT[1]	3	Reference crystal feedback
SEL0, SEL1	19, 20	CPU frequency select input (see table below)
CPUCLK[0:2]	24, 23, 21	CPU clock outputs
PCICLK[0:4]	5, 6, 7, 9, 10	PCI clock outputs
AGPCLK[0:1]	13, 14	AGP clock outputs
REF	27	3.3V Reference clock output
USBCLK	17	USB clock output

Function Table

SEL1	SEL0	CPU/PCI Ratio	CPUCLK (MHz)	PCICLK (MHZ)	AGP (MHz)	REF (MHz)	USBCLK (MHz)
0	0	2	66.8	33.4	66.8	14.318	48.008
0	1	2.5	75.0	30.0	60.0	14.318	48.008
1	0	2.5	83.33	33.33	66.66	14.318	48.008
1	1	3	100	33.33	66.66	14.318	48.008

Actual Clock Frequency Values

Clock Output	Target Frequency (MHz)	Actual Frequency (MHz)	PPM
CPUCLK	66.67	66.8	2222
CPUCLK	75	75	0
CPUCLK	83.33	83.14	–2306
CPUCLK	100	99.8	–1938
USBCLK	48.0	48.008	167

Note:
1. For best accuracy, use a parallel-resonant crystal, C_{LOAD} = 18 pF.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Supply Voltage .....–0.5 to +7.0V

Input Voltage ..... –0.5V to V_{DD}+0.5

Storage Temperature (Non-Condensing) ... –65°C to +150°C

Max. Soldering Temperature (10 sec) ..... +260°C

Junction Temperature ..... +150°C

Package Power Dissipation 1W

Static Discharge Voltage ..... >2000V (per MIL-STD-883, Method 3015)

Operating Conditions[2]

Parameter	Description	Min.	Max.	Unit
AV_{DD}, V_{DDPCI}, V_{DDUSB}, V_{DDREF}, V_{DDAGP}	Analog and Digital Supply Voltage	3.135	3.465	V
V_{DDCPU}	CPU Supply Voltage	2.375 3.135	2.625 3.465	V
T_A	Operating Temperature, Ambient	0	70	°C
C_L	Max. Capacitive Load on CPUCLK PCICLK, AGPCLK REF USB		 20 30 20 20	pF
$f_{(REF)}$	Reference Frequency, Oscillator Nominal Value	14.318	14.318	MHz

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions			Min.	Max.	Unit
V_{IH}	High-level Input Voltage	Except Crystal Inputs[3]			2.0		V
V_{IL}	Low-level Input Voltage	Except Crystal Inputs[3]				0.7	V
V_{OH}	High-level Output Voltage	V_{DDCPU} = 2.375V	I_{OH} = 12 mA	CPUCLK	2.0		V
V_{OL}	Low-level Output Voltage	V_{DDCPU} = 2.375V	I_{OL} = 12 mA	CPUCLK		0.4	V
V_{OH}	High-level Output Voltage	V_{DDPCI}, AV_{DD}, V_{DDREF}, V_{DDUSB}, V_{DDAGP} = 3.135V	I_{OH} = 14.5 mA	PCICLK AGPCLK	2.4		V
			I_{OH} = 16 mA	USBCLK			
			I_{OH} = 16 mA	REF			
V_{OL}	Low-level Output Voltage	V_{DDPCI}, AV_{DD}, V_{DDREF}, V_{DDUSB}, V_{DDAGP} = 3.135V	I_{OL} = 9.4 mA	PCICLK AGPCLK		0.4V	V
			I_{OL} = 9 mA	USBCLK			
			I_{OL} = 9 mA	REF			
I_{IH}	Input High Current	V_{IH} = V_{DD}			–10	+10	µA
I_{IL}	Input Low Current	V_{IL} = 0V				10	µA
I_{DD25}	Power Supply Current for 2.5V clocks	V_{DDCPU} = 2.625V, V_{IN} = 0 or V_{DD}, Loaded Outputs, CPU = 66.6 MHz				70	mA
I_{DD25}	Power Supply Current for 2.5V clocks	V_{DDCPU} = 2.625V, V_{IN} = 0 or V_{DD}, Loaded Outputs, CPU = 100 MHz				100	mA
I_{DD33}	Power Supply Current for 3.3V clocks	V_{DD} = 3.465V, V_{IN} = 0 or V_{DD}, Loaded Outputs				170	mA

Notes:

2. Electrical parameters are guaranteed with these operating conditions.
3. Crystal Inputs have CMOS thresholds.

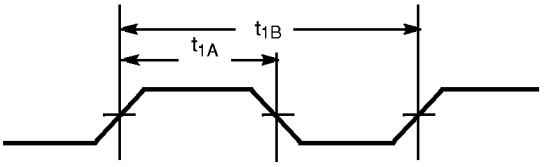
Switching Characteristics[4] Over the Operating Range

Parameter	Output	Description	Test Conditions	Min.	Typ.	Max.	Unit
t_1	All	Output Duty Cycle[5]	$t_1 = t_{1A} \div t_{1B}$	45	50	55	%
t_2	CPUCLK	CPU Clock Rising and Falling Edge Rate	Between 0.4V and 2.0V	0.75		4.0	V/ns
t_2	PCICLK, AGCLK, REF	PCI, AGP, REF Clock Rising and Falling Edge Rate	Between 0.4V and 2.4V	0.85		4.0	V/ns
t_2	USBCLK	USB Rising and Falling Edge Rate	Between 0.4V and 2.4V	0.5		2.0	V/ns
t_3	CPUCLK	CPU-CPU Clock Skew	Measured at 1.25V for 2.5V clocks Measured at 1.5V for 3.3V clocks		100	500	ps
t_4	AGPCLK, PCICLK	AGP-PCI Clock Skew	Measured at 1.5V for 3.3V clocks		250	1200	ps
t_5	CPUCLK, PCICLK	CPU-PCI Clock Skew [6]	Measured at 1.25V for 2.5V clocks, and at 1.5V for 3.3V clocks	1.0		4.0	ns
t_6	PCICLK, PCICLK	PCI-PCI Clock Skew	Measured at 1.5V			500	ps
t_7	AGPCLK	Cycle-Cycle Clock Jitter	Measured at 1.5V		250	800	ps
t_8	CPUCLK	Cycle-Cycle Clock Jitter	Measured at 1.25V		200	500	ps
t_9	PCICLK	Cycle-Cycle Clock Jitter	Measured at 1.5V		250	750	ps
t_{10}	CPUCLK, PCICLK	Power-up Time	CPU, PCI clock stabilization from power-up			3	ms

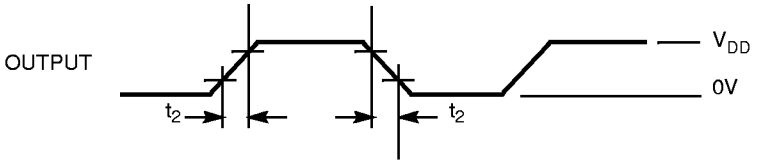
Notes:
4. All parameters specified with loaded outputs.
5. Duty cycle is measured at 1.5V when V_{DD} = 3.3V. When V_{DD} = 2.5V, duty cycle is measured at 1.25V.
6. PCI lags CPU.

Switching Waveforms

Duty Cycle Timing

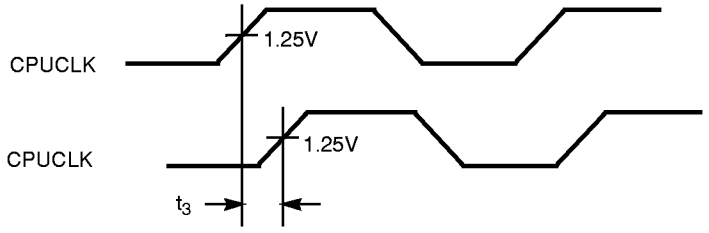


All Outputs Rise/Fall Time

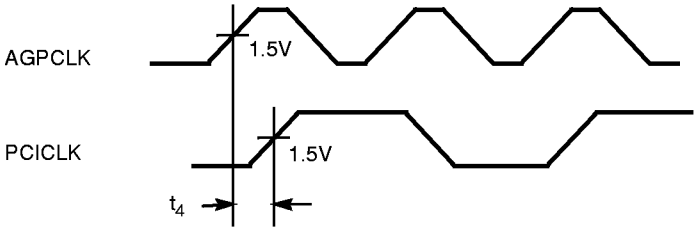


Switching Waveforms (continued)

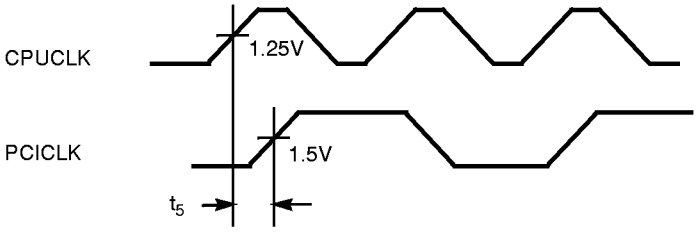
CPU-CPU Clock Skew



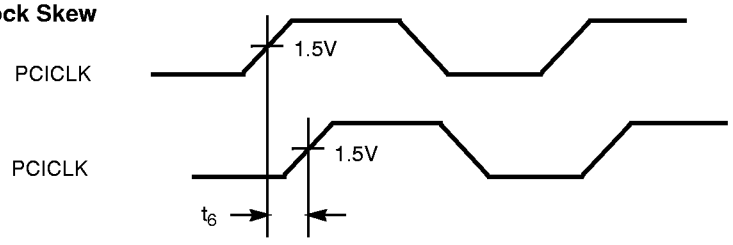
AGP-PCI Clock Skew



CPU-PCI Clock Skew



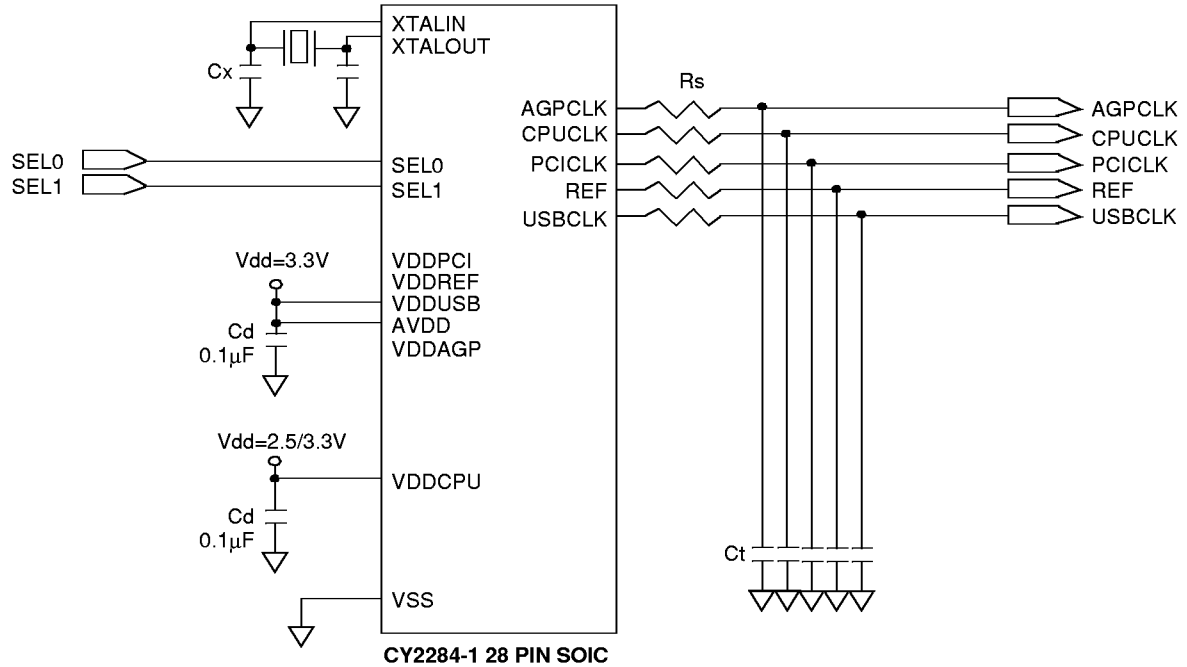
PCI-PCI Clock Skew



Application Information

Clock traces must be terminated with either series or parallel termination, as they are normally done.

Application Circuit



CY2284-1 28 PIN SOIC

Cd = DECOUPLING CAPACITORS
Ct = OPTIONAL EM-REDUCING CAPACITORS
Cx = OPTIONAL LOAD MATCHING CAPACITOR
Rs = SERIES TERMINATING RESISTORS

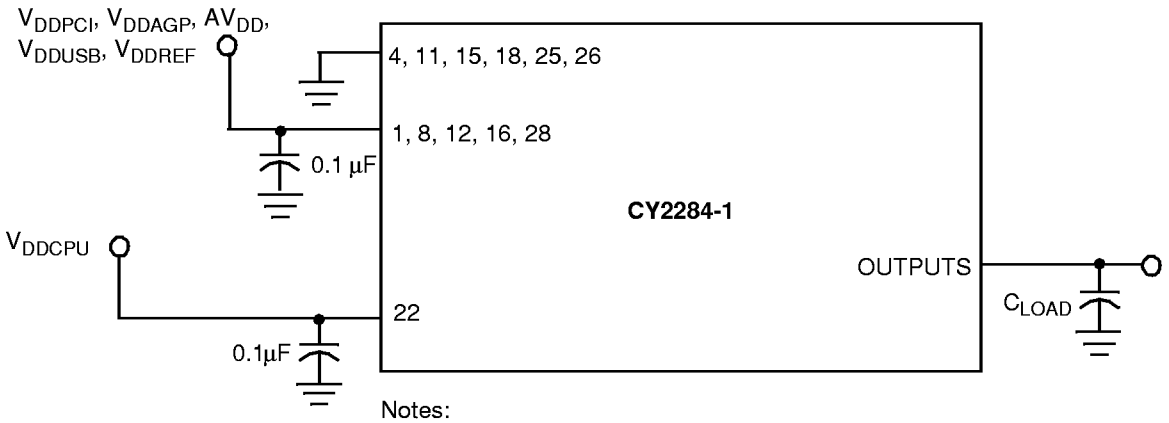
Summary

- A parallel-resonant crystal should be used as the reference to the clock generator. The operating frequency and CLOAD of this crystal should be as specified in the data sheet. Optional trimming capacitors may be needed if a crystal with a different CLOAD is used. Footprints must be laid out for flexibility.
- Surface mount, low-ESR, ceramic capacitors should be used for filtering. Typically, these capacitors have a value of 0.1 µF. In some cases, smaller value capacitors may be required.
- The value of the series terminating resistor satisfies the following equation, where Rtrace is the loaded characteristic impedance of the trace, Rout is the output impedance of the clock generator (specified in the data sheet), and Rseries is the series terminating resistor.

  $$R_{series} > R_{trace} - R_{out}$$

- Footprints must be laid out for optional EMI-reducing capacitors, which should be placed as close to the terminating resistor as is physically possible. Typical values of these capacitors range from 4.7 pF to 22 pF.
- A Ferrite Bead **may** be used to isolate the Board VDD from the clock generator VDD island. Ensure that the Ferrite Bead offers greater than 50Ω impedance at the clock frequency, under loaded DC conditions. Please refer to the application note "Layout and Termination Techniques for Cypress Clock Generators" for more details.
- If a Ferrite Bead is used, a 10 µF–22 µF tantalum bypass capacitor should be placed close to the Ferrite Bead. This capacitor prevents power supply droop during current surges.

Test Circuit



Notes:
Each supply pin must have an individual decoupling capacitor
All capacitors must be placed as close to the pins as is possible.

Ordering Information

Ordering Code	Package Name	Package Type	Operating Range
CY2284SC–1	S21	28-Pin SOIC	Commercial

Document #: 38–00697

Package Diagram

28-Lead (300-Mil) Molded SOIC S21