4 Megabit Static RAM
512K x 8-Bit

Features

- High speed access times
  Com'l: 15, 17, 20, 25, 35 and 45 ns
  Ind: 17, 20, 25, 35, and 45 ns
- TTL compatible inputs and outputs
- Single +5V (±10%) power supply
- Three-State Output
- Packages
  Plastic SOJ (400 mil) - SO
  Ceramic Flatpack (500 mil) -F

Description

The PDM41096 is a high-performance CMOS static RAM organized as 524,288 x 8 bits. This product is produced in Paradigm's proprietary CMOS technology which offers the designer the highest speed parts. Writing is accomplished when the write enable ($\overline{WE}$) and the chip enable ($\overline{CE}$) inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ and $\overline{OE}$ are both LOW.

The PDM41096 operates from a single +5V power supply and all the inputs and outputs are fully TTL compatible. The PDM41096 comes in two versions, the standard power version PDM41096S and a low power version the PDM41096L. The two versions are functionally the same and only differ in their power consumption.

The PDM41096 is available in a 36-pin 400 mil Plastic SOJ abd a 500 mil Ceramic Flatpack.

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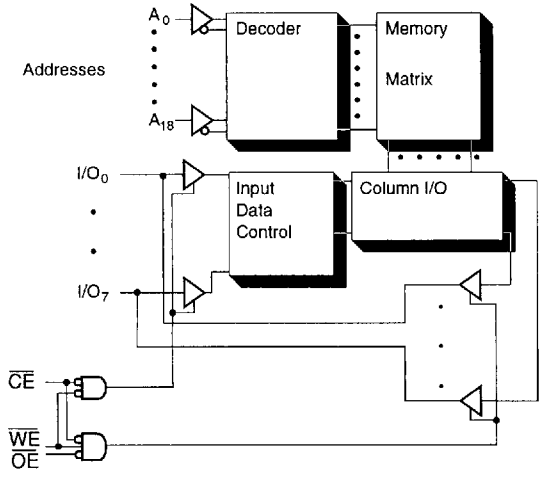
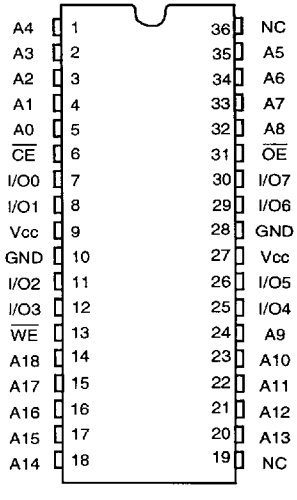
Functional Block Diagram



Pin Configuration

SOJ, Flatpack



Truth Table[1]

$\overline{OE}$	$\overline{WE}$	$\overline{CE}$	I/O	MODE
X	X	H	Hi-Z	Standby
L	H	L	D_{OUT}	Read
X	L	L	D_{IN}	Write
H	H	L	Hi-Z	Output Disable

NOTE: 1. H = V_{IH}, L = V_{IL}, X = DON'T CARE

Absolute Maximum Ratings [1]

Symbol	Rating	Com'l./ Ind.	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
T_{BIAS}	Temperature Under Bias	–55 to +125	°C
T_{STG}	Storage Temperature	–55 to +125	°C
P_T	Power Dissipation	1.4	W
I_{OUT}	DC Output Current	50	mA

NOTE: 1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
Commercial	Ambient Temperature	0	25	70	°C

DC Electrical Characteristics (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Conditions		PDM41096S Min.	PDM41096S Max.	PDM41096 L Min.	PDM41096 L Max.	Unit
I_{LI}	Input Leakage Current	V_{CC} = MAX., V_{IN} = GND to V_{CC}	Com'l	–5	5	–2	2	µA
I_{LO}	Output Leakage Current	V_{CC} = MAX., $\overline{CE}$ = V_{IH}, V_{OUT} = GND to V_{CC}	Com'l	–5	5	–2	2	µA
V_{IH}	Input High Voltage			2.2	6.0	2.2	6.0	V
V_{IL}	Input Low Voltage			–0.5(1)	0.8	–0.5(1)	0.8	V
V_{OL}	Output Low Voltage	I_{OL} = 8 mA, V_{CC} = Min. I_{OL} = 10 mA, V_{CC} = Min.		— —	0.4 0.5	— —	0.4 0.5	V V
V_{OH}	Output High Voltage	I_{OH} = –4 mA, V_{CC} = Min.		2.4	—	2.4	—	V

NOTE: 1. V_{IL}(min) = –3.0V for pulse width less than 20 ns.

Power Supply Characteristics

Symbol	Parameter	Power	-15	-17	-20	-25	-35, -45	Unit
I_{CC}	Operating Current $\overline{CE} \geq V_{IL}$	S	280	270	250	220	200	mA
	V_{CC} = Max., f = f_{MAX} = 1/trc I_{OUT} = 0 mA	L	240	230	210	180	160	mA
I_{SB}	Standby Current (TTL Level)	S	130	120	110	100	90	mA
	$\overline{CE} \geq V_{IH}$ V_{CC} = Max., f = f_{MAX} = 1/trc	L	100	90	80	70	60	mA
I_{SB1}	Full Standby Current (CMOS Level)	S	40	40	40	40	40	mA
	$\overline{CE} \geq V_{IH}$ V_{CC} = Max., f = 0 = 1/trc $V_{IN} \geq V_{CC} - 0.2V$ or $\leq 0.2V$	L	20	20	20	20	20	mA

SHADED AREA = PRELIMINARY DATA.

NOTE: All values are maximum guaranteed values.
$V_{LC} \leq 0.2V$, $V_{HC} \geq V_{CC} - 0.2V$.

Capacitance(1) (T_A = +25°C, f=1.0 MHz)

Symbol	Parameter	Max.	Unit
C_{IN}	Input Capacitance	8	pF
C_{OUT}	Output Capacitance	8	pF

NOTE: 1. This parameter is determined by device characterization but is not production tested.

AC Test Conditions

Input Pulse Levels	GND to 3.0V
Input rise and fall times	5 ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See figures 1 and 2

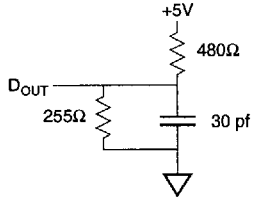


Figure 1. Output Load Equivalent

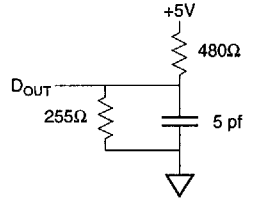
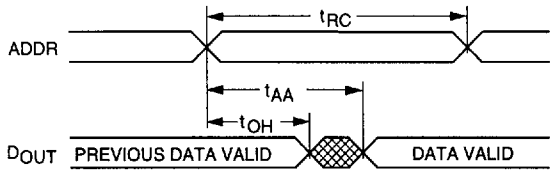
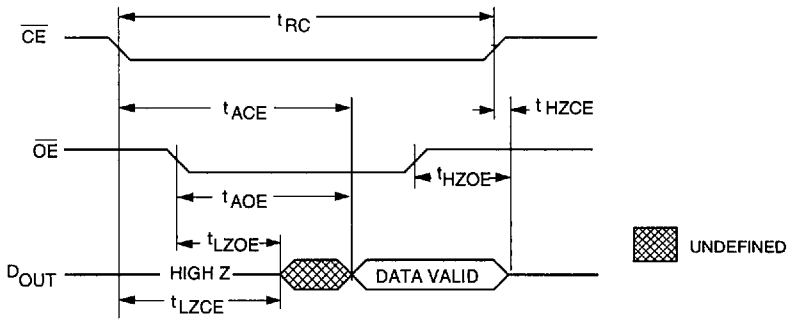


Figure 2. Output Load Equivalent (for t_{LZCE}, t_{HZCE}, t_{LZWE}, t_{HZWE}, t_{LZOE}, t_{HZOE})

Read Cycle No. 1[6, 7]



Read Cycle No. 2[3, 6, 8]



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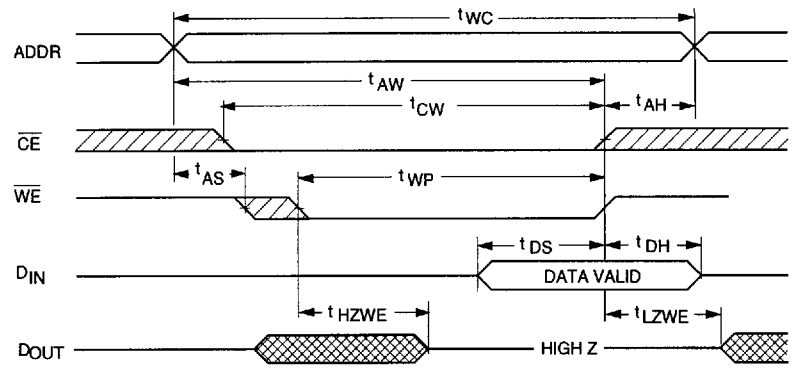
AC Electrical Characteristics (V_{CC} = 5V ± 10%, All Temperature Ranges)

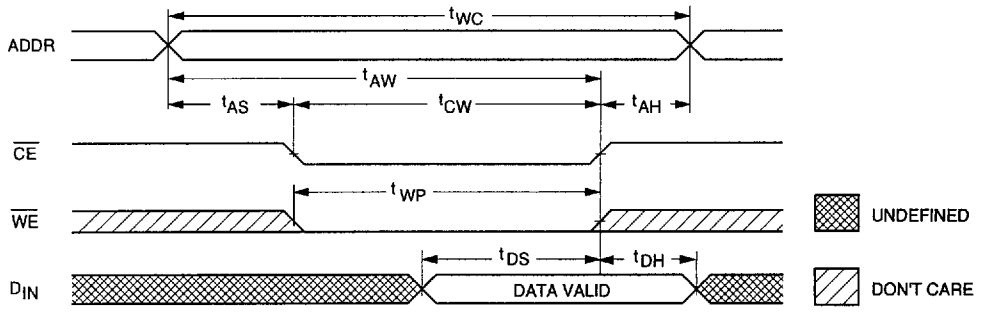
Description		-15[6]		-17[8]		-20		-25		-35		-45		
READ Cycle	**Symbol**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
READ Cycle time	t_{RC}	15		17		20		25		35		45		ns
Address access time	t_{AA}		15		17		20		25		35		45	ns
Chip enable access time	t_{ACE}		15		17		20		25		35		45	ns
Output hold from address change	t_{OH}	5		5		5		5		5		5		ns
Chip enable to output in low Z[2, 4]	t_{LZCE}	5		5		5		5		5		5		ns
Chip disable to output in high Z[2, 3, 4]	t_{HZCE}		6		7		8		10		15		18	ns
Chip enable to power up time[4]	t_{PU}	0		0		0		0		0		0		ns
Chip disable to power down time[4]	t_{PD}		15		17		20		25		35		45	ns
Output enable access time	t_{AOE}		6		7		8		10		12		15	ns
Output Enable to output in low Z[2, 4]	t_{LZOE}	0		0		0		0		0		0		ns
Output disable to output in high Z[2, 4]	t_{HZOE}		6		7		8		10		12		15	ns

SHADED AREA = PRELIMINARY DATA.
Notes referenced are after Data Retention Table.

Write Cycle No. 1 (Write Enable Controlled)



Write Cycle No. 2 (Chip Enable Controlled)

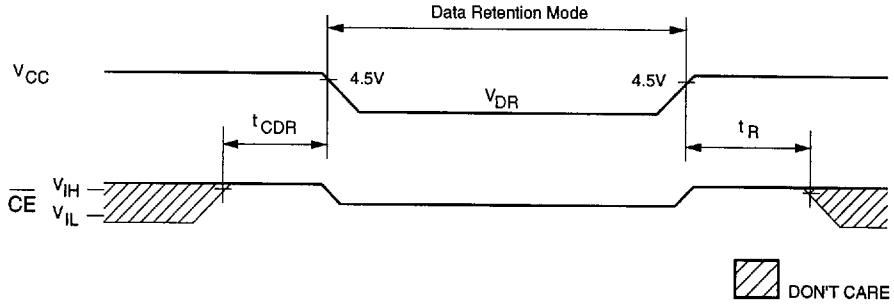


AC Electrical Characteristics (V_{CC} = 5V ± 10%, All Temperature Ranges)

Description		-15[8]		-17[8]		-20		-25		-35		-45		
WRITE Cycle	**Symbol**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
WRITE Cycle time	t_{WC}	15		17		20		25		35		45		ns
Chip enable to end of write	t_{CW}	12		15		15		20		25		25		ns
Address Valid to end of write	t_{AW}	12		15		15		20		25		25		ns
Address setup time	t_{AS}	0		0		0		0		0		0		ns
Address hold from end of write	t_{AH}	0		0		0		0		0		0		ns
Write pulse width	t_{WP}	11		12		12		20		25		25		ns
Data setup time	t_{DS}	8		9		10		15		20		20		ns
Data hold time	t_{DH}	0		0		0		0		0		0		ns
Write disable to output in low Z[2, 3]	t_{LZWE}	0		0		0		0		0		0		ns
Write enable to output in high Z[2, 3]	t_{HZWE}		6		7		8		10		15		20	ns

SHADED AREA = PRELIMINARY DATA.
Notes referenced are after Data Retention Table.

Low V_{CC} Data Retention Waveform



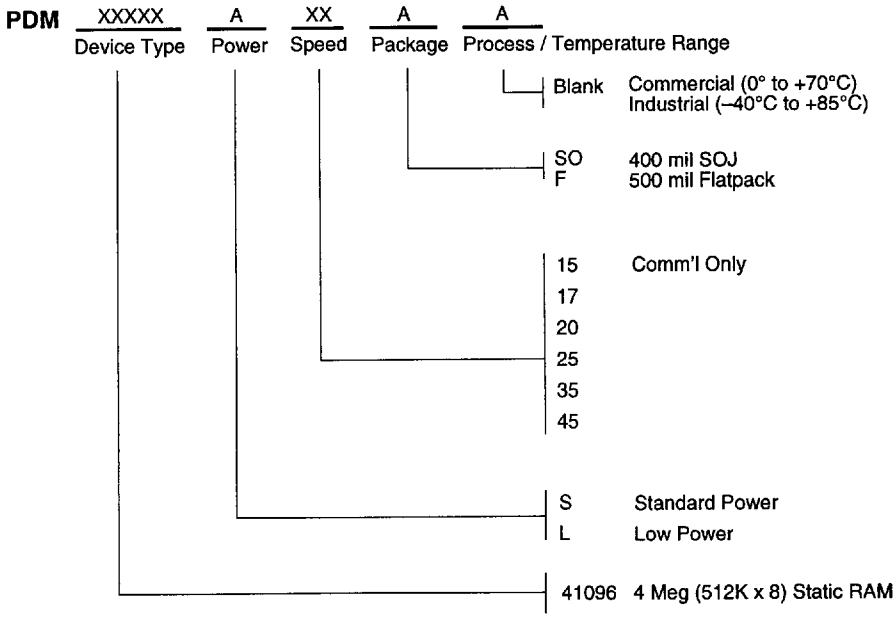
Data Retention Electrical Characteristics (L Version Only)

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
V_{DR}	V_{CC} for Retention Data			2	—	—	V
I_{CCDR}	Data Retention Current	$\overline{CE} \geq V_{CC} - 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $\leq 0.2V$	V_{CC} = 2V Com'l	—	—	1,000	µA
			V_{CC} = 3V Com'l	—	—	1,500	µA
t_{CDR}	Chip Deselect to Data Retention Time			0	—	—	ns
t_R(4)	Operation Recovery Time			t_{RC}(5)	—	—	ns

NOTES: (For 3 previous Electrical Characteristics tables)

1. –55°C to + 125°C temperature range only.
2. The parameter is tested with CL = 5 pF as shown in Fig. #2. Transition is measured ±200 mV from steady state voltage.
3. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}.
4. This parameter is sampled.
5. t_{RC} = Read cycle time.
6. $\overline{WE}$ is high for a READ cycle.
7. The device is continuously selected. All the Chip Enables are held in their active state.
8. V_{CC} = 5V ± 5%.

Ordering Information



Chip	Package Type
PDM41096	36-pin SOJ 400 Mil 36-pin Flatpack 500 Mil