M82C84A
CHMOS CLOCK GENERATOR AND DRIVER FOR M80C86 PROCESSOR

Military

- **Generates the System Clock for the M80C86 Processor: M82C84A for 8 MHz**
- **Pin Compatible with Bipolar M8284A***
- **Uses a Crystal or an External Frequency Source**
- **Provides Local READY and MULTIBUS® READY Synchronization**
- **Military Temperature T Range −55°C to +125°C (T_C)**
- **Generates System Reset Output from Schmitt Trigger Input**
- **Capable of Clock Synchronization with other M82C84As**
- **Low Power Consumption**
- **Single 5V Power Supply**
- **TTL Compatible Inputs/Outputs**
- **Available in 18-Lead DIP**

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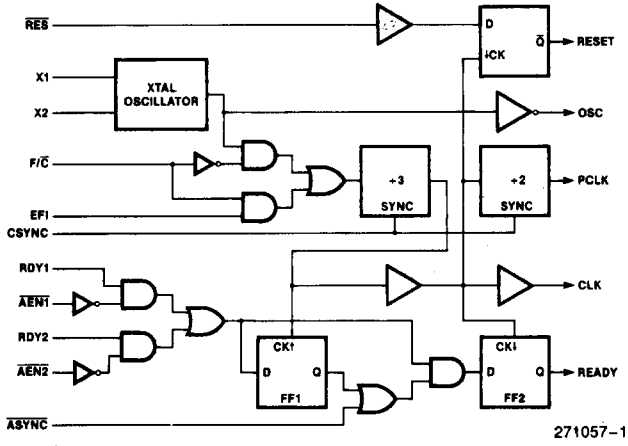
The Intel M82C84A is a high performance CHMOS clock generator-driver designed to service the requirements of the M80C86 and M8086. Power consumption is a fraction of that of equivalent bipolar circuits. The chip contains a crystal controlled oscillator, a divide-by-three counter and complete READY synchronization and reset logic. Crystal controlled operation up to 15, 25 MHz utilizes a parallel, fundamental mode crystal and two small load capacitors.

*The Bipolar M8284A requires two load resistors and a resonant crystal.



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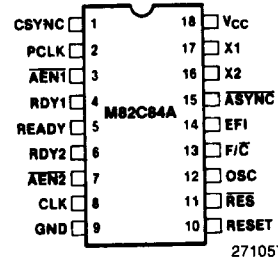
M82C84A Block Diagram

M82C84A Pin Description

Control Pin	Logical 1	Logical 0
F/$\overline{C}$	External Clock	Crystal Drive
$\overline{RES}$	Normal	Reset
RDY 1 RDY 2	Bus Ready	Bus not ready
$\overline{AEN1}$ $\overline{AEN2}$	Address Disabled	Address Enabled
$\overline{ASYNC}$	1 Stage Ready Synchronization	2 Stage Ready Synchronization



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M82C84A 18-Lead DIP Configuration

September 1990
Order Number: 271057-006

Table 1. Pin Description

Symbol	Type	Name and Function
$\overline{AEN1}$, $\overline{AEN2}$	I	**ADDRESS ENABLE:** $\overline{AEN}$ is an active LOW signal. AEN serves to qualify its repective Bus Ready Signal (RDY1 or RDY2). $\overline{AEN1}$ validates RDY1 while $\overline{AEN2}$ validates RDY2. Two AEN signal inputs are useful in system configurations which permit the processor to access two Multi-Master System Busses. In non Multi-Master configurations the $\overline{AEN}$ signal inputs are tied true (LOW).
RDY1, RDY2	I	**BUS READY:** (Transfer Complete). RDY is an active HIGH signal which is an indication from a device located on the system data bus that data has been received, or is available. RDY1 is qualified by $\overline{AEN1}$ while RDY2 is qualified by $\overline{AEN2}$.
$\overline{ASYNC}$	I	**READY SYNCHRONIZATION SELECT:** $\overline{ASYNC}$ is an input which defines the synchronization mode of the READY logic. When $\overline{ASYNC}$ is LOW, two stages of READY synchronization are provided. When $\overline{ASYNC}$ is left open (an internal pull-up is provided) or HIGH a single stage of READY synchronization is provided.
READY	O	**READY:** READY is an active HIGH signal which is the synchronized RDY signal input. READY is cleared after the guaranteed hold time to the processor has been met.
X1, X2	I	**CRYSTAL IN:** X1 and X2 are the pins to which a crystal is attached. The crystal frequency is 3 times the desired processor clock frequency. (If no crystal is attached, then X1 should be tied to V_{CC} or GND and X2 should be left open.)
F/$\overline{C}$	I	**FREQUENCY/CRYSTAL SELECT:** F/$\overline{C}$ is a strapping option. When strapped LOW, F/$\overline{C}$ permits the processor's clock to be generated by the crystal. When F/$\overline{C}$ is strapped HIGH, CLK is generated from the EFI input.
EFI	I	**EXTERNAL FREQUENCY:** When F/$\overline{C}$ is strapped HIGH, CLK is generated from the input frequency appearing on this pin. The input signal is a square wave 3 times the frequency of the desired CLK output. When F/$\overline{C}$ is strapped LOW, EFI should be tied HIGH or LOW.
CLK	O	**PROCESSOR CLOCK:** CLK is the clock output used by the processor and all devices which directly connect to the processor's local bus (i.e., the bipolar support chips and other MOS devices). CLK has an output frequency which is 1/3 of the crystal or EFI input frequency and a 1/3 duty cycle.
PCLK	O	**PERIPHERAL CLOCK:** PCLK is a TTL level peripheral clock signal whose output frequency is 1/2 that of CLK and has a 50% duty cycle.
OSC	O	**OSCILLATOR OUTPUT:** OSC is the TTL level output of the internal oscillator circuitry. Its frequency is equal to that of the crystal.
$\overline{RES}$	I	**RESET IN:** $\overline{RES}$ is an active LOW signal which is used to generate RESET. The M82C84A provides a Schmitt trigger input so that an RC connection can be used to establish the power-up reset of proper duration.

Table 1. Pin Description (Continued)

Symbol	Type	Name and Function
RESET	O	**RESET:** RESET is an active HIGH signal which is used to reset the M80C86 family processors. Its timing characteristics are determined by $\overline{RES}$.
CSYNC	I	**CLOCK SYNCHRONIZATION:** CSYNC is an active HIGH signal which allows multiple M82C84A's to be synchronized to provide clocks that are in phase. When CSYNC is HIGH the internal counters are reset. When CSYNC goes LOW the internal counters are allowed to resume counting. CSYNC needs to be externally synchronized to EFI. When using the internal oscillator CSYNC should be hardwired to ground.
GND		**GROUND.**
V_{CC}		**POWER:** +5V supply.

FUNCTIONAL DESCRIPTION

Oscillator

The oscillator circuit of the M82C84A is designed primarily for use with an external parallel resonant, fundamental mode crystal from which the basic operating frequency is derived.

The crystal frequency should be selected at three times the required CPU clock. X1 and X2 are the two crystal input crystal connections. For the most stable operation of the oscillator (OSC) output circuit, two capacitors (C1 = C2) as shown in the waveform figures are recommended. The output of the oscillator is buffered and brought out on OSC so that other system timing signals can be derived from this stable, crystal-controlled source.

Capacitors C1, C2 are chosen such that their combined capacitance:

$$CT = \frac{C1 \bullet C2}{C1 + C2} \quad \text{(Including stray capacitance)}$$

matches the load capacitance as specified by the crystal manufacturer. This insures operation within the frequency tolerance specified by the crystal manufacturer.

Clock Generator

The clock generator consists of a synchronous divide-by-three counter with a special clear input that inhibits the counting. This clear input (CSYNC) allows the output clock to be synchronized with an external event (such as another M82C84A clock). It is necessary to synchronize the CSYNC input to the EFI clock external to the M82C84A. This is accomplished with two Schottky flip-flops. The counter output is a 33% duty cycle clock at one-third the input frequency.

The F/$\overline{C}$ input is a strapping pin that selects either the crystal oscillator or the EFI input as the clock for the ÷3 counter. If the EFI input is selected as the clock source, the oscillator section can be used independently for another clock source. Output is taken from OSC.

Clock Outputs

The CLK ouput is a 33% duty cycle MOS clock driver designed to drive the M80C86 processors directly. PCLK is a TTL level peripheral clock signal whose output frequency is ½ that of CLK. PCLK has a 50% duty cycle.

Reset Logic

The reset logic provides a Schmitt trigger input ($\overline{RES}$) and a synchronizing flip-flop to generate the reset timing. The reset signal is synchronized to the falling edge of CLK. A simple RC network can be used to provide power-on reset by utilizing this function of the M82C84A.

READY Synchronization

Two READY inputs (RDY1, RDY2) are provided to accommodate two Multi-Master system busses. Each input has a qualifier ($\overline{AEN1}$ and $\overline{AEN2}$, respectively). The $\overline{AEN}$ signals validate their respective RDY signals. If a Multi-Master system is not being used the $\overline{AEN}$ pin should be tied LOW.

Synchronization is required for all asynchronous active-going edges of either RDY input to guarantee that the RDY setup and hold times are met. Inactive-going edges of RDY in normally ready systems do not require synchronization but must satisfy RDY setup and hold as a matter of proper system design.

The $\overline{\text{ASYNC}}$ input defines two modes of READY synchronization operation.

When $\overline{\text{ASYNC}}$ is LOW, two stages of synchronization are provided for active READY input signals. Positive-going asynchronous READY inputs will first be synchronized to flip-flop one at the rising edge of CLK and then synchronized to flip-flop two at the next falling edge of CLK, after which time the READY output will go active (HIGH). Negative-going asynchronous READY inputs will be synchronized directly to flip-flop two at the falling edge of CLK, after which time the READY output will go inactive. This mode of operation is intended for use by asynchronous (normally not ready) devices in the system which cannot be guaranteed by design to meet the required RDY setup timing, T_{R1VCL}, on each bus cycle.

When $\overline{\text{ASYNC}}$ is HIGH, the first READY flip-flop is bypassed in the READY synchronization logic. READY inputs are synchronized by flip-flop two on the falling edge of CLK before they are presented to the processor. This mode is available for synchronous devices that can be guaranteed to meet the required RDY setup time.

$\overline{\text{ASYNC}}$ can be changed on every bus cycle to select the appropriate mode of synchronization for each device in the system.

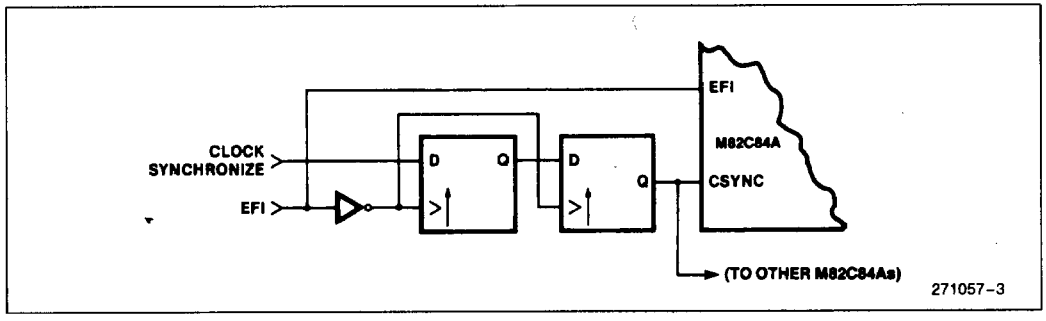

Figure 3. CSYNC Synchronization

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage ..... −0.5V to 7.0V
Input Voltage Applied ..... −0.5V to V_{CC} +0.5V
Output Voltage Applied ..... −0.5V to V_{CC} +0.5V
Storage Temperature ..... −65°C to +150°C
Case Temp. Under Bias ..... −55°C to +125°C
Power Dissipation ..... 1.0 Watt

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

Operating Conditions

Symbol	Parameter	Min	Max	Units
T_C	Case Temperature (Instant On)	−55	125	°C
V_{CC}	Digital Supply Voltage	4.50	5.50	V

D.C. CHARACTERISTICS (Over Specified Operating Conditions)

Symbol	Parameter		Min	Max	Units	Comments
I_{CC}	Operating Supply Current M82C84A			40	mA	25 MHz xtal, C_L = 0
I_{CCS}	Stand By Supply Current (Note 1)			100	μA	
I_{LI}	Input Leakage Current (Note 2)	$\overline{ASYNC}$ Only		10	μA	$\overline{ASYNC}$ = V_{CC}
				−130	μA	$\overline{ASYNC}$ = GND
		All Other Pins		±1.0	μA	0V ≤ V_{IN} ≤ V_{CC}
V_{IL}	Input LOW Voltage			0.8	V	
V_{IH}	Input HIGH Voltage		2.2	V_{CC} + 0.5	V	
V_{IHR}	Reset Input HIGH Voltage		V_{CC} − 0.8V		V	
V_{OL}	Output LOW Voltage			0.4	V	CLK: I_{OL} = 4 mA Others: I_{OL} = 2.5 mA
V_{OH}	Output HIGH Voltage		V_{CC} − 0.4		V V	CLK: I_{OH} = −4 mA Others: I_{OH} = −2.5 mA
V_{IHR}-V_{ILR}	$\overline{RES}$ Input Hysteresis		0.100		V	
C_{IN}	Input Capacitance		4	10	pF	freq = 1 MHz

NOTES:
1. V_{IH}, F/$\overline{C}$, X1 ≥ V_{CC} − 0.2V; EFI = V_{CC} or GND; V_{IL} ≤ 0.2V; ASYNC = V_{CC} or ASYNC = OPEN; X2 = OPEN.
2. An internal pull-up resistor is implemented on the $\overline{ASYNC}$ input.

A.C. CHARACTERISTICS (Over Specified Operating Conditions)

TIMING REQUIREMENTS

Symbol	Parameter	M82C84A		Units	Comments
		Min	Max		
t_{EHEL}	External Frequency HIGH Time	13		ns	90%–90% V_{IN}
t_{ELEH}	External Frequency LOW Time	13		ns	10%–10% V_{IN}
t_{ELEL}	EFI Period	36			(Note 1)
	XTAL Frequency	2.4	25	MHz	
t_{R1VCL}	RDY1, RDY2 Active Setup to CLK	35		ns	$\overline{ASYNC}$ = HIGH
t_{R1VCH}	RDY1, RDY2 Active Setup to CLK	35		ns	$\overline{ASYNC}$ = LOW
t_{R1VCL}	RDY1, RDY2 Inactive Setup to CLK	35		ns	
t_{CLR1X}	RDY1, RDY2 Hold to CLK	0		ns	
t_{AYVCL}	$\overline{ASYNC}$ Setup to CLK	50		ns	
t_{CLAYX}	$\overline{ASYNC}$ Hold to CLK	0		ns	
t_{A1VR1V}	$\overline{AEN1}$, $\overline{AEN2}$ Setup to RDY1, RDY2	15		ns	
t_{CLA1X}	$\overline{AEN1}$, $\overline{AEN2}$ Hold to CLK	0		ns	
t_{YHEH}	CSYNC Setup to EFI	20		ns	
t_{EHYL}	CSYNC Hold to EFI	20		ns	
t_{YHYL}	CSYNC Width	2 • t_{ELEL}		ns	
t_{I1HCL}	$\overline{RES}$ Setup to CLK	65		ns	(Note 2)
t_{CLI1H}	$\overline{RES}$ Hold to CLK	20		ns	(Note 2)

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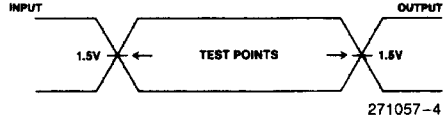
A.C. CHARACTERISTICS (Continued)

TIMING RESPONSES

Symbol	Parameter	Min M82C84A	Max	Units	Comments
t_{CLCL}	CLK Cycle Period	125		ns	
t_{CHCL}	CLK HIGH Time	$(1/3\ t_{CLCL})+2$		ns	
t_{CLCH}	CLK LOW Time	$(2/3\ t_{CLCL})-15$		ns	
t_{CH1CH2} t_{CL2CL1}	CLK Rise or Fall Time		10	ns	1.0V to 3.5V
t_{PHPL}	PCLK HIGH Time	$t_{CLCL}-20$		ns	
t_{PLPH}	PCLK LOW Time	$t_{CLCL}-20$		ns	
t_{RYLCL}	Ready Inactive to CLK (Note 4)	-5		ns	
t_{RYHCH}	Ready Active to CLK (Note 3)	$(2/3\ t_{CLCL})-15$		ns	
t_{CLIL}	CLK to Reset Delay		40	ns	
t_{CLPH}	CLK to PCLK HIGH DELAY		22	ns	
t_{CLPL}	CLK to PCLK LOW Delay		22	ns	
t_{OLCH}	OSC to CLK HIGH Delay	-5	22	ns	
t_{OLCL}	OSC to CLK LOW Delay	2	35	ns	

NOTES:
1. Transition between V_{IL}(max) − 0.4V and V_{IH}(min) + 0.4V.
2. Setup and hold necessary only to guarantee recognition at next clock.
3. Applies only to T3 and TW states.
4. Applies only to T2 states.

A.C. TESTING INPUT, OUTPUT WAVEFORM



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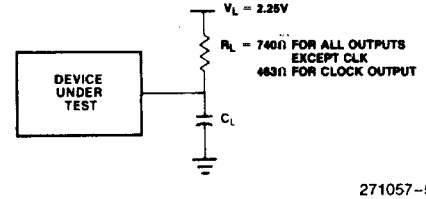
A.C. TESTING: ALL INPUT SIGNALS MUST SWITCH BETWEEN 0.45V AND 2.4V. T_{RISE} AND T_{FALL} MUST BE ≤ 15 ns.
ALL TIMING MEASUREMENTS ARE MADE AT 1.5V.

A.C. TESTING LOAD CIRCUIT



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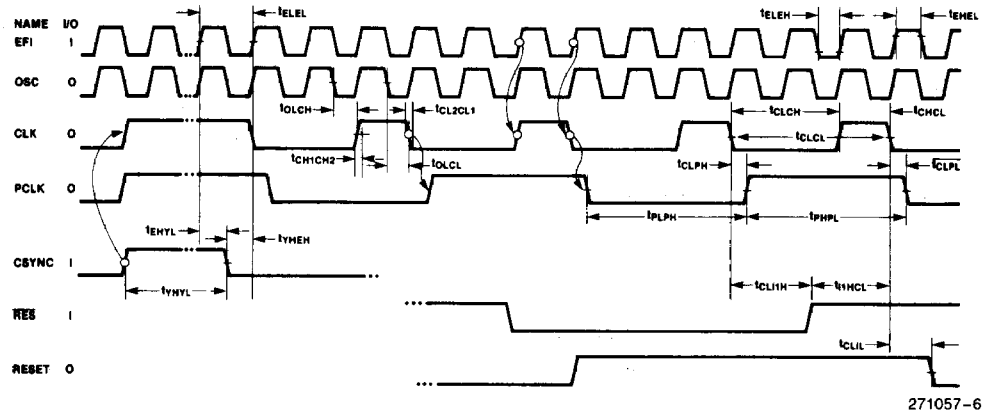
C_L = 100 pF FOR CLK
C_L = 30 pF FOR READY
C_L INCLUDES PROBE AND JIG CAPACITANCE
ALL OTHER OUTPUTS = 30 pF

WAVEFORMS

CLOCKS AND RESET SIGNALS



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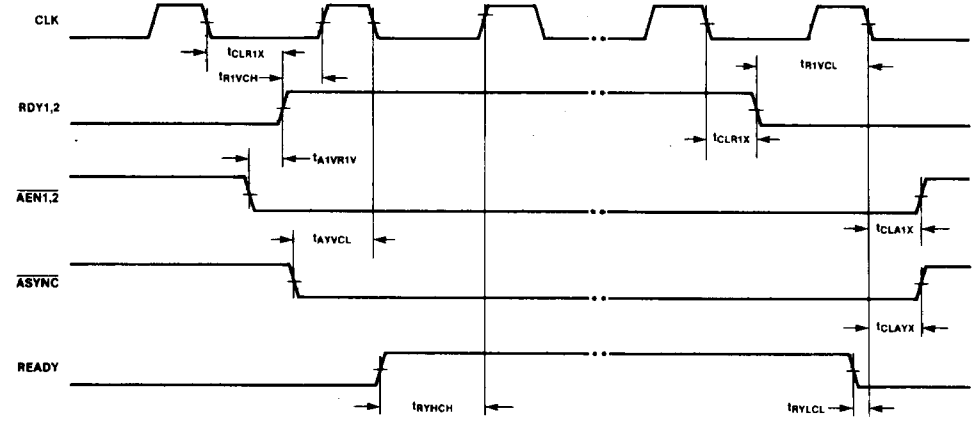
NOTE:
ALL TIMING MEASUREMENTS ARE MADE AT 1.5V, UNLESS OTHERWISE NOTED.

READY SIGNALS (FOR ASYNCHRONOUS DEVICES)



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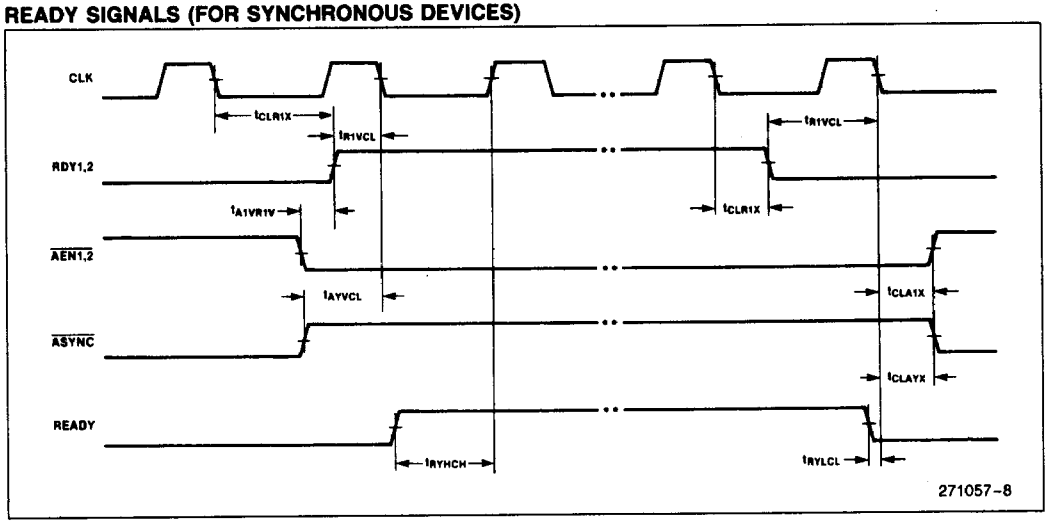
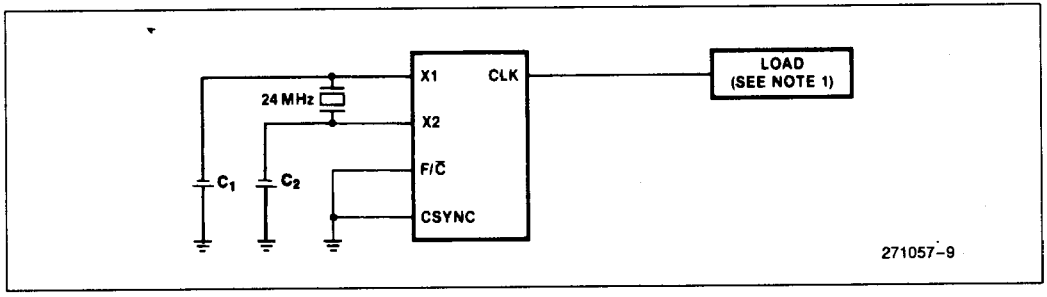
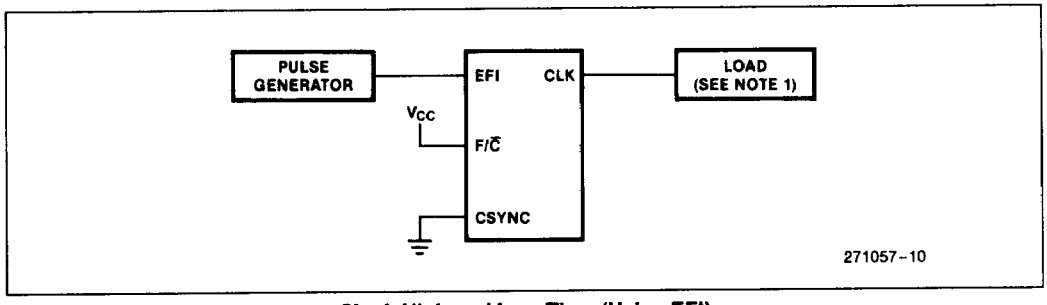
WAVEFORMS (Continued)

READY SIGNALS (FOR SYNCHRONOUS DEVICES)

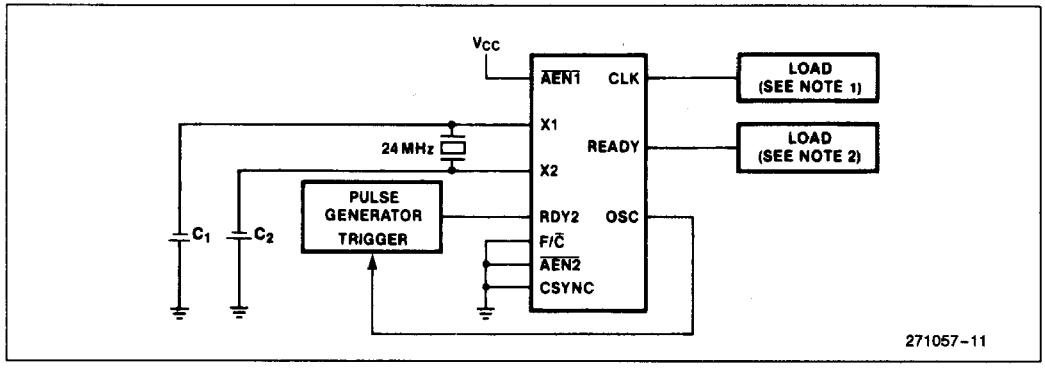




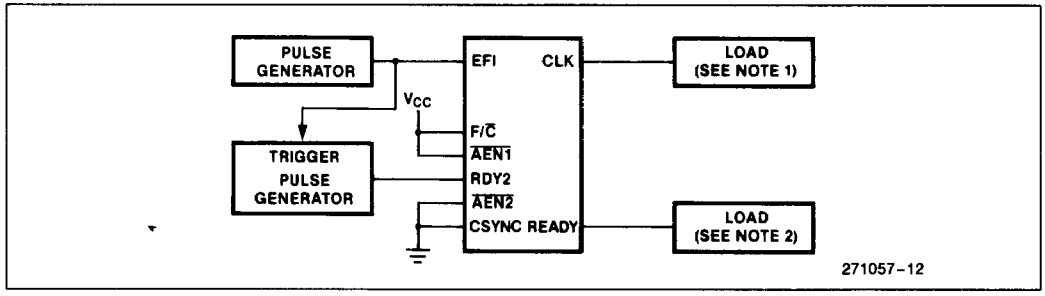
Clock High and Low Time (Using X1, X2)



Clock High and Low Time (Using EFI)



Ready to Clock (Using X1, X2)



Ready to Clock (Using EFI)

NOTES:
1. C_L = 100 pF
2. C_L = 30 pF