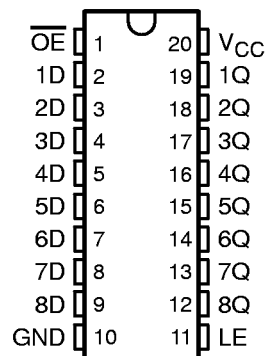


SN54LVTH573, SN74LVTH573 3.3-V ABT OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

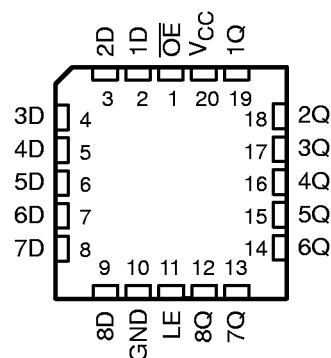
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- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low Static-Power Dissipation
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Support Unregulated Battery Operation Down to 2.7 V
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- I_{off} and Power-Up 3-State Support Hot Insertion
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Latch-Up Performance Exceeds 500 mA Per JESD 17
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model ($C = 200$ pF, $R = 0$)
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK), Ceramic Flat (W) Package, and Ceramic (J) DIPs

SN54LVTH573 . . . J OR W PACKAGE
SN74LVTH573 . . . DB, DW, OR PW PACKAGE
(TOP VIEW)



SN54LVTH573 . . . FK PACKAGE
(TOP VIEW)



description

These octal latches are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

The eight latches of the 'LVTH573 devices are transparent D-type latches. While the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the logic levels set up at the D inputs.

A buffered output-enable (\overline{OE}) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

\overline{OE} does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

When V_{CC} is between 0 and 1.5 V, the devices are in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

SN54LVTH573, SN74LVTH573

3.3-V ABT OCTAL TRANSPARENT D-TYPE LATCHES

WITH 3-STATE OUTPUTS

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description (continued)

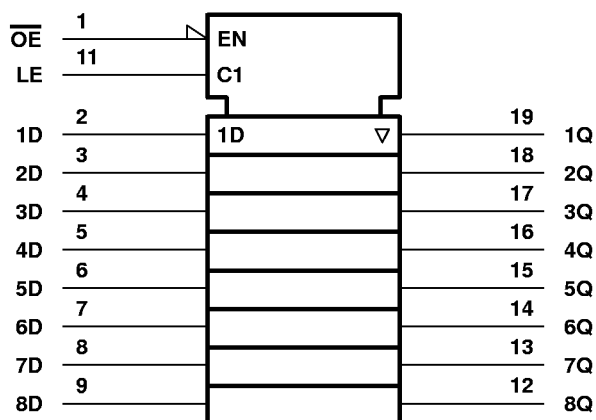
These devices are fully specified for hot-insertion applications using I_{off} and power-up 3-state. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

The SN54LVTH573 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LVTH573 is characterized for operation from -40°C to 85°C .

FUNCTION TABLE
(each latch)

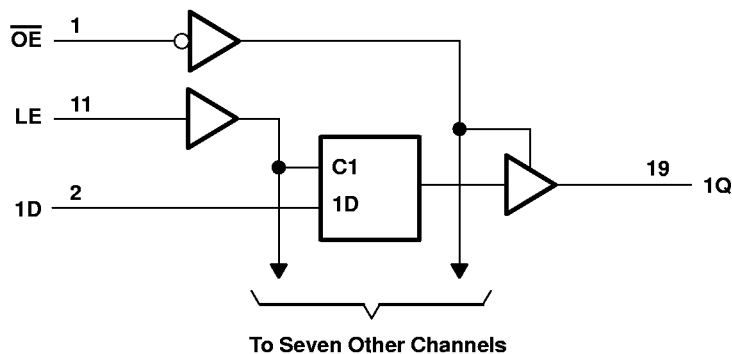
INPUTS			OUTPUT
$\overline{\text{OE}}$	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



SN54LVTH573, SN74LVTH573
3.3-V ABT OCTAL TRANSPARENT D-TYPE LATCHES
WITH 3-STATE OUTPUTS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	–0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high state, V_O (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Current into any output in the low state, I_O : SN54LVTH573	96 mA
SN74LVTH573	128 mA
Current into any output in the high state, I_O (see Note 2): SN54LVTH573	48 mA
SN74LVTH573	64 mA
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Package thermal impedance, θ_{JA} (see Note 3): DB package	115°C/W
DW package	97°C/W
PW package	128°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

		SN54LVTH573		SN74LVTH573		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage		5.5		5.5	V
I_{OH}	High-level output current		–24		–32	mA
I_{OL}	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled			10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate	200		200		μs/V
T_A	Operating free-air temperature	–55	125	–40	85	°C

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



SN54LVTH573, SN74LVTH573
3.3-V ABT OCTAL TRANSPARENT D-TYPE LATCHES
WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54LVTH573			SN74LVTH573			UNIT	
			MIN	TYP†	MAX	MIN	TYP†	MAX		
V_{IK}	$V_{CC} = 2.7\text{ V}$, $I_I = -18\text{ mA}$		-1.2			-1.2			V	
V_{OH}	$V_{CC} = 2.7\text{ V to }3.6\text{ V}$, $I_{OH} = -100\text{ }\mu\text{A}$		$V_{CC}-0.2$			$V_{CC}-0.2$			V	
	$V_{CC} = 2.7\text{ V}$, $I_{OH} = -8\text{ mA}$		2.4			2.4				
	$V_{CC} = 3\text{ V}$	$I_{OH} = -24\text{ mA}$	2			2				
$I_{OH} = -32\text{ mA}$										
V_{OL}	$V_{CC} = 2.7\text{ V}$	$I_{OL} = 100\text{ }\mu\text{A}$				0.2			V	
		$I_{OL} = 24\text{ mA}$				0.5				
	$V_{CC} = 3\text{ V}$	$I_{OL} = 16\text{ mA}$				0.4				
		$I_{OL} = 32\text{ mA}$				0.5				
		$I_{OL} = 48\text{ mA}$				0.55				
		$I_{OL} = 64\text{ mA}$				0.55				
I_I		$V_{CC} = 0\text{ or }3.6\text{ V}$, $V_I = 5.5\text{ V}$	10			10			μA	
	Control inputs	$V_{CC} = 3.6\text{ V}$, $V_I = V_{CC}\text{ or GND}$	± 1			± 1				
	Data inputs	$V_{CC} = 3.6\text{ V}$	$V_I = V_{CC}$	1			1			
$V_I = 0$			-5			-5				
I_{off}		$V_{CC} = 0$, $V_I\text{ or }V_O = 0\text{ to }4.5\text{ V}$				± 100			μA	
$I_{I(\text{hold})}$	Data inputs	$V_{CC} = 3\text{ V}$	$V_I = 0.8\text{ V}$	75			75			μA
			$V_I = 2\text{ V}$	-75			-75			
		$V_{CC} = 3.6\text{ V}\ddagger$, $V_I = 0\text{ to }3.6\text{ V}$				± 500				
I_{OZH}		$V_{CC} = 3.6\text{ V}$, $V_O = 3\text{ V}$	5			5			μA	
I_{OZL}		$V_{CC} = 3.6\text{ V}$, $V_O = 0.5\text{ V}$	-5			-5			μA	
I_{OZPU}		$V_{CC} = 0\text{ to }1.5\text{ V}$, $V_O = 0.5\text{ V to }3\text{ V}$, $OE = \text{don't care}$	$\pm 100^*$			± 100			μA	
I_{OZPD}		$V_{CC} = 1.5\text{ V to }0$, $V_O = 0.5\text{ V to }3\text{ V}$, $OE = \text{don't care}$	$\pm 100^*$			± 100			μA	
I_{CC}	$V_{CC} = 3.6\text{ V}$, $I_O = 0$, $V_I = V_{CC}\text{ or GND}$	Outputs high	0.19			0.19			mA	
		Outputs low	5			5				
		Outputs disabled	0.19			0.19				
$\Delta I_{CC}\S$		$V_{CC} = 3\text{ V to }3.6\text{ V}$, One input at $V_{CC} - 0.6\text{ V}$, Other inputs at $V_{CC}\text{ or GND}$	0.2			0.2			mA	
C_i		$V_I = 3\text{ V or }0$	3			3			pF	
C_o		$V_O = 3\text{ V or }0$	7			7			pF	

*On products compliant to MIL-PRF-38535, this parameter is not production tested.

† All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.



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timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

	SN54LVTH573				SN74LVTH573				UNIT
	V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _w	Pulse duration, LE high				3	3	3	3	ns
t _{su}	Setup time, data before LE↓				0.7	0.6	0.7	0.6	ns
t _h	Hold time, data after LE↓				1.5	1.7	1.5	1.7	ns

switching characteristics over recommended free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVTH573				SN74LVTH573				UNIT	
			V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V			
			MIN	MAX	MIN	MAX	MIN	TYP†	MAX	MIN		MAX
t _{PLH}	D	Q	1.4	4.1	4.7		1.5	2.6	3.9	4.5		ns
t _{PHL}			1.4	4.5	4.8		1.5	2.9	3.9	4.5		
t _{PLH}	LE	Q	1	4.4	5.4		1.9	2.9	4.2	4.9		ns
t _{PHL}			1.4	4.4	5.1		1.9	2.9	4.2	4.9		
t _{PZH}	\overline{OE}	Q	1.4	5.2	6.2		1.5	3.2	5.1	5.9		ns
t _{PZL}			1.4	5.2	6.2		1.5	3.9	5.1	5.9		
t _{PHZ}	\overline{OE}	Q	1.2	5.4	5.7		2	3.5	4.9	5.5		ns
t _{PLZ}			1	5.2	5.2		2	3.2	4.6	4.9		

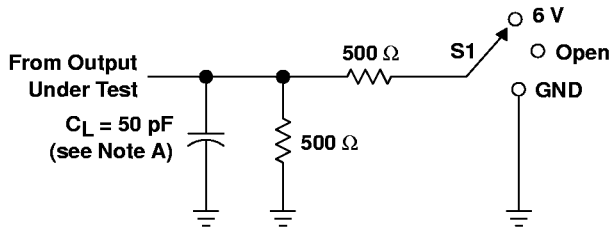
† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.



SN54LVTH573, SN74LVTH573
3.3-V ABT OCTAL TRANSPARENT D-TYPE LATCHES
WITH 3-STATE OUTPUTS

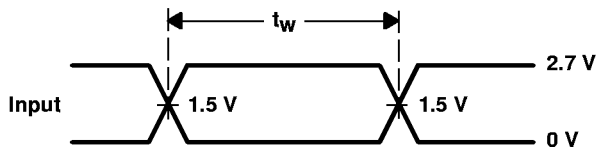
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PARAMETER MEASUREMENT INFORMATION

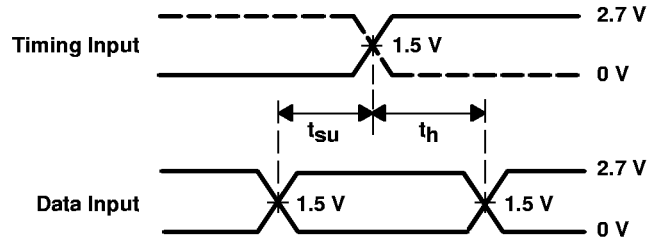


LOAD CIRCUIT

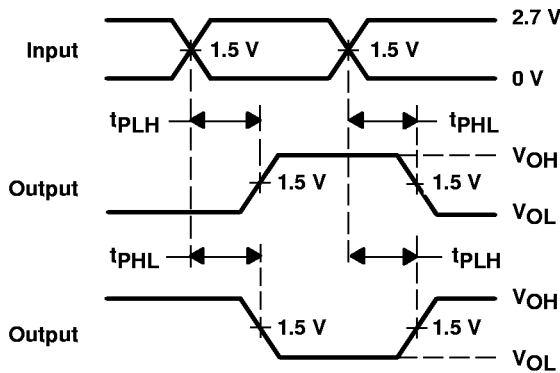
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



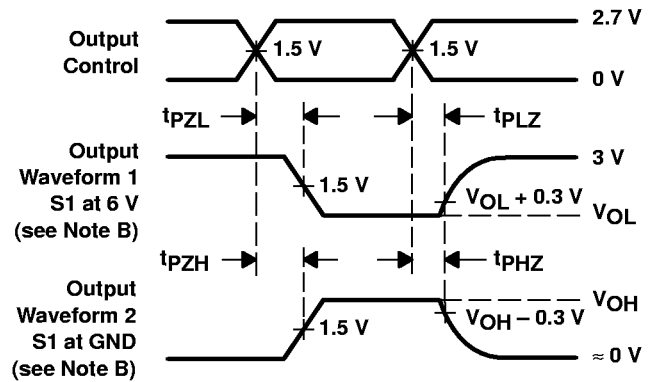
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: PRR $\leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms