

# SN54LS540, SN54LS541, SN74LS540, SN74LS541 OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

D2546, AUGUST 1979—REVISED MARCH 1988

- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- P-N-P Inputs Reduce D-C Loading
- Hysteresis at Inputs Improves Noise Margins
- Data Flow-thru Pinout (All Inputs on Opposite Side from Outputs)

## description

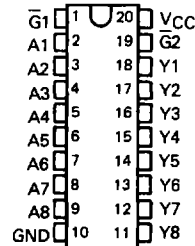
These octal buffers and line drivers are designed to have the performance of the popular SN54LS240/SN74LS240 series and, at the same time, offer a pinout having the inputs and outputs on opposite sides of the package. This arrangement greatly enhances printed circuit board layout.

The three-state control gate is a 2-input NOR such that if either  $\overline{G1}$  or  $\overline{G2}$  are high, all eight outputs are in the high-impedance state.

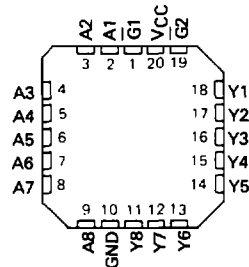
The 'LS540 offers inverting data and the 'LS541 offers true data at the outputs.

The SN54LS540 and SN54LS541 are characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74LS540 and SN74LS541 are characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

SN54LS540, SN54LS541 . . . J OR W PACKAGE  
SN74LS540, SN74LS541 . . . DW OR N PACKAGE  
(TOP VIEW)

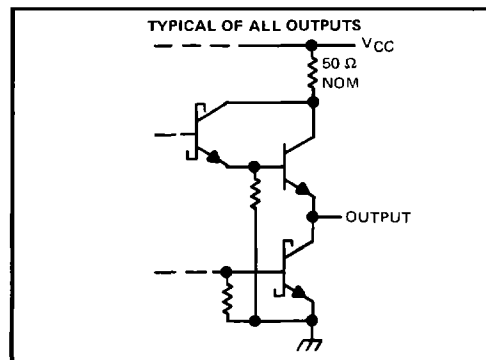
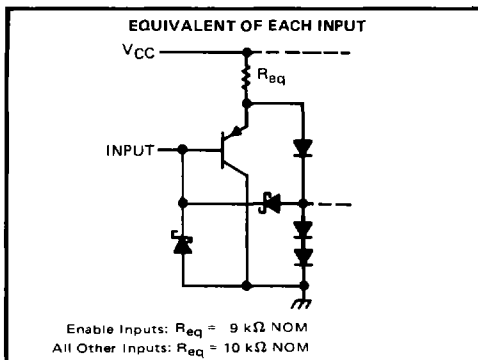


SN54LS540, SN54LS541 . . . FK PACKAGE  
(TOP VIEW)



TYPE	RATED		TYPICAL POWER	
	$I_{OL}$ (SINK CURRENT)	$I_{OH}$ (SOURCE CURRENT)	DISSIPATION (ENABLED)	
			'LS540	'LS541
SN54LS'	12 mA	-12 mA	92.5 mW	120 mW
SN74LS'	24 mA	-15 mA	92.5 mW	120 mW

## schematics of inputs and outputs



PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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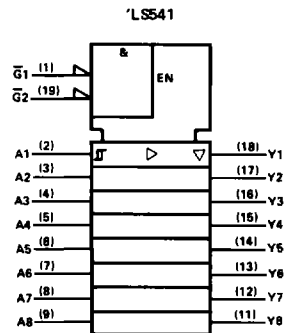
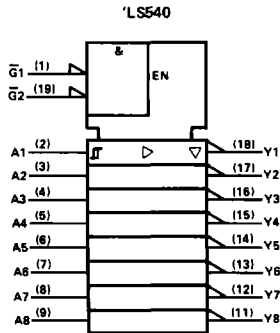
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# SN54LS540, SN54LS541, SN74LS540, SN74LS541

## OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

logic symbols†

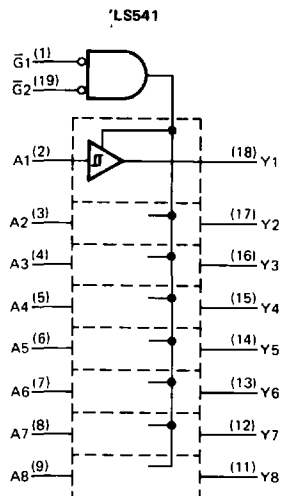
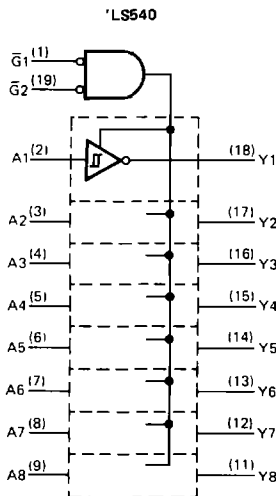


† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, $V_{CC}$ (see Note 1)	7 V
Input voltage	7 V
Operating free-air temperature range: SN54LS540, SN54LS541	-55°C to 125°C
SN74LS540, SN74LS541	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to the network ground terminal.

# SN54LS540, SN54LS541, SN74LS540, SN74LS541 OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

## recommended operating conditions

PARAMETER	SN54LS'			SN74LS'			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, $V_{CC}$ (see Note 1)	4.5	5	5.5	4.75	5	5.25	V
High-level output current, $I_{OH}$			-12			-15	mA
Low-level output current, $I_{OL}$			12			24	mA
Operating free-air temperature, $T_A$	-55		125	0		70	°C

NOTE 1: Voltage values are with respect to network ground terminal.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54LS'			SN74LS'			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
$V_{IH}$ High-level input voltage		2			2			V
$V_{IL}$ Low-level input voltage				0.6			0.6	V
$V_{IK}$ Input clamp voltage	$V_{CC} = \text{MIN}$ , $I_I = -18 \text{ mA}$			-1.5			-1.5	V
Hysteresis ( $V_{T+} - V_{T-}$ )	$V_{CC} = \text{MIN}$	0.2	0.4		0.2	0.4		V
$V_{OH}$ High-level output voltage	$V_{CC} = \text{MIN}$ , $V_{IH} = 2 \text{ V}$ , $V_{IL} = V_{IL \text{ max}}$ , $I_{OH} = -3 \text{ mA}$	2.4	3.4		2.4	3.4		V
	$V_{CC} = \text{MIN}$ , $V_{IH} = 2 \text{ V}$ , $V_{IL} = 0.5 \text{ V}$ , $I_{OH} = \text{MAX}$	2			2			
$V_{OL}$ Low-level output voltage	$V_{CC} = \text{MIN}$ , $V_{IH} = 2 \text{ V}$ , $V_{IL} = V_{IL \text{ max}}$ , $I_{OL} = 12 \text{ mA}$		0.25	0.4		0.25	0.4	V
	$V_{CC} = \text{MIN}$ , $V_{IH} = 2 \text{ V}$ , $V_{IL} = V_{IL \text{ max}}$ , $I_{OL} = 24 \text{ mA}$					0.35	0.5	
$I_{OZH}$ Off-state output current, high-level voltage applied	$V_{CC} = \text{MAX}$ , $V_{IH} = 2 \text{ V}$ , $V_O = 2.7 \text{ V}$			20			20	$\mu\text{A}$
$I_{OZL}$ Off-state output current, low-level voltage applied	$V_{CC} = \text{MAX}$ , $V_{IL} = V_{IL \text{ max}}$ , $V_O = 0.4 \text{ V}$			-20			-20	
$I_I$ Input current at maximum input voltage	$V_{CC} = \text{MAX}$ , $V_I = 7 \text{ V}$			0.1			0.1	mA
$I_{IH}$ High-level input current, any input	$V_{CC} = \text{MAX}$ , $V_I = 2.7 \text{ V}$			20			20	$\mu\text{A}$
$I_{IL}$ Low-level input current	$V_{CC} = \text{MAX}$ , $V_I = 0.4 \text{ V}$			-0.2			-0.2	mA
$I_{OS}$ Short-circuit output current‡	$V_{CC} = \text{MAX}$	-40		-225	-40		-225	mA
$I_{CC}$ Supply current	Outputs high	$V_{CC} = \text{MAX}$ , Outputs open	'LS540	13	25	13	25	mA
			'LS541	18	32	18	32	
	Outputs low		'LS540	24	45	24	45	
			'LS541	30	52	30	52	
	All outputs disabled		'LS540	30	52	30	52	
		'LS541	32	55	32	55		

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions

‡All typical values are at  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

§Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

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**SN54LS540, SN54LS541, SN74LS540, SN74LS541**  
**OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS**

switching characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	'LS540			'LS541			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
$t_{PLH}$ Propagation delay time, low-to-high-level output	$C_L = 45\text{ pF}$ , $R_L = 667\ \Omega$ , See Note 2	9	15		9	15	ns	
$t_{PHL}$ Propagation delay time, high-to-low-level output		9	15		10	18	ns	
$t_{PZL}$ Output enable time to low level		25	38		25	38	ns	
$t_{PZH}$ Output enable time to high level		15	25		20	32	ns	
$t_{PLZ}$ Output disable time from low level	$C_L = 5\text{ pF}$ , $R_L = 667\ \Omega$ , See Note 2	10	18		10	18	ns	
$t_{PHZ}$ Output disable time from high level		15	25		18	29	ns	

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

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