

74LS373, 74LS374, S373, S374

Latches/Flip-Flops

'373 Octal Transparent Latch With 3-State Outputs

'374 Octal D Flip-Flop With 3-State Outputs

Product Specification

Logic Products

FEATURES

- 8-bit transparent latch — '373
- 8-bit positive, edge-triggered register — '374
- 3-State output buffers
- Common 3-State Output Enable
- Independent register and 3-State buffer operation

DESCRIPTION

The '373 is an octal transparent latch coupled to eight 3-State output buffers. The two sections of the device are controlled independently by Latch Enable (E) and Output Enable (\overline{OE}) control gates.

| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT (TOTAL) |
|---------|---------------------------|--------------------------------|
| 74LS373 | 19ns | 24mA |
| 74S373 | 10ns | 105mA |
| 74LS374 | 19ns | 27mA |
| 74S374 | 8ns | 116mA |

ORDERING CODE

| PACKAGES | COMMERCIAL RANGE |
|----------------|--|
| | $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$ |
| Plastic DIP | N74LS373N, N74S373N, N74LS374N, N74S374N |
| Plastic SOL-20 | N74LS373D, N74S373D, N74LS374D, N74S374D |

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

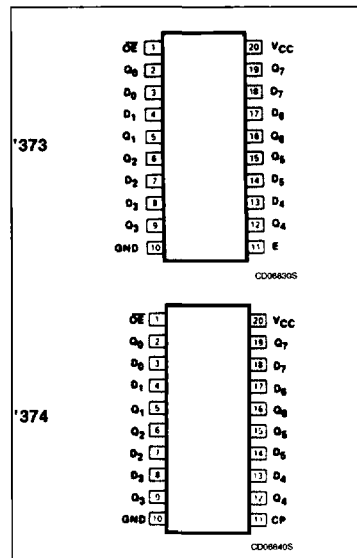
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

| PINS | DESCRIPTION | 74S | 74LS |
|------|-------------|-------|--------|
| All | Inputs | 1Sul | 1LSul |
| All | Outputs | 10Sul | 30LSul |

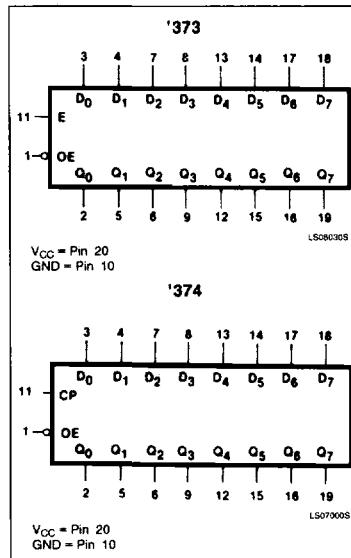
NOTE:

Where a 74S unit load (Sul) is $50\mu A$ I_{IH} and $-2.0mA$ I_{IL} , and a 74LS unit load (LSul) is $20\mu A$ I_{IH} and $-0.4mA$ I_{IL} .

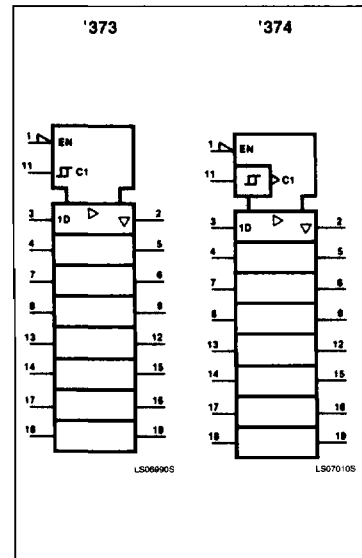
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/EC)



Latches/Flip-Flops

74LS373, 74LS374, S373, S374

The data on the D inputs are transferred to the latch outputs when the Latch Enable (E) input is HIGH. The latch remains transparent to the data inputs while E is HIGH, and stores the data present one set-up time before the HIGH-to-LOW enable transition. The enable gate has hysteresis built in to help minimize problems that signal and ground noise can cause on the latching operation.

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active LOW Output Enable (\overline{OE}) controls all eight 3-State buffers independent of the latch

operation. When \overline{OE} is LOW, the latched or transparent data appears at the outputs. When \overline{OE} is HIGH, the outputs are in the HIGH impedance "off" state, which means they will neither drive nor load the bus.

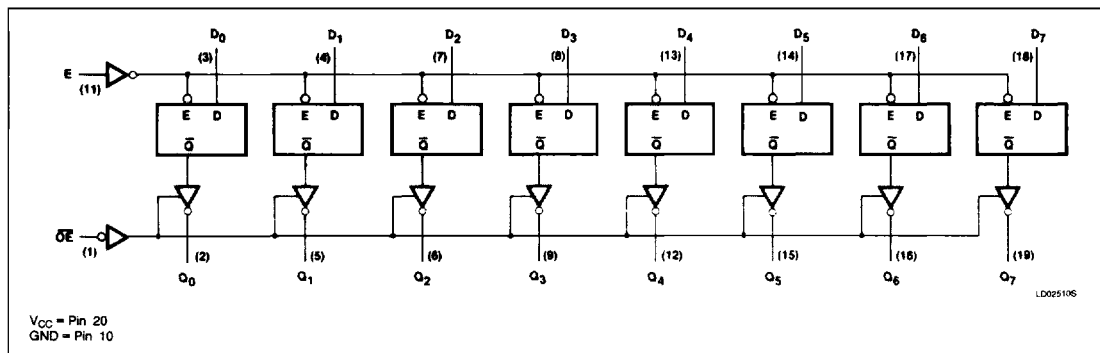
The '374 is an 8-bit, edge-triggered register coupled to eight 3-State output buffers. The two sections of the device are controlled independently by the Clock (CP) and Output Enable (\overline{OE}) control gates.

The register is fully edge triggered. The state of each D input, one set-up time before the LOW-to-HIGH clock transition, is transferred

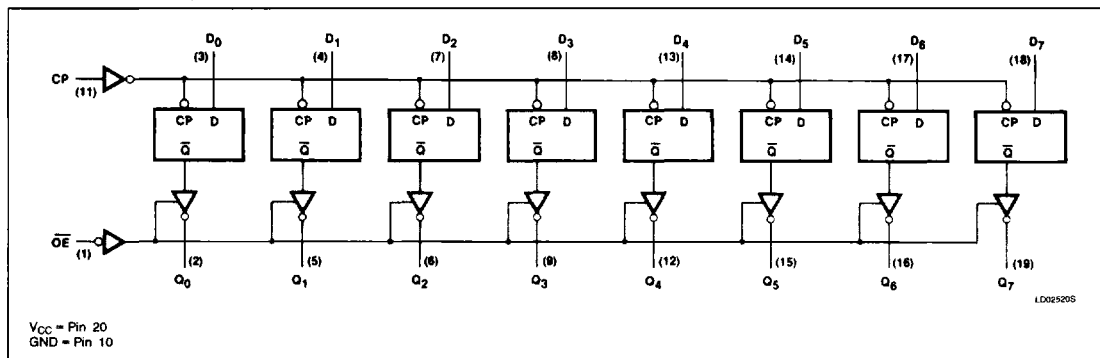
to the corresponding flip-flop's Q output. The clock buffer has hysteresis built in to help minimize problems that signal and ground noise can cause on the clocking operation.

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active LOW Output Enable (\overline{OE}) controls all eight 3-State buffers independent of the register operation. When \overline{OE} is LOW, the data in the register appears at the outputs. When \overline{OE} is HIGH, the outputs are in the HIGH impedance "off" state, which means they will neither drive nor load the bus.

LOGIC DIAGRAM, '373



LOGIC DIAGRAM, '374



MODE SELECT — FUNCTION TABLE '373

| OPERATING MODES | INPUTS | | | INTERNAL REGISTER | OUTPUTS |
|------------------------------------|-----------------|---|-------|-------------------|-------------|
| | \overline{OE} | E | D_n | | $Q_0 - Q_7$ |
| Enable and read register | L | H | L | L | L |
| | L | H | H | H | H |
| Latch and read register | L | L | l | L | L |
| | L | L | h | H | H |
| Latch register and disable outputs | H | L | l | L | (Z) |
| | H | L | h | H | (Z) |

Latches/Flip-Flops

74LS373, 74LS374, S373, S374

MODE SELECT — FUNCTION TABLE '374

| OPERATING MODES | INPUTS | | | INTERNAL REGISTER | OUTPUTS |
|-----------------------------------|-----------------|--------|--------|-------------------|-------------|
| | \overline{OE} | CP | D_n | | $Q_0 - Q_7$ |
| Load and read register | L L | ↑ ↑ | l h | L H | L H |
| Load register and disable outputs | H H | ↑ ↑ | l h | L H | (Z) (Z) |

H = HIGH voltage level
 h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition or HIGH-to-LOW \overline{OE} transition
 L = LOW voltage level
 l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition or HIGH-to-LOW \overline{OE} transition
 (Z) = HIGH impedance "off" state
 ↑ = LOW-to-HIGH clock transition

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

| PARAMETER | | 74LS | 74S | UNIT |
|-----------|--|--------------------|--------------------|------|
| V_{CC} | Supply voltage | 7.0 | 7.0 | V |
| V_{IN} | Input voltage | -0.5 to +7.0 | -0.5 to +5.5 | V |
| I_{IN} | Input current | -30 to +1 | -30 to +5 | mA |
| V_{OUT} | Voltage applied to output in HIGH output state | -0.5 to + V_{CC} | -0.5 to + V_{CC} | V |
| T_A | Operating free-air temperature range | 0 to 70 | | °C |

RECOMMENDED OPERATING CONDITIONS

| PARAMETER | 74LS | | | 74S | | | UNIT | |
|-----------|--------------------------------|------|-----|------|------|-----|------|----|
| | Min | Nom | Max | Min | Nom | Max | | |
| V_{CC} | Supply voltage | 4.75 | 5.0 | 5.25 | 4.75 | 5.0 | 5.25 | V |
| V_{IH} | HIGH-level input voltage | 2.0 | | | 2.0 | | | V |
| V_{IL} | LOW-level input voltage | | | +0.8 | | | +0.8 | V |
| I_{IK} | Input clamp current | | | -18 | | | -18 | mA |
| I_{OH} | HIGH-level output current | | | -2.6 | | | -6.5 | mA |
| I_{OL} | LOW-level output current | | | 24 | | | 20 | mA |
| T_A | Operating free-air temperature | 0 | | 70 | 0 | | 70 | °C |

5

Latches/Flip-Flops

74LS373, 74LS374, S373, S374

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

| PARAMETER | TEST CONDITIONS ¹ | 74LS373, 374 | | | 74S373, 374 | | | UNIT |
|--|--|---|------------------|------|-------------|------------------|-------|------|
| | | Min | Typ ² | Max | Min | Typ ² | Max | |
| V _{OH} HIGH-level output voltage | V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OH} = MAX | 2.4 | 3.1 | | 2.4 | 3.1 | | V |
| V _{OL} LOW-level output voltage | V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX | I _{OL} = MAX | 0.35 | 0.5 | | | 0.5 | V |
| | | I _{OL} = 12mA (74LS) | 0.25 | 0.4 | | | | V |
| V _{IK} Input clamp voltage | V _{CC} = MIN, I _I = I _{IK} | | | -1.5 | | | -1.2 | V |
| I _{OZH} Off-state output current, HIGH-level voltage applied | V _{CC} = MAX, V _{IH} = MIN | V _O = 2.7V | | 20 | | | | μA |
| | | V _O = 2.4V | | | | | 50 | μA |
| I _{OZL} Off-state output current, LOW-level voltage applied | V _{CC} = MAX, V _{IH} = MIN | V _O = 0.4V | | -20 | | | | μA |
| | | V _O = 0.5V | | | | | -50 | μA |
| I _I Input current at maximum input voltage | V _{CC} = MAX | V _I = 7.0V | | 0.1 | | | | mA |
| | | V _I = 5.5V | | | | | 1.0 | mA |
| I _{IH} HIGH-level input current | V _{CC} = MAX, V _I = 2.7V | | | 20 | | | 50 | μA |
| I _{IL} LOW-level input current | V _{CC} = MAX | V _I = 0.4V | | -0.4 | | | | mA |
| | | V _I = 0.5V | | | | | -0.25 | mA |
| I _{OS} Short-circuit output current ³ | V _{CC} = MAX | -30 | | -130 | -40 | | -100 | mA |
| I _{CC} Supply current (total) | V _{CC} = MAX | I _{CCZ} \overline{OE} = 4.5V 'LS373 | 24 | 40 | | | | mA |
| | | I _{CCL} \overline{OE} = 0V 'S373 | | | | 105 | 160 | mA |
| | | I _{CCZ} \overline{OE} = 4.5V 'LS374 | 27 | 40 | | | | mA |
| | | I _{CCL} All inputs grounded 'S374 | | | | 102 | 140 | mA |
| | | I _{CCZ} CP, \overline{OE} = 4.5V D inputs = GND 'S374 | | | | 131 | 180 | mA |

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

| PARAMETER | TEST CONDITIONS | 74LS | | 74S | | UNIT |
|---|----------------------------------|--|----------|--|----------|------|
| | | C _L = 45pF, R _L = 667Ω | | C _L = 15pF, R _L = 280Ω | | |
| | | Min | Max | Min | Max | |
| f _{MAX} Maximum clock frequency | Waveform 6, '374 | 35 | | 75 | | MHz |
| t _{PLH} Propagation delay t _{PHL} Latch enable to output | Waveform 1, '373 | | 30 30 | | 14 18 | ns |
| t _{PLH} Propagation delay t _{PHL} Data to output | Waveform 4, '373 | | 18 18 | | 12 12 | ns |
| t _{PLH} Propagation delay t _{PHL} Clock to output | Waveform 6, '374 | | 28 28 | | 15 17 | ns |
| t _{PZH} Enable time to HIGH level | Waveform 2 | | 28 | | 15 | ns |
| t _{PZL} Enable time to LOW level | Waveform 3, '373 '374 | | 36 28 | | 18 18 | ns |
| t _{PHZ} Disable time from HIGH level | Waveform 2, C _L = 5pF | | 20 | | 9 | ns |
| t _{PLZ} Disable time from LOW level | Waveform 3, C _L = 5pF | | 25 | | 12 | ns |

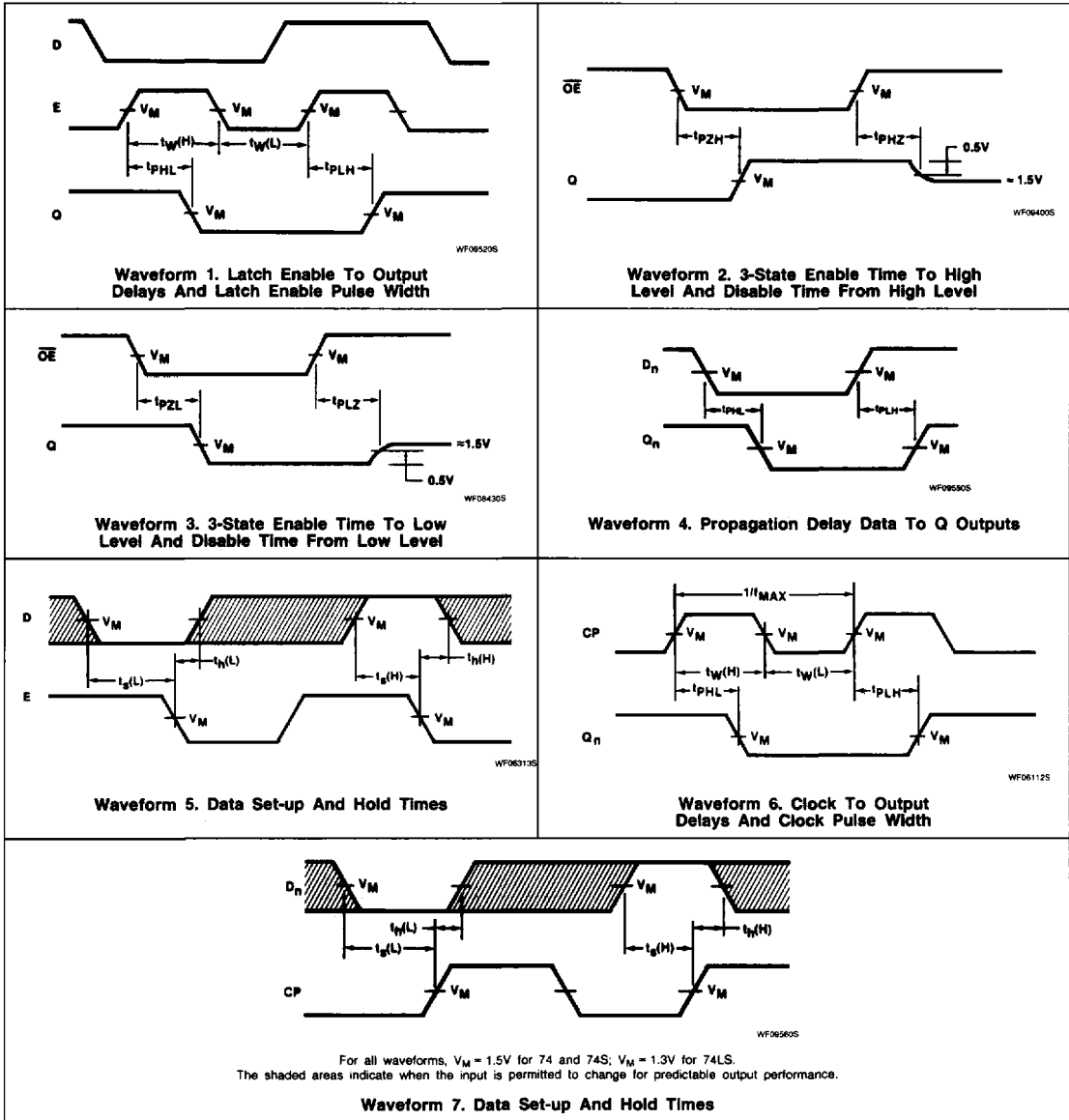
NOTE:

Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

Latches/Flip-Flops

74LS373, 74LS374, S373, S374

AC WAVEFORMS



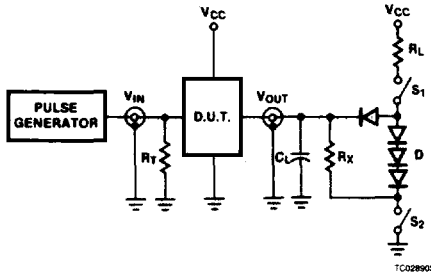
Latches/Flip-Flops

74LS373, 74LS374, S373, S374

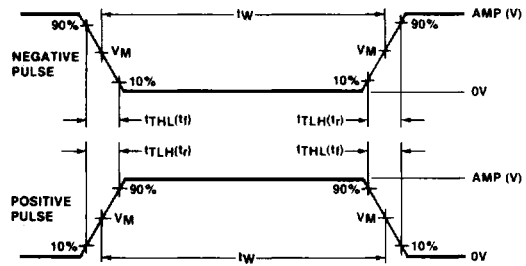
AC SET-UP REQUIREMENTS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

| PARAMETER | TEST CONDITIONS | 74LS | | 74S | | UNIT |
|--------------------------|-----------------------------------|------------------|-----|-----|----------|------|
| | | Min | Max | Min | Max | |
| $t_{W(H)}$ $t_{W(L)}$ | Latch enable pulse width | Waveform 1, '373 | 15 | | 6 7.3 | ns |
| t_s | Set-up time, data to latch enable | Waveform 5, '373 | 5 | | 0 | ns |
| t_h | Hold time, data to latch enable | Waveform 5, '373 | 20 | | 10 | ns |
| $t_{W(H)}$ $t_{W(L)}$ | Clock pulse width | Waveform 6, '374 | 15 | | 6 7.3 | ns |
| t_s | Set-up time, data to clock | Waveform 7, '374 | 20 | | 5 | ns |
| t_h | Hold time, data to clock | Waveform 7, '374 | 0 | | 2 | ns |

TEST CIRCUITS AND WAVEFORMS



Test Circuit For 3-State Outputs



$V_M = 1.3\text{V}$ for 74LS; $V_M = 1.5\text{V}$ for all other TTL families.

Input Pulse Definition

SWITCH POSITION

| TEST | SWITCH 1 | SWITCH 2 |
|-----------|----------|----------|
| t_{PZH} | Open | Closed |
| t_{PZL} | Closed | Open |
| t_{PHZ} | Closed | Closed |
| t_{PLZ} | Closed | Closed |

| FAMILY | INPUT PULSE REQUIREMENTS | | | | |
|--------|--------------------------|-----------|-------------|-----------|-----------|
| | Amplitude | Rep. Rate | Pulse Width | t_{TLH} | t_{THL} |
| 74 | 3.0V | 1MHz | 500ns | 7ns | 7ns |
| 74LS | 3.0V | 1MHz | 500ns | 15ns | 6ns |
| 74S | 3.0V | 1MHz | 500ns | 2.5ns | 2.5ns |

DEFINITIONS

R_L = Load resistor to V_{CC} ; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.

D = Diodes are 1N916, 1N3064, or equivalent.

$R_X = 1\text{k}\Omega$ for 74, 74S, $R_X = 5\text{k}\Omega$ for 74LS.

t_{TLH} , t_{THL} Values should be less than or equal to the table entries.