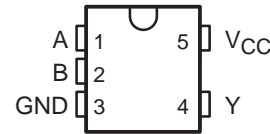


# SN74AHCT1G32 SINGLE 2-INPUT POSITIVE-OR GATE

SCLS320H – MARCH 1996 – REVISED NOVEMBER 1999

- **EPIC™ (Enhanced-Performance Implanted CMOS) Process**
- **Inputs Are TTL-Voltage Compatible**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **Package Options Include Plastic Small-Outline Transistor (DBV, DCK) Packages**

DBV OR DCK PACKAGE  
(TOP VIEW)



## description

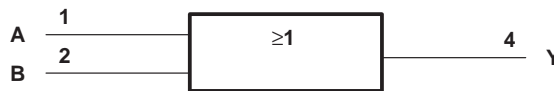
The SN74AHCT1G32 is a single 2-input positive-OR gate. The device performs the Boolean function  $Y = A + B$  or  $Y = \overline{\overline{A} \cdot \overline{B}}$  in positive logic.

The SN74AHCT1G32 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
H	X	H
X	H	H
L	L	L

## logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS  
INSTRUMENTS**

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# SN74AHCT1G32

## SINGLE 2-INPUT POSITIVE-OR GATE

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### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$	.....	-0.5 V to 7 V	
Input voltage range, $V_I$ (see Note 1)	.....	-0.5 V to 7 V	
Output voltage range, $V_O$ (see Note 1)	.....	-0.5 V to $V_{CC} + 0.5$ V	
Input clamp current, $I_{IK}$ ( $V_I < 0$ )	.....	-20 mA	
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ )	.....	$\pm 20$ mA	
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )	.....	$\pm 25$ mA	
Continuous current through $V_{CC}$ or GND	.....	$\pm 50$ mA	
Package thermal impedance, $\theta_{JA}$ (see Note 2): DBV package	.....	347°C/W	
	DCK package	.....	389°C/W
Storage temperature range, $T_{stg}$	.....	-65°C to 150°C	

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
 2. The package thermal impedance is calculated in accordance with JESD 51.

### recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage	4.5	5.5	V
$V_{IH}$	High-level input voltage	2		V
$V_{IL}$	Low-level input voltage		0.8	V
$V_I$	Input voltage	0	5.5	V
$V_O$	Output voltage	0	$V_{CC}$	V
$I_{OH}$	High-level output current		-8	mA
$I_{OL}$	Low-level output current		8	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		20	ns/V
$T_A$	Operating free-air temperature	-40	85	°C

NOTE 3: All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$V_{CC}$	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
			MIN	TYP	MAX			
$V_{OH}$	$I_{OH} = -50 \mu\text{A}$	4.5 V	4.4	4.5		4.4		V
	$I_{OH} = -8 \text{ mA}$					3.8		
$V_{OL}$	$I_{OL} = 50 \mu\text{A}$	4.5 V			0.1		0.1	V
	$I_{OL} = 8 \text{ mA}$				0.36		0.44	
$I_I$	$V_I = V_{CC}$ or GND	5.5 V			$\pm 0.1$		$\pm 1$	$\mu\text{A}$
$I_{CC}$	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			1		10	$\mu\text{A}$
$\Delta I_{CC}^\ddagger$	One input at 3.4 V, Other inputs at $V_{CC}$ or GND	5.5 V			1.35		1.5	mA
$C_i$	$V_I = V_{CC}$ or GND	5 V		2	10		10	pF

‡ This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or  $V_{CC}$ .



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switching characteristics over recommended operating free-air temperature range,  
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
				MIN	TYP	MAX			
$t_{PLH}$	A or B	Y	$C_L = 15\text{ pF}$	5	6.9	1	8	ns	
$t_{PHL}$				5	6.9	1	8		
$t_{PLH}$	A or B	Y	$C_L = 50\text{ pF}$	5.5	7.9	1	9	ns	
$t_{PHL}$				5.5	7.9	1	9		

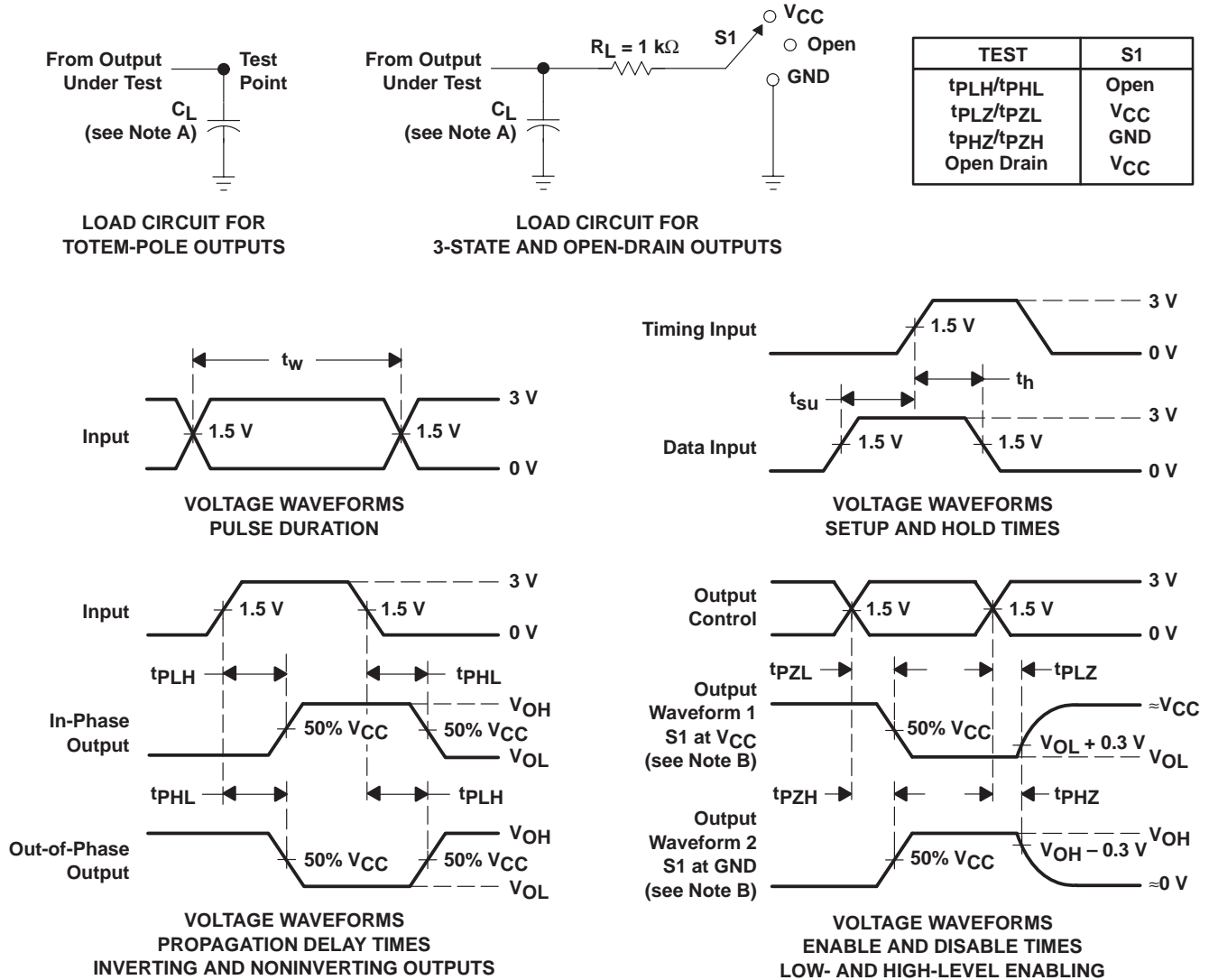
operating characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
$C_{pd}$ Power dissipation capacitance	No load, $f = 1\text{ MHz}$	11.5	pF

# SN74AHCT1G32 SINGLE 2-INPUT POSITIVE-OR GATE

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## PARAMETER MEASUREMENT INFORMATION



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq 1\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 3\text{ ns}$ ,  $t_f \leq 3\text{ ns}$ .  
 D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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