MOTOROLA

Military 54LS243

Octal Bus Transceivers With 3-State Outputs

ELECTRICALLY TESTED PER:
MIL-M-38510/32802

The 54LS243 is a Quad Bus Transmitter/Receiver designed for 4-line asynchronous 2-way data communications between data buses.

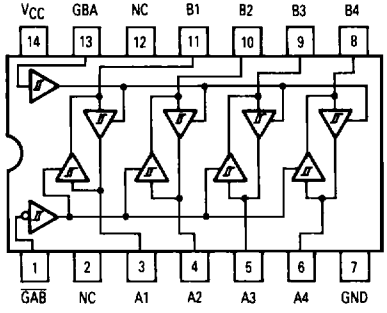
- Hysteresis at Inputs to Improve Noise Margins
- 2-Way Asynchronous Data Bus Communications
- Input Clamp Diodes Limit High-Speed Termination Effects

AVAILABLE AS:

1) JAN: JM38510/32802BXA
2) SMD: 8002002
3) 883C: 54LS243/BXAJC

X = CASE OUTLINE AS FOLLOWS:
PACKAGE: CERDIP: C
CERFLAT: D
LCC: 2
***Call Factory for latest update**

LOGIC DIAGRAM



PIN ASSIGNMENTS

FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION A)
$\overline{GAB}$	1	1	2	V_{CC}
NC	2	2	3	V_{CC}
A1	3	3	4	V_{CC}
A2	4	4	6	V_{CC}
A3	5	5	8	V_{CC}
A4	6	6	9	V_{CC}
GND	7	7	10	GND
B4	8	8	12	V_{CC}
B3	9	9	13	V_{CC}
B2	10	10	14	V_{CC}
B1	11	11	16	V_{CC}
NC	12	12	18	V_{CC}
GBA	13	13	19	V_{CC}
V_{CC}	14	14	20	V_{CC}

BURN-IN CONDITIONS:
V_{CC} = 5.0 V MIN/6.0 V MAX

TRUTH TABLE		
Inputs		**Output**
$\overline{GAB}$	D	
L	L	L
L	H	H
H	X	(Z)

TRUTH TABLE		
Inputs		**Output**
GBA	D	
L	X	(Z)
H	L	L
H	H	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = HIGH Impedance

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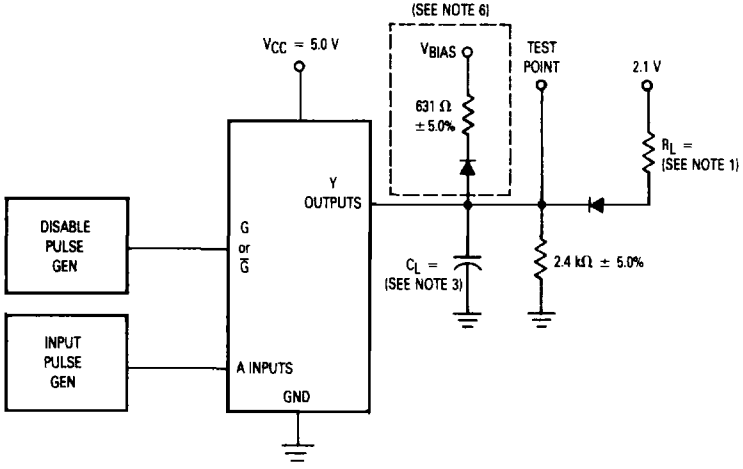
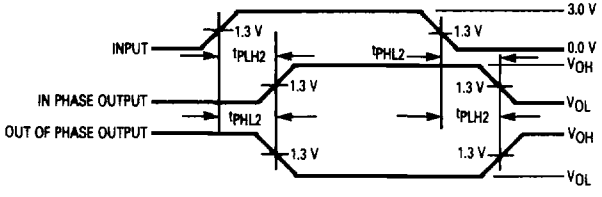
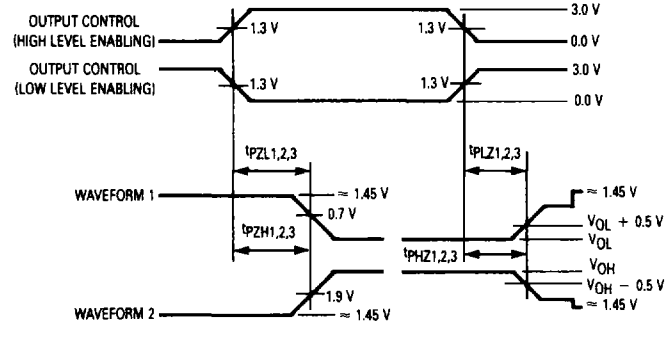
AC TEST CIRCUIT



WAVEFORMS



Voltage Waveforms Propagation Delay Times



Voltage Waveforms Enable and Disable Times, Three-State Outputs

Symbol	Parameter	Limits						Units	Test Condition (Unless Otherwise Specified)
		+25°C		+125°C		−55°C			
	Static Parameters:	Subgroup 1		Subgroup 2		Subgroup 3			
		Min	Max	Min	Max	Min	Max		
V_{OHH}	Logical "1" Output Voltage	2.4		2.4		2.4		V	V_{CC} = 4.5 V, I_{OH} = −3.0 mA, V_{IN} = 2.0 V (all inputs), $\overline{GAB}$/GBA = 0.7 V or 2.0 V per truth table.
V_{OHL}	Logical "1" Output Voltage	2.0		2.0		2.0		V	V_{CC} = 4.5 V, I_{OH} = −12 mA, V_{IN} = 2.0 V (all inputs), $\overline{GAB}$/GBA = 2.0 V or 0.5 V per truth table.
V_{OL}	Logical "0" Output Voltage		0.4		0.4		0.4	V	V_{CC} = 4.5 V, I_{OL} = 12 mA, V_{IN} = 0.7 V (all inputs), $\overline{GAB}$/GBA = 2.0 V or 0.7 V per truth table.
V_{IC}	Input Clamping Voltage		−1.5					V	V_{CC} = 4.5 V, I_{IN} = −18 mA, other inputs are open, $\overline{GAB}$/GBA = GND, open, 5.5 V, 4.5 V per truth table.
I_{IH}	Logical "1" Input Current		20		20		20	μA	V_{CC} = 5.5 V, V_{IH} = 2.7 V, other inputs are open, $\overline{GAB}$/GBA = 5.5 V, 2.7 V or GND per truth table.
I_{IHH}	Logical "1" Input Current		100		100		100	μA	V_{CC} = 5.5 V, V_{IHH} = 5.5 V, other inputs are open, $\overline{GAB}$/GBA = 0 V, 4.5 V, 5.5 V or open per truth table.
I_{IL}	Logical "0" Input Current	0	−150	0	−150	0	−150	μA	V_{CC} = 5.5 V, V_{IN} = 0.4 V, other inputs are open, $\overline{GAB}$/GBA = GND, 0.4 V, 4.5 V, 5.5 V per truth table.
I_{OS}	Output Short Circuit Current	−40	−225	−40	−225	−40	−225	mA	V_{CC} = 5.5 V, V_{IN} = 5.5 V all inputs, V_{OUT} = GND, $\overline{GAB}$/GBA = GND or 5.5 V per truth table.
I_{IOZH}	Output Off Current High		20		20		20	μA	V_{CC} = 5.5 V, V_{IN} = 2.7 V, other inputs are open, $\overline{GAB}$ = 2.0 V or open, GBA = 0.7 V or open.
I_{IOZL}	Output Off Current Low		−200		−200		−200	μA	V_{CC} = 5.5 V, V_{IN} = 0.4 V, other inputs are open, $\overline{GAB}$ = 2.0 V or open, GBA = 0.7 V or open.
I_{CCH}	Power Supply Current		38		38		38	mA	V_{CC} = 5.5 V, V_{IN} = 5.5 V (all inputs), $\overline{GAB}$/GBA = GND.
I_{CCL}	Power Supply Current		50		50		50	mA	V_{CC} = 5.5 V, V_{IN} = GND (all inputs).
I_{CCZ}	Power Supply Current Off		50		50		50	mA	V_{CC} = 5.5 V, all inputs are open, $\overline{GAB}$ = 5.5 V, GBA = GND.
V_{IH}	Logical "1" Input Voltage	2.0		2.0		2.0		V	V_{CC} = 4.5 V.
V_{IL}	Logical "0" Input Voltage		0.7		0.7		0.7	V	V_{CC} = 4.5 V.
		Subgroup 7		Subgroup 8A		Subgroup 8B			
	Functional Tests								per Truth Table with V_{CC} = 5.0 V, V_{INL} = 0.4 V, and V_{INH} = 2.4 V.

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Symbol	Parameter	Limits						Units	Test Condition (Unless Otherwise Specified)
	Switching Parameters	+25°C		+125°C		−55°C			
		Subgroup 9		Subgroup 10		Subgroup 11			
		Min	Max	Min	Max	Min	Max		
t_{PHL2} t_{PHL2}	Propagation Delay /Data-Output Output High-Low	2.0	23 18	2.0	30 25	2.0	30 25	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 110 Ω. V_{CC} = 5.0 V, C_L = 45 pF, R_L = 667 Ω.
t_{PLH2} t_{PLH2}	Propagation Delay /Data-Output Output Low-High	2.0	19 18	2.0	25 23	2.0	25 23	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 110 Ω. V_{CC} = 5.0 V, C_L = 45 pF, R_L = 667 Ω.
t_{PLZ1} t_{PLZ1}	Propagation Delay /Data-Output Output Low-High	2.0	30 25	2.0	39 34	2.0	39 34	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 110 Ω. V_{CC} = 5.0 V, C_L = 45 pF, R_L = 667 Ω.
t_{PHZ1} t_{PHZ1}	Propagation Delay /Data-Output Output High-Low	2.0	35 18	2.0	46 41	2.0	46 41	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 110 Ω. V_{CC} = 5.0 V, C_L = 45 pF, R_L = 667 Ω.
t_{PZL1} t_{PZL1}	Propagation Delay /Data-Output Output Low-High	2.0	35 30	2.0	46 41	2.0	46 41	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 110 Ω. V_{CC} = 5.0 V, C_L = 45 pF, R_L = 667 Ω.
t_{PZH1} t_{PZH1}	Propagation Delay /Data-Output Output High-Low	2.0	28 23	2.0	36 31	2.0	36 31	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 110 Ω. V_{CC} = 5.0 V, C_L = 45 pF, R_L = 667 Ω.

NOTES:
1. R_L = 110 Ω ± 5.0%
2. All diodes are 1N3064 or equivalent.
3. C_L = 50 pF ± 10% including probe and jig capacitance.
4. The pulse generators have the following characteristics:
   V_{gen} = 3.0 V, PRR ≤ 1.0 MHz, t_r ≤ 15 ns, t_f = 6.0 ns, Z_{OUT} = 50 Ω.
5. Clock pulse characteristics: $t_{p(clock)}$ = 20 ns, t_{setup} = 20 ns.
6. The diode and resistor shown within the dotted area are optional. When the diode and resistor are used, V_{BIAS} shall be 5.5 V for all tests except for t_{PHZ}, for t_{PHZ} tests, V_{BIAS} shall be −0.6 V.

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