# SRAM

# 512K x 8 SRAM

## WITH OUTPUT ENABLE

### FEATURES

- High speed: 20, 25, 35 and 55ns
- High-performance, low-power, CMOS double-metal process
- Single +5V ±10% power supply
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ options
- All inputs and outputs are TTL compatible
- Fast Output Enable access time: 8ns

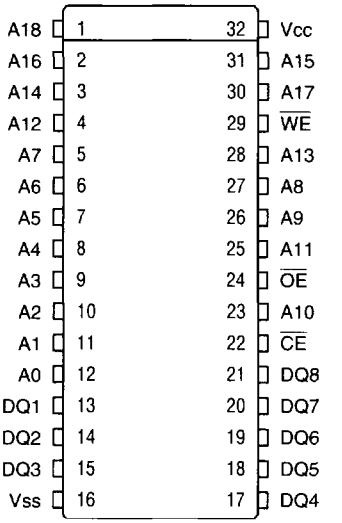
### OPTIONS — MARKING

- Timing
  - 20ns access — -20
  - 25ns access — -25
  - 35ns access — -35
  - 55ns access — -55
- Packages
  - Plastic SOJ (400 mil) — DJ

  Available in ceramic packages tested to meet military specifications. Please refer to Micron's ***Military Data Book.***
- 2V data retention — L
- Temperature
  - Industrial (-40°C to +85°C) — IT
  - Automotive (-40°C to +125°C) — AT
  - Extended (-55°C to +125°C) — XT

### PIN ASSIGNMENT (Top View)

**32-Pin SOJ**
(E-11)




### GENERAL DESCRIPTION

The Micron SRAM family employs high-speed, low-power CMOS designs using a four-transistor memory cell. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

For flexibility in high-speed memory applications, Micron offers chip enable ($\overline{CE}$) capability. This enhancement can place the outputs in High-Z for additional flexibility in system design.

Writing to this device is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH while output enable ($\overline{OE}$) and $\overline{CE}$ go LOW. The device offers a reduced power standby mode when disabled. This allows system designers to achieve their low standby power requirements.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible.