54AC/74AC563 • 54ACT/74ACT563

Octal D-Type Latch With 3-State Outputs

Description

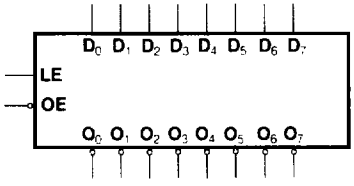
The 'AC/'ACT563 is a high-speed octal latch with buffered common Latch Enable (LE) and buffered common Output Enable ($\overline{OE}$) inputs.

The 'AC/'ACT563 device is functionally identical to the 'AC/'ACT573, but with inverted outputs.

- **Inputs and Outputs on Opposite Sides of Package Allowing Easy Interface with Microprocessors**
- **Useful as Input or Output Port for Microprocessors**
- **Functionally Identical to 'AC/'ACT573 but with Inverted Outputs**
- **Outputs Source/Sink 24 mA**
- **'ACT563 has TTL-Compatible Inputs**

Ordering Code: See Section 6

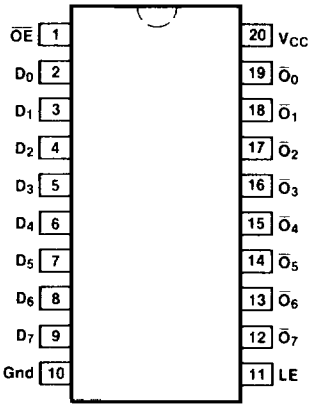
Logic Symbol



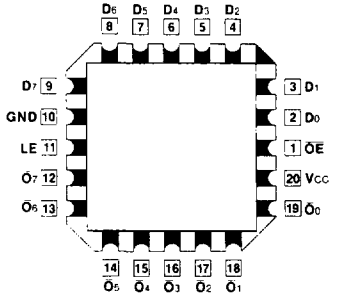
Pin Names

D_0 - D_7	Data Inputs
LE	Latch Enable Input
$\overline{OE}$	3-State Output Enable Input
$\overline{O}_0$ - $\overline{O}_7$	3-State Latch Outputs

Connection Diagrams



Pin Assignment for DIP, Flatpak and SOIC



Pin Assignment for LCC

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Functional Description

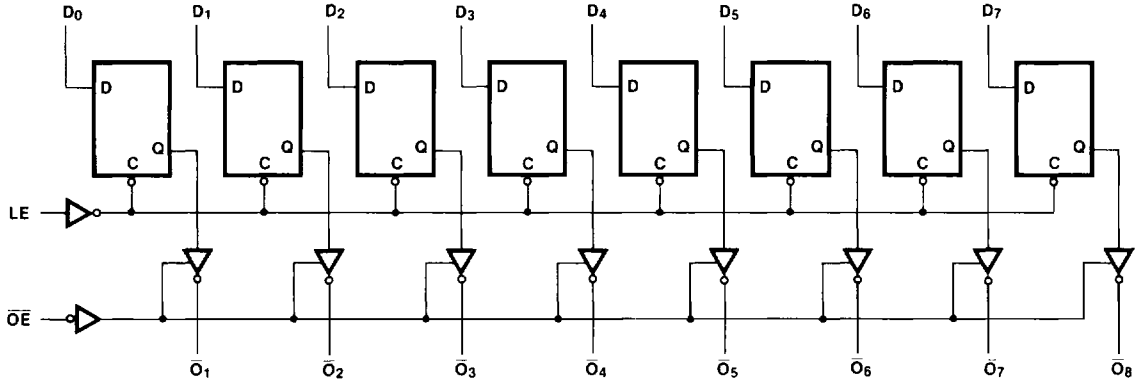
The 'AC/'ACT563 contains eight D-type latches with 3-state complementary outputs. When the Latch Enable (LE) input is HIGH, data on the D_n inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW the latches store the information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE. The 3-state buffers are controlled by the Output Enable ($\overline{OE}$) input. When $\overline{OE}$ is LOW, the buffers are in the bi-state mode. When $\overline{OE}$ is HIGH the buffers are in the high impedance mode but that does not interfere with entering new data into the latches.

Function Table

Inputs			Internal	Outputs	Function
$\overline{OE}$	LE	D	Q	O	
H	X	X	X	Z	High Z
H	H	L	H	Z	High Z
H	H	H	L	Z	High Z
H	L	X	NC	Z	Latched
L	H	L	H	H	Transparent
L	H	H	L	L	Transparent
L	L	X	NC	NC	Latched

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance
NC = No Change

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics (unless otherwise specified)

Symbol	Parameter	54AC/ACT	74AC/ACT	Units	Conditions
I_{CC}	Maximum Quiescent Supply Current	160	80	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, T_A = Worst Case
I_{CC}	Maximum Quiescent Supply Current	8.0	8.0	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, $T_A = 25°C$
I_{CCT}	Maximum Additional Icc/Input ('ACT563)	1.6	1.5	mA	$V_{IN} = V_{CC} - 2.1$ V, $V_{CC} = 5.5$ V, T_A = Worst Case

AC Characteristics

Symbol	Parameter	Vcc* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay D_n to $\overline{O}_n$	3.3 5.0		7.5 5.0						ns	3-5
t_{PHL}	Propagation Delay D_n to $\overline{O}_n$	3.3 5.0		7.0 4.5						ns	3-5
t_{PLH}	Propagation Delay LE to $\overline{O}_n$	3.3 5.0		7.5 5.0						ns	3-6
t_{PHL}	Propagation Delay LE to $\overline{O}_n$	3.3 5.0		8.0 5.5						ns	3-6
t_{PZH}	Output Enable Time	3.3 5.0		6.0 4.0						ns	3-7
t_{PZL}	Output Enable Time	3.3 5.0		6.0 4.0						ns	3-8
t_{PHZ}	Output Disable Time	3.3 5.0		7.0 5.0						ns	3-7
t_{PLZ}	Output Disable Time	3.3 5.0		5.0 3.5						ns	3-8

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

AC Operating Requirements

Symbol	Parameter	Vcc* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF Typ	74AC $T_A = +25°C$, $C_L = 50$ pF Guaranteed Minimum	54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF Guaranteed Minimum	74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF Guaranteed Minimum	Units	Fig. No.
t_s	Setup Time, HIGH or LOW, D_n to LE	3.3 5.0	2.0 1.5				ns	3-9
t_h	Hold Time, HIGH or LOW D_n to LE	3.3 5.0	−2.5 −1.5				ns	3-9
t_w	LE Pulse Width, HIGH	3.3 5.0	3.0 2.5				ns	3-6

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

AC Characteristics

Symbol	Parameter	Vcc* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF Min	Typ	Max	54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF Min	Max	74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF Min	Max	Units	Fig. No.
t_{PLH}	Propagation Delay D_n to $\overline{O}_n$	5.0	1.0	7.0	11.5	1.0	14.0	1.0	12.5	ns	3-5
t_{PHL}	Propagation Delay D_n to $\overline{O}_n$	5.0	1.0	6.0	10.0	1.0	12.0	1.0	11.0	ns	3-5
t_{PLH}	Propagation Delay LE to $\overline{O}_n$	5.0	1.0	6.5	10.5	1.0	12.5	1.0	11.5	ns	3-6
t_{PHL}	Propagation Delay LE to $\overline{O}_n$	5.0	1.0	5.5	9.5	1.0	11.5	1.0	10.5	ns	3-6
t_{PZH}	Output Enable Time	5.0	1.0	5.5	9.0	1.0	11.0	1.0	10.0	ns	3-7
t_{PZL}	Output Enable Time	5.0	1.0	5.5	8.5	1.0	10.5	1.0	9.5	ns	3-8
t_{PHZ}	Output Disable Time	5.0	1.0	6.5	10.5	1.0	12.5	1.0	11.5	ns	3-7
t_{PLZ}	Output Disable Time	5.0	1.0	4.5	8.0	1.0	9.5	1.0	8.5	ns	3-8

*Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

AC Operating Requirements

Symbol	Parameter	Vcc* (V)	74ACT		54ACT	74ACT	Units	Fig. No.
			$T_A = +25°C$ $C_L = 50$ pF		$T_A = -55°C$ to $+125°C$ $C_L = 50$ pF	$T_A = -40°C$ to $+85°C$ $C_L = 50$ pF		
			Typ	Guaranteed Minimum				
t_s	Setup Time, HIGH or LOW, D_n to LE	5.0	1.5	4.0	5.0	4.5	ns	3-9
t_h	Hold Time, HIGH or LOW D_n to LE	5.0	−2.0	0	0	0	ns	3-9
t_w	LE Pulse Width, HIGH	5.0	2.0	3.0	5.0	3.0	ns	3-6

*Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

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Capacitance

Symbol	Parameter	54/74AC/ACT	Units	Conditions
		Typ		
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.5$ V
C_{PD}	Power Dissipation Capacitance	50.0	pF	$V_{CC} = 5.5$ V