Signetics

54LS74A, 54S74
Flip-Flops

Dual D-Type Flip-Flops

Product Specification

Military Logic Products

DESCRIPTION

The 54LS74A, 54S74 is a dual positive edge-triggered D-type flip-flop featuring individual Data, Clock, Set and Reset inputs; also complementary Q and $\overline{Q}$ outputs.

Set ($\overline{S}_D$) and Reset ($\overline{R}_D$) are asynchronous active-Low inputs and operate independently of the clock input. Information on the Data (D) input is transferred to the Q output on the Low-to-High transition of the clock pulse. The D inputs must be stable one setup time prior to the Low-to-High clock transition for predictable operation. Although the Clock input is level-sensitive, the positive transition of the clock pulse between the 0.8V and 2.0V levels should be equal to or less than the clock-to-output delay time for reliable operation.

ORDERING INFORMATION

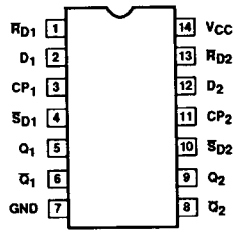
DESCRIPTION	ORDER CODE
14-Pin Ceramic DIP	54LS74A/BCA 54S74/BCA
14-Pin Ceramic FlatPack	54LS74A/BDA 54S74/BDA
14-Pin Ceramic LLCC	54LS74A/B2A 54S74/B2A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54S	54LS
D	Input	1SUL	1LSUL
$\overline{R}_D$	Input	3SUL	2LSUL
$\overline{S}_D$	Input	2SUL	2LSUL
CP	Input	2SUL	1LSUL
Q, $\overline{Q}$	Outputs	10SUL	10LSUL

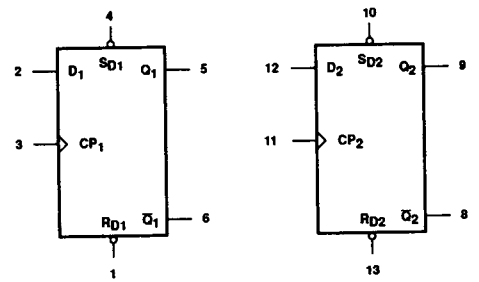
NOTE: Where a 54S Unit Load (SUL) is 50μA I_{IH} and -2.0mA I_{IL}, and 54LS Unit Load (LSUL) is 20μA I_{IH} and -0.4mA I_{IL}.

PIN CONFIGURATION



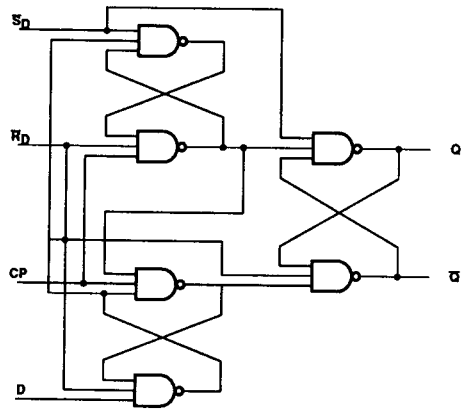
For LLCC pin assignments, see JEDEC Standard No. 2

LOGIC SYMBOL



For LLCC pin assignments, see JEDEC Standard No. 2

LOGIC DIAGRAM



FUNCTION TABLE

OPERATING MODE	INPUTS				OUTPUTS	
	$\overline{S}_D$	$\overline{R}_D$	CP	D	Q	$\overline{Q}$
Asynchronous Set	L	H	X	X	H	L
Asynchronous Reset (Clear)	H	L	X	X	L	H
Undetermined(1)	L	L	X	X	H	H
Load "1" (Set)	H	H	↑	h	H	L
Load "0" (Reset)	H	H	↑	l	L	H

H = High voltage level steady state.
h = High voltage level one setup time prior to the Low-to-High clock transition.
L = Low voltage level steady state.
l = Low voltage level one setup time prior to the Low-to-High clock transition.
X = Don't care.
↑ = Low-to-High clock transition.

NOTE:
(1) Both outputs will be High while both $\overline{S}_D$ and $\overline{R}_D$ are Low, but the output states are unpredictable if $\overline{S}_D$ and $\overline{R}_D$ go High simultaneously.

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	54LS	54S	UNIT
V_{CC}	Supply voltage	7.0	7.0	V
V_I	Input voltage range	-0.5 to +7.0	-0.5 to +5.5	V
I_I	Input current range	-30 to +1	-30 to +5	mA
V_O	Voltage applied to output in High output state range	-0.5 to $+V_{CC}$	-0.5 to $+V_{CC}$	V
T_{STG}	Storage temperature range	-65 to +150	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	54LS			54S			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			2.0			V
V_{IL}	Low-level input voltage			+0.7			+0.8	V
	+125°C			+0.7			+0.7	V
I_{IK}	Input clamp current			-18			-18	mA
I_{OH}	High-level output current			-400			-1000	µA
I_{OL}	Low-level output current			4			20	mA
T_A	Operating free-air temperature range	-55		+125	-55		+125	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]			54LS74A			54S74			UNIT
					Min	Typ[2]	Max	Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC} = Min, V_{IH} = Min, V_{IL} = Max, I_{OH} = Max			2.5	3.4		2.5	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = Min, V_{IH} = Min, V_{IL} = Max,				0.25	0.4			0.5	V
		I_{OL} = Max	+125 °C				0.4			0.45	V
V_{IK}	Input clamp voltage	V_{CC} = Min, I_I = I_{IK}					-1.5			-1.2	V
I_{IH2}	Input current at maximum input voltage	V_{CC} = Max	V_I = 5.5V							1.0	mA
			V_I = 7.0V	D input			0.1				mA
				$\overline{R}_D$ input			0.2				mA
				$\overline{S}_D$ input			0.2				mA
				CP input			0.1				mA
I_{IH1}	High-level input current	V_{CC} = Max, V_I = 2.7V		D input			20			50	µA
				$\overline{R}_D$ input			40			150	µA
				$\overline{S}_D$ input			40			100	µA
				CP input			20			100	µA
I_{IL}	Low-level input current[5]	V_{CC} = Max	V_I = 0.4V	D input			-0.4				mA
				$\overline{R}_D$ input			-0.8				mA
				$\overline{S}_D$ input			-0.8				mA
				CP input			-0.4				mA
			V_I = 0.5V	D input						-2	mA
				$\overline{R}_D$ input						-6	mA
				$\overline{S}_D$ input						-4	mA
				CP input						-4	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = Max			-20		-100	-40		-110	mA
I_{CC}	Supply current[4] (total)	V_{CC} = Max				4	8		30	50	mA

AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V[6]

SYMBOL	PARAMETER	TEST CONDITIONS	54LS		54S		UNIT
			C_L = 15pF		C_L = 15pF		
			Min	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	25		75		MHz
t_{PLH} t_{PHL}	Propagation delay Clock to output	Waveform 1		25 40		9 9	ns ns
t_{PLH}	Propagation delay	Waveform 2		25		6	ns
t_{PHL}	Set or Reset to output	Waveform 2 CP = High		40		13.5	ns
t_{PHL}	Set or Reset to output	Waveform 2 CP = Low		40		8	ns

AC SETUP REQUIREMENTS T_A = 25°C, V_{CC} = 5.0V

SYMBOL	PARAMETER	TEST CONDITIONS	54LS		54S		UNIT
			Min	Max	Min	Max	
t_w(H)	Clock pulse width (High)	Waveform 1	25		6		ns
t_w(L)	Clock pulse width (Low)	Waveform 1			7.3		ns
t_w(L)	Set or reset pulse width (Low)	Waveform 2	25		7		ns
t_s(H)	Setup time (High) data to clock	Waveform 1	20		3		ns
t_s(L)	Setup time (Low) data to clock	Waveform 1	20		3		ns
t_h	Hold time data to clock	Waveform 1	5		2		ns

AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

SYMBOL	PARAMETER	TEST CONDITIONS	54LS		54S		UNIT
			C_L = 50pF		C_L = 50pF		
			Min	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	25		75		MHz
t_{PLH} t_{PHL}	Propagation delay Clock to output	Waveform 1		30 45		13 10	ns ns
t_{PLH}	Propagation delay	Waveform 2		30		8.0	ns
t_{PHL}	Set or Reset to output	Waveform 2 CP = High		45		16	ns
t_{PHL}	Set or Reset to output	Waveform 2 CP = Low		45		10	ns

AC ELECTRICAL CHARACTERISTICS T_A = -55°C and +125°C, V_{CC} = 5.0V[6]

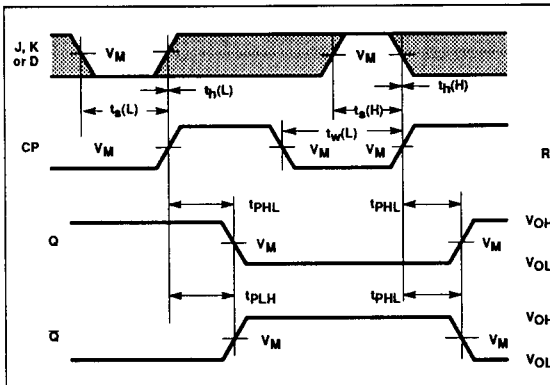
SYMBOL	PARAMETER	TEST CONDITIONS	54LS		54S		UNIT
			C_L = 50pF		C_L = 50pF		
			Min	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	25		55		MHz
t_{PLH} t_{PHL}	Propagation delay Clock to output	Waveform 1		39 59		16 13	ns ns
t_{PLH}	Propagation delay	Waveform 2		39		10	ns
t_{PHL}	Set or Reset to output	Waveform 2 CP = High		59		19	ns
t_{PHL}	Set or Reset to output	Waveform 2 CP = Low		59		13	ns

AC SETUP REQUIREMENTS T_A = -55°C and +125°C, V_{CC} = 5.0V[6]

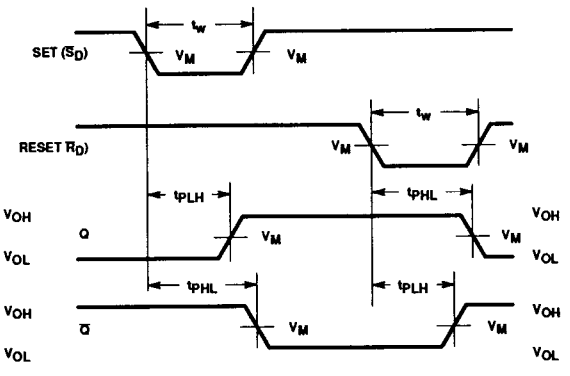
SYMBOL	PARAMETER	TEST CONDITIONS	54LS		54S		UNIT
			Min	Max	Min	Max	
$t_w(H)$	Clock pulse width (High)	Waveform 1	25		8		ns
$t_w(L)$	Clock pulse width (Low)	Waveform 1			10		ns
$t_w(L)$	Set or reset pulse width (Low)	Waveform 2	35		10		ns
$t_s(H)$	Setup time (High) data to clock	Waveform 1	20		4		ns
$t_s(L)$	Setup time (Low) data to clock	Waveform 1	20		4		ns
t_h	Hold time data to clock	Waveform 1	5		2		ns

NOTES:
1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type and function table operating mode.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. Measure I_{CC} with the Clock inputs grounded and all outputs open, with the Q and $\overline{Q}$ outputs High in turn.
5. Set is tested with reset High and reset is tested with set High.
6. These parameters are guaranteed, but not tested.

AC WAVEFORMS



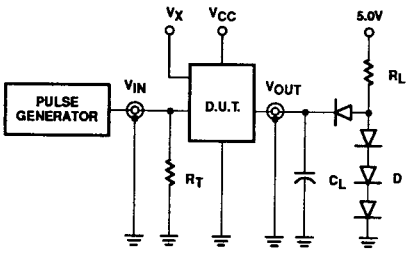
Waveform 1. Clock to Output Delays, Data Setup and Hold Times, Clock Pulse Width



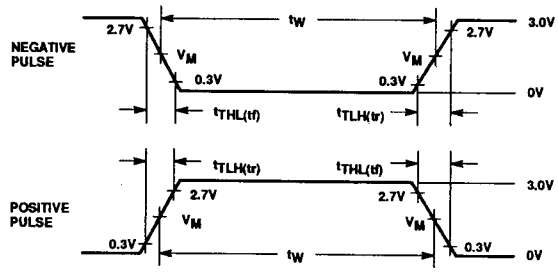
Waveform 2. Set and Reset to Output Delays, Set and Reset Pulse Widths

NOTE: V_M = 1.3V for 54LS; V_M = 1.5V for all other TTL families.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORM



Test Circuit for 54 Totem-Pole Outputs



Input Pulse Definition

FAMILY	INPUT PULSE CHARACTERISTICS					
	R_L	V_M	Rep. Rate	T_W	T_{TLH}	T_{THL}
54LSXXX	2.0kΩ	1.3V	1MHz	500ns	≤15ns	≤6ns
54SXXX	280Ω	1.5V	1MHz	500ns	≤2.5ns	≤2.5ns

DEFINITIONS:

C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
V_X = Unclocked pins must be held at ≤0.8V, ≥2.7V or open per FunctionTable.