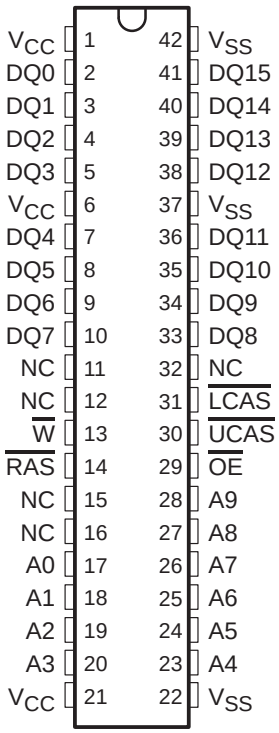
This data sheet is applicable to TMS418169A and TMS428169A symbolized by Revision "E", and subsequent revisions as described in the device symbolization section.

- **Organization . . . 1048576 by 16 Bits**
- **Single 5-V Power Supply for TMS418169A (± 10% Tolerance)**
- **Single 3.3-V Power Supply for TMS428169A (± 0.3 V Tolerance)**
- **1024-Cycle Refresh in 16 ms**
- **Performance Ranges:**

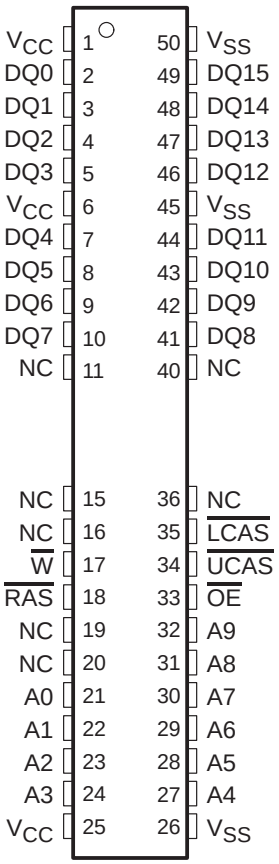
	ACCESS TIME t_{RAC} MAX	ACCESS TIME t_{CAC} MAX	ACCESS TIME t_{AA} MAX	READ OR EDO CYCLE MIN
'418169A-50	50 ns	13 ns	25 ns	20 ns
'418169A-60	60 ns	15 ns	30 ns	25 ns
'418169A-70	70 ns	18 ns	35 ns	30 ns
'428169A-60	60 ns	15 ns	30 ns	25 ns
'428169A-70	70 ns	18 ns	35 ns	30 ns

- **Extended-Data-Out (EDO) Operation**
- **$\overline{\text{xCAS}}$-Before-$\overline{\text{RAS}}$ (xCBR) Refresh**
- **3-State Unlatched Output**
- **Low Power Dissipation**
- **High-Reliability Plastic 42-Lead 400-Mil-Wide Surface-Mount Small-Outline J-Lead (SOJ) Package (DZ Suffix) and 44/50-Lead Surface-Mount Thin Small-Outline Package (TSOP) (DGE Suffix)**
- **Ambient Temperature Range 0°C to 70°C**

DZ PACKAGE (TOP VIEW)



DGE PACKAGE (TOP VIEW)



description

The TMS418169A and TMS428169A are 16777216-bit dynamic random-access memory (DRAM) devices organized as 1048576 words of 16 bits each. They employ state-of-the-art technology for high performance, reliability, and low power at low cost.

PIN NOMENCLATURE

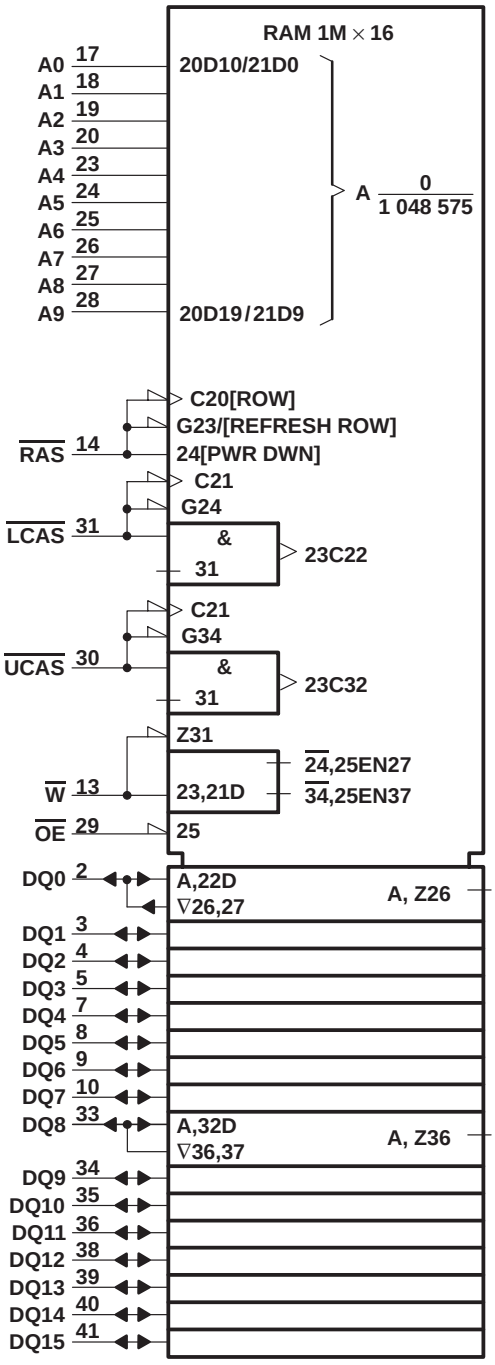
A[0:9]	Address Inputs
DQ[0:15]	Data In / Data Out
$\overline{\text{LCAS}}$	Lower Column-Address Strobe
$\overline{\text{UCAS}}$	Upper Column-Address Strobe
NC	No Internal Connection
$\overline{\text{OE}}$	Output Enable
$\overline{\text{RAS}}$	Row-Address Strobe
V_{CC}	5-V or 3.3-V Supply
V_{SS}	Ground
$\overline{\text{W}}$	Write Enable

The TMS418169A features maximum $\overline{\text{RAS}}$ access times of 50-, 60-, and 70 ns, and the TMS428169A features maximum $\overline{\text{RAS}}$ access times of 60- and 70 ns. All addresses and data-in lines are latched on-chip to simplify system design. Data out is unlatched to allow greater system flexibility.

The TMS418169A is offered in a 42-lead plastic surface-mount SOJ package (DZ suffix). The TMS428169A is offered in a 44/50-lead plastic surface-mount TSOP (DGE suffix). These packages are designed for operation from 0°C to 70°C.

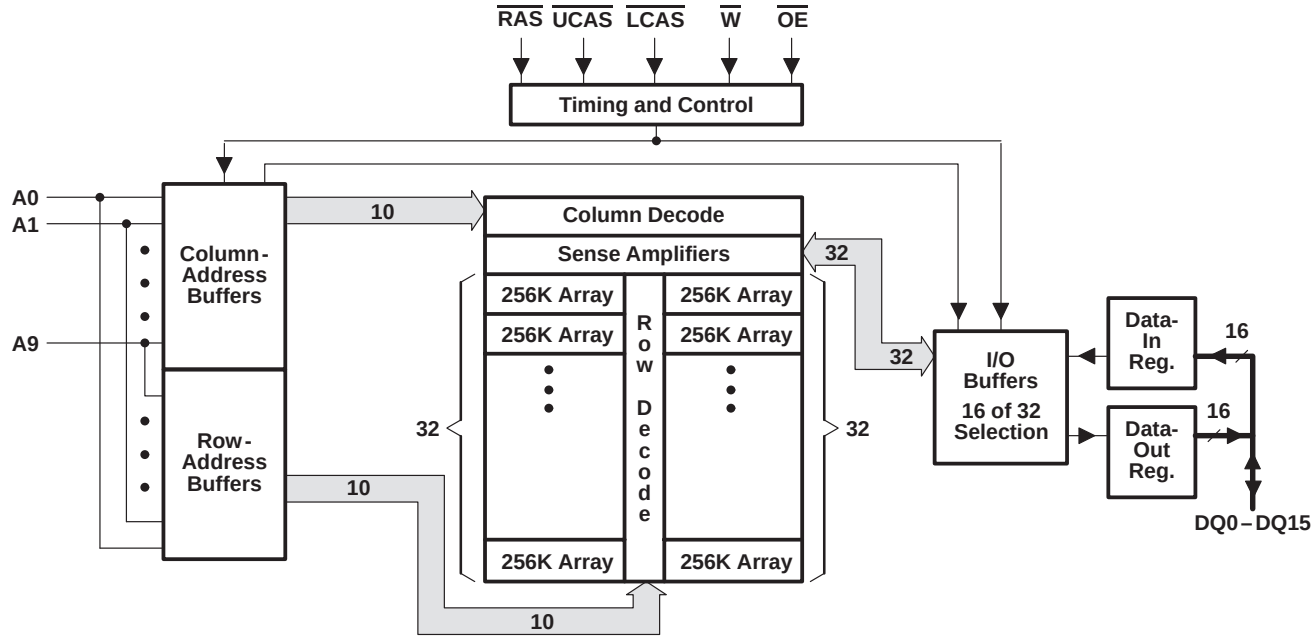
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

logic symbol (TMS418169A and TMS428169A)†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
The pin numbers shown correspond to the DZ package.

functional block diagram (TMS418169A and TMS428169A)



operation

dual $\overline{\text{xCAS}}$

Two $\overline{\text{xCAS}}$ pins ($\overline{\text{LCAS}}$ and $\overline{\text{UCAS}}$) are provided to give independent control of the 16 data I/O pins (DQ0–DQ15), with $\overline{\text{LCAS}}$ corresponding to DQ0–DQ7 and $\overline{\text{UCAS}}$ corresponding to DQ8–DQ15. Each $\overline{\text{xCAS}}$ going low enables its corresponding DQx pins.

In write cycles, data-in setup and hold times (t_{DS} and t_{DH}) and write-command setup and hold times (t_{WCS}, t_{CWL}, and t_{WCH}) must be satisfied for each individual $\overline{\text{xCAS}}$ to ensure writing into the storage cells of the corresponding DQ pins.

Different modes of operation for upper and lower bytes in one cycle are not allowed, such as the example in Figure 1.

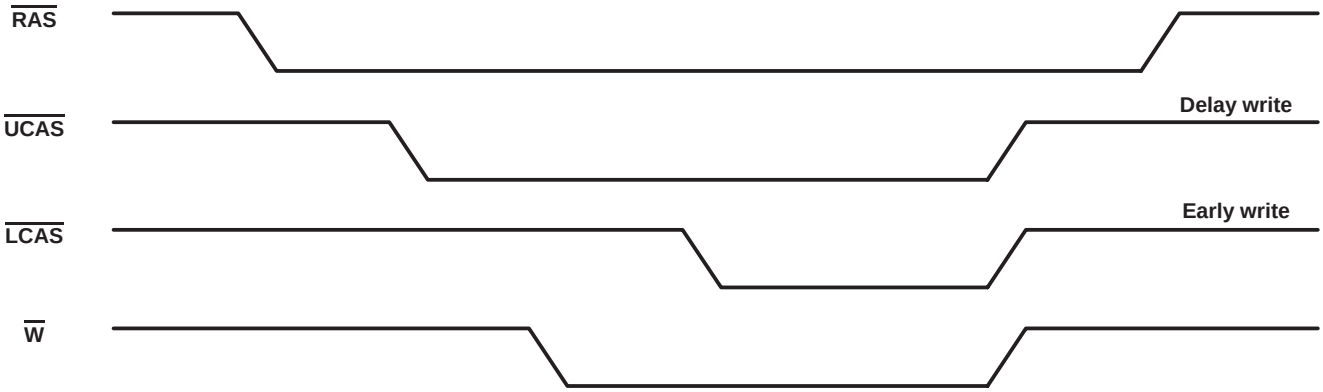


Figure 1. Illegal Dual-$\overline{\text{xCAS}}$ Operation

extended data out

Extended data out (EDO) allows for data output rates of up to 50 MHz for 50-ns devices. When keeping the same row address while selecting random column addresses, the time for row-address setup-and-hold and address multiplexing is eliminated. The maximum number of columns that can be accessed is determined by t_{RASP}, the maximum $\overline{RAS}$ low time.

EDO does not enter the DQs into the high-impedance state with the rising edge of $\overline{xCAS}$. The output remains valid for the system to latch the data. After $\overline{xCAS}$ goes high, the DRAM decodes the next address. $\overline{OE}$ and $\overline{W}$ can be used to control the output impedance. Descriptions of $\overline{OE}$ and $\overline{W}$ further explain the benefit of EDO operation.

address: A0 – A9

Twenty address bits are required to decode each of the 1048576 storage cell locations. Ten row-address bits are set up on A0 – A9 and latched on the chip by $\overline{RAS}$. Ten column-address bits are set up on A0 – A9 and latched on the chip by the first $\overline{xCAS}$. All addresses must be stable on or before the falling edge of $\overline{RAS}$ and $\overline{xCAS}$. $\overline{RAS}$ is similar to a chip-enable in that it activates the sense amplifiers as well as the row decoder. $\overline{xCAS}$ is used as a chip-select, activating its corresponding output buffer and latching the address bits into the column-address buffers.

The column address is latched on the first $\overline{xCAS}$ falling edge with address setup and hold parameters referenced to that edge. In order to latch in a new column address, both $\overline{xCAS}$ pins must be brought high. The column-precharge time (see parameter t_{CP}) is measured from the last $\overline{xCAS}$ rising edge to the first $\overline{xCAS}$ falling edge of the new cycle. Keeping a column address valid while toggling $\overline{xCAS}$ requires a minimum setup time, t_{CLCH}. During t_{CLCH}, at least one $\overline{xCAS}$ must be brought low before the other $\overline{xCAS}$ is taken high.

write enable ($\overline{W}$)

The read- or write mode is selected through $\overline{W}$. A logic high on $\overline{W}$ selects the read mode and a logic low selects the write mode. The data input is disabled when the read mode is selected. When $\overline{W}$ goes low prior to $\overline{xCAS}$ (early write), data out remains in the high-impedance state for the entire cycle, permitting a write operation independent of the state of $\overline{OE}$. This permits early-write operations to be completed with $\overline{OE}$ grounded. If $\overline{W}$ goes low in an EDO-read cycle, the DQ pins go into the high-impedance state as long as $\overline{xCAS}$ is high (see Figure 9).

data in (DQ0 – DQ15)

Data is written during a write- or read-modify-write cycle. Depending on the mode of operation, the falling edge of $\overline{xCAS}$ or $\overline{W}$ strobes data into the on-chip data latch. In an early-write cycle, $\overline{W}$ is brought low prior to an $\overline{xCAS}$ falling edge, and data is strobed into the on-chip data latch for the corresponding DQ pins with setup-and-hold times referenced to this $\overline{xCAS}$ signal.

In a delayed-write- or read-modify-write cycle, $\overline{xCAS}$ is already low and data is strobed in by $\overline{W}$ with setup-and-hold times referenced to this signal. Also, $\overline{OE}$ must be high to bring the output buffers to the high-impedance state prior to impressing data on the I/O lines (see parameter t_{OED}).

data out (DQ0 – DQ15)

Data out is the same polarity as data in. The output is in the high-impedance (floating) state until $\overline{xCAS}$ and $\overline{OE}$ are brought low. In a read cycle, the output becomes valid after the access-time interval t_{CAC} (which begins with the negative transition of $\overline{xCAS}$) as long as t_{RAC} and t_{AA} are satisfied. The delay time from $\overline{xCAS}$ low to valid data out is measured from each individual $\overline{xCAS}$ to its corresponding DQx pin.

output enable ($\overline{OE}$)

$\overline{OE}$ controls the impedance of the output buffers. While $\overline{xCAS}$ and $\overline{RAS}$ are low and $\overline{W}$ is high, $\overline{OE}$ can be brought low or high and the DQs transition between valid data and high impedance. There are two methods of placing the DQs into the high-impedance state and keeping them in that state during $\overline{xCAS}$ high time by using $\overline{OE}$. The first method is to transition $\overline{OE}$ high before $\overline{xCAS}$ transitions high and to keep $\overline{OE}$ high for t_{CHO} past the $\overline{xCAS}$ transition. This disables the DQs and they remain in the high-impedance state, regardless of $\overline{OE}$, until $\overline{xCAS}$ falls again (see Figure 8). The second method is to have $\overline{OE}$ low as $\overline{xCAS}$ transitions high. Then $\overline{OE}$ can pulse high for a minimum of t_{OEP} anytime during $\overline{xCAS}$ high time, disabling the DQs regardless of further transitions on $\overline{OE}$ until $\overline{xCAS}$ falls again (see Figure 8).

$\overline{RAS}$-only refresh

A refresh operation must be performed at least once every 16 ms to retain data. This is achieved by strobing each of the 1024 rows (A0–A9). A normal read or write cycle refreshes all bits in each row that is selected. A $\overline{RAS}$-only operation can be used by holding both $\overline{xCAS}$ pins at the high (inactive) level, conserving power as the output buffers remain in the high-impedance state. Externally generated addresses must be used for a $\overline{RAS}$-only refresh.

hidden refresh

Hidden refresh can be performed while maintaining valid data at the output pins. This is accomplished by holding $\overline{xCAS}$ at V_{IL} after a read operation and cycling $\overline{RAS}$ after a specified precharge period, similar to a $\overline{RAS}$-only refresh cycle. The external address is ignored and the refresh address is generated internally.

$\overline{xCAS}$-before-$\overline{RAS}$ (xCBR) refresh

xCBR refresh is achieved by bringing at least one $\overline{xCAS}$ low earlier than $\overline{RAS}$ (see parameter t_{CSR}) and holding it low after $\overline{RAS}$ falls (see parameter t_{CHR}). For successive xCBR refresh cycles, $\overline{xCAS}$ can remain low while cycling $\overline{RAS}$. The external address is ignored and the refresh address is generated internally.

power-up

To achieve proper device operation, an initial pause of 200 µs, followed by a minimum of eight initialization cycles, is required after power up to the full V_{CC} level. These eight initialization cycles must include at least one refresh ($\overline{RAS}$-only or xCBR) cycle.

absolute maximum ratings over ambient temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}: TMS418169A . . . . . – 1 V to 7 V
TMS428169A . . . . . – 0.5 V to 4.6 V
Voltage range on any pin (see Note 1): TMS418169A . . . . . – 1 V to 7 V
TMS428169A . . . . . – 0.5 V to 4.6 V
Short-circuit output current . . . . . 50 mA
Power dissipation . . . . . 1 W
Ambient temperature range, T_A . . . . . 0°C to 70°C
Storage temperature range, T_{stg} . . . . . – 55°C to 125°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS}.

recommended operating conditions

		’418169A			’428169A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	3	3.3	3.6	V
V_{SS}	Supply voltage		0			0		V
V_{IH}	High-level input voltage	2.4		6.5	2		V_{CC} + 0.3	V
V_{IL}	Low-level input voltage (see Note 2)	– 1		0.8	– 0.3		0.8	V
T_A	Ambient temperature	0		70	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used for logic-voltage levels only.

TMS418169A

electrical characteristics over recommended ranges of supply voltage and ambient temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	'418169A-50		'418169A-60		'418169A-70		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 5 mA	2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA		0.4		0.4		0.4	V
I_I	Input current (leakage)	V_{CC} = 5.5 V, V_I = 0 V to 6.5 V, All others = 0 V to V_{CC}		± 10		± 10		± 10	µA
I_O	Output current (leakage)	V_{CC} = 5.5 V, V_O = 0 V to V_{CC}, $\overline{xCAS}$ high		± 10		± 10		± 10	µA
I_{CC1}‡§	Average read- or write-cycle current	V_{CC} = 5.5 V, Minimum cycle		180		160		150	mA
I_{CC2}	Average standby current	V_{IH} = 2.4 V (TTL), After one memory cycle, $\overline{RAS}$ and $\overline{xCAS}$ high		2		2		2	mA
		V_{IH} = V_{CC} – 0.2 V (CMOS), After one memory cycle, $\overline{RAS}$ and $\overline{xCAS}$ high		1		1		1	mA
I_{CC3}§	Average refresh current ($\overline{RAS}$-only refresh or xCBR)	V_{CC} = 5.5 V, Minimum cycle, $\overline{RAS}$ cycling, $\overline{xCAS}$ high ($\overline{RAS}$ only), $\overline{xCAS}$ before $\overline{RAS}$ (xCBR)		180		160		150	mA
I_{CC4}‡¶	Average EDO current	V_{CC} = 5.5 V, t_{HPC} = MIN, $\overline{RAS}$ low, $\overline{xCAS}$ cycling		140		110		100	mA

† For conditions shown as MIN/MAX, use the appropriate value specified in the timing requirements.
‡ Measured with outputs open
§ Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}
¶ Measured with a maximum of one address change during each EDO cycle, t_{HPC}

TMS428169A

electrical characteristics over recommended ranges of supply voltage and ambient conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		'428169A-60 MIN	'428169A-60 MAX	'428169A-70 MIN	'428169A-70 MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = – 2 mA	LVTTL	2.4		2.4		V
		I_{OH} = – 100 µA	LVCMOS	V_{CC}–0.2		V_{CC}–0.2		
V_{OL}	Low-level output voltage	I_{OL} = 2 mA	LVTTL		0.4		0.4	V
		I_{OL} = 100 µA	LVCMOS		0.2		0.2	
I_I	Input current (leakage)	V_{CC} = 3.6 V, V_I = 0 V to 3.9 V, All others = 0 V to V_{CC}			± 10		± 10	µA
I_O	Output current (leakage)	$\overline{V_{CC}}$ = 3.6 V, V_O = 0 V to V_{CC}, $\overline{xCAS}$ high			± 10		± 10	µA
I_{CC1}‡§	Average read- or write-cycle current	V_{CC} = 3.6 V, Minimum cycle			150		140	mA
I_{CC2}	Average standby current	V_{IH} = 2 V (LVTTL), After one memory cycle, $\overline{RAS}$ and $\overline{xCAS}$ high			2		2	mA
		V_{IH} = V_{CC} – 0.2 V (LVCMOS), After one memory cycle, $\overline{RAS}$ and $\overline{xCAS}$ high			1		1	mA
I_{CC3}§	Average refresh current (RAS-only refresh or xCBR)	$\overline{V_{CC}}$ = 3.6 V, Minimum cycle, $\overline{RAS}$ cycling, $\overline{xCAS}$ high (RAS-only refresh) $\overline{xCBR}$			150		140	mA
I_{CC4}‡¶	Average EDO current	$\overline{V_{CC}}$ = 3.6 V, t_{HPC} = MIN, $\overline{RAS}$ low, $\overline{xCAS}$ cycling			110		100	mA

† For conditions shown as MIN/MAX, use the appropriate value specified in the timing requirements.
‡ Measured with outputs open
§ Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}
¶ Measured with a maximum of one address change during each EDO cycle, t_{HPC}

capacitance over recommended ranges of supply voltage and ambient temperature, f = 1 MHz (see Note 3)

PARAMETER		MIN	MAX	UNIT
$C_{i(A)}$	Input capacitance, A0–A9		5	pF
$C_{i(OE)}$	Input capacitance, $\overline{OE}$		7	pF
$C_{i(RC)}$	Input capacitance, $\overline{xCAS}$ and $\overline{RAS}$		7	pF
$C_{i(W)}$	Input capacitance, $\overline{W}$		7	pF
C_O	Output capacitance†		7	pF

† $\overline{xCAS}$ and $\overline{OE}$ = V_{IH} to disable outputs

NOTE 3: V_{CC} = 5 V ± 0.5 V or 3.3 V ± 0.3 V, and the bias on pins under test is 0 V.

switching characteristics over recommended ranges of supply voltage and ambient temperature (see Note 4)

PARAMETER		’418169A-50		’418169A-60 ’428169A-60		’418169A-70 ’428169A-70		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{AA}	Access time from column address (see Note 5)		25		30		35	ns
t_{CAC}	Access time from $\overline{xCAS}$ (see Note 5)		13		15		18	ns
t_{CPA}	Access time from $\overline{xCAS}$ precharge (see Note 5)		28		35		40	ns
t_{RAC}	Access time from $\overline{RAS}$ (see Note 5)		50		60		70	ns
t_{OEA}	Access time from $\overline{OE}$ (see Note 5)		13		15		18	ns
t_{CLZ}	Delay time, $\overline{xCAS}$ to output in the low-impedance state	0		0		0		ns
t_{OEZ}	Output buffer turnoff delay from $\overline{OE}$ (see Note 6)	3	13	3	15	3	18	ns
t_{REZ}	Output buffer turnoff delay from $\overline{RAS}$ (see Note 6)	3	13	3	15	3	18	ns
t_{CEZ}	Output buffer turnoff delay from $\overline{xCAS}$ (see Note 6)	3	13	3	15	3	18	ns
t_{WEZ}	Output buffer turnoff delay from $\overline{W}$ (see Note 6)	3	13	3	15	3	18	ns

NOTES: 4. With ac parameters, it is assumed that t_T = 2 ns.
5. Access times for TMS428169A are measured with output reference levels of V_{OH} = 2 V and V_{OL} = 0.8 V.
6. The MAX specifications of t_{REZ}, t_{CEZ}, t_{WEZ}, and t_{OEZ} are specified when the output is no longer driven. Data-in should not be driven until one of the applicable maximum specifications is satsified.

EDO timing requirements (see Note 4)

		’418169A-50		’418169A-60 ’428169A-60		’418169A-70 ’428169A-70		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{HPC}	Cycle time, EDO page-mode read or write	20		25		30		ns
t_{PRWC}	Cycle time, EDO read-write	57		68		78		ns
t_{CSH}	Delay time, $\overline{RAS}$ active to $\overline{xCAS}$ precharge	40		48		58		ns
t_{CHO}	Hold time, $\overline{OE}$ from $\overline{xCAS}$	7		10		10		ns
t_{DOH}	Hold time, output from $\overline{xCAS}$ active	5		5		5		ns
t_{CAS}	Pulse duration, $\overline{xCAS}$ active (see Note 7)	8	10000	10	10000	12	10000	ns
t_{WPE}	Pulse duration, $\overline{W}$ (output disable only)	7		7		7		ns
t_{CP}	Pulse duration, $\overline{xCAS}$ precharge	8		10		10		ns
t_{OCH}	Setup time, $\overline{OE}$ before $\overline{xCAS}$	8		10		10		ns
t_{OEP}	Precharge time, $\overline{OE}$ (output disable only)	5		5		5		ns

NOTES: 4. With ac parameters, it is assumed that t_T = 2 ns.
7. In a read-write cycle, t_{CWD} and t_{CWL} must be observed.

ac timing requirements (see Note 4)

		’418169A-50		’418169A-60 ’428169A-60		’418169A-70 ’428169A-70		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{RC}	Cycle time, read	84		104		124		ns
t_{WC}	Cycle time, write	84		104		124		ns
t_{RWC}	Cycle time, read-write	111		135		160		ns
t_{RASP}	Pulse duration, $\overline{RAS}$ active, page mode (see Note 8)	50	100 000	60	100 000	70	100 000	ns
t_{RAS}	Pulse duration, $\overline{RAS}$ active, nonpage mode (see Note 8)	50	10 000	60	10 000	70	10 000	ns
t_{RP}	Pulse duration, $\overline{RAS}$ precharge	30		40		50		ns
t_{WP}	Pulse duration, write command	8		10		10		ns
t_{ASC}	Setup time, column address	0		0		0		ns
t_{ASR}	Setup time, row address	0		0		0		ns
t_{DS}	Setup time, data in (see Note 9)	0		0		0		ns
t_{RCS}	Setup time, read command	0		0		0		ns
t_{CWL}	Setup time, write command before $\overline{xCAS}$ precharge	8		10		12		ns
t_{RWL}	Setup time, write command before $\overline{RAS}$ precharge	8		10		12		ns
t_{WCS}	Setup time, write command before $\overline{xCAS}$ active (early-write only)	0		0		0		ns
t_{WRP}	Setup time, write before $\overline{RAS}$ active (xCBR refresh only)	10		10		10		ns
t_{CSR}	Setup time, $\overline{xCAS}$ referenced to $\overline{RAS}$ (xCBR refresh only)	5		5		5		ns
t_{CAH}	Hold time, column address	8		10		12		ns
t_{DH}	Hold time, data in (see Note 9)	8		10		12		ns
t_{RAH}	Hold time, row address	8		10		10		ns
t_{RCH}	Hold time, read command referenced to $\overline{xCAS}$ (see Note 10)	0		0		0		ns
t_{RRH}	Hold time, read command referenced to $\overline{RAS}$ (see Note 10)	0		0		0		ns
t_{WCH}	Hold time, write command during $\overline{xCAS}$ active (early-write only)	8		10		12		ns
t_{CLCH}	Hold time, $\overline{xCAS}$ low to $\overline{xCAS}$ high	5		5		5		ns
t_{RHCP}	Hold time, $\overline{RAS}$ active from $\overline{xCAS}$ precharge	28		35		40		ns
t_{OEH}	Hold time, $\overline{OE}$ command	13		15		18		ns
t_{ROH}	Hold time, $\overline{RAS}$ referenced to $\overline{OE}$	8		10		10		ns
t_{WRH}	Hold time, write after $\overline{RAS}$ active (xCBR refresh only)	10		10		10		ns
t_{AWD}	Delay time, column address to write command (read-write only)	42		49		57		ns
t_{CHR}	Delay time, $\overline{xCAS}$ referenced to $\overline{RAS}$ (xCBR refresh only)	8		10		10		ns
t_{CRP}	Delay time, $\overline{xCAS}$ precharge to $\overline{RAS}$	5		5		5		ns
t_{CWD}	Delay time, $\overline{xCAS}$ to write command (read-write operation only)	30		34		40		ns

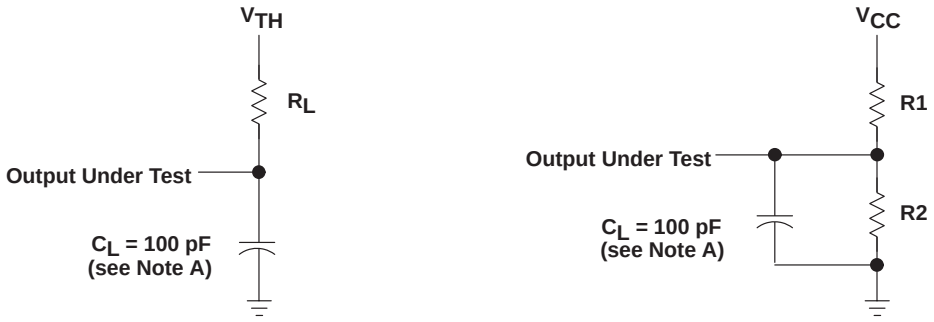
NOTES: 4. With ac parameters, it is assumed that t_T = 2 ns.
8. In a read-write cycle, t_{RWD} and t_{RWL} must be observed.
9. Referenced to the later of $\overline{xCAS}$ or $\overline{W}$ in write operations
10. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

ac timing requirements (see Note 4) (continued)

			’418169A-50		’418169A-60 ’428169A-60		’418169A-70 ’428169A-70		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{OED}	Delay time, $\overline{OE}$ to data in		13		15		18		ns
t_{RAD}	Delay time, $\overline{RAS}$ to column address (see Note 11)		10	25	12	30	12	35	ns
t_{RAL}	Delay time, column address to $\overline{RAS}$ precharge		25		30		35		ns
t_{CAL}	Delay time, column address to $\overline{xCAS}$ precharge		18		20		25		ns
t_{RCD}	Delay time, $\overline{RAS}$ to $\overline{xCAS}$ (see Note 11)		12	37	14	45	14	52	ns
t_{RPC}	Delay time, $\overline{RAS}$ precharge to $\overline{xCAS}$		5		5		5		ns
t_{RSH}	Delay time, $\overline{xCAS}$ active to $\overline{RAS}$ precharge		8		10		12		ns
t_{RWD}	Delay time, $\overline{RAS}$ active to write command (read-write only)		67		79		92		ns
t_{CPW}	Delay time, $\overline{xCAS}$ precharge to write command (read-write only)		45		54		62		ns
t_{REF}	Refresh time interval	’418169A		16		16		16	ms
		’428169A		16		16		16	ms
t_T	Transition time		2	30	2	30	2	30	ns

NOTES: 4. With ac parameters, it is assumed that t_T = 2 ns.
11. The maximum value is specified only to assure access time.

PARAMETER MEASUREMENT INFORMATION



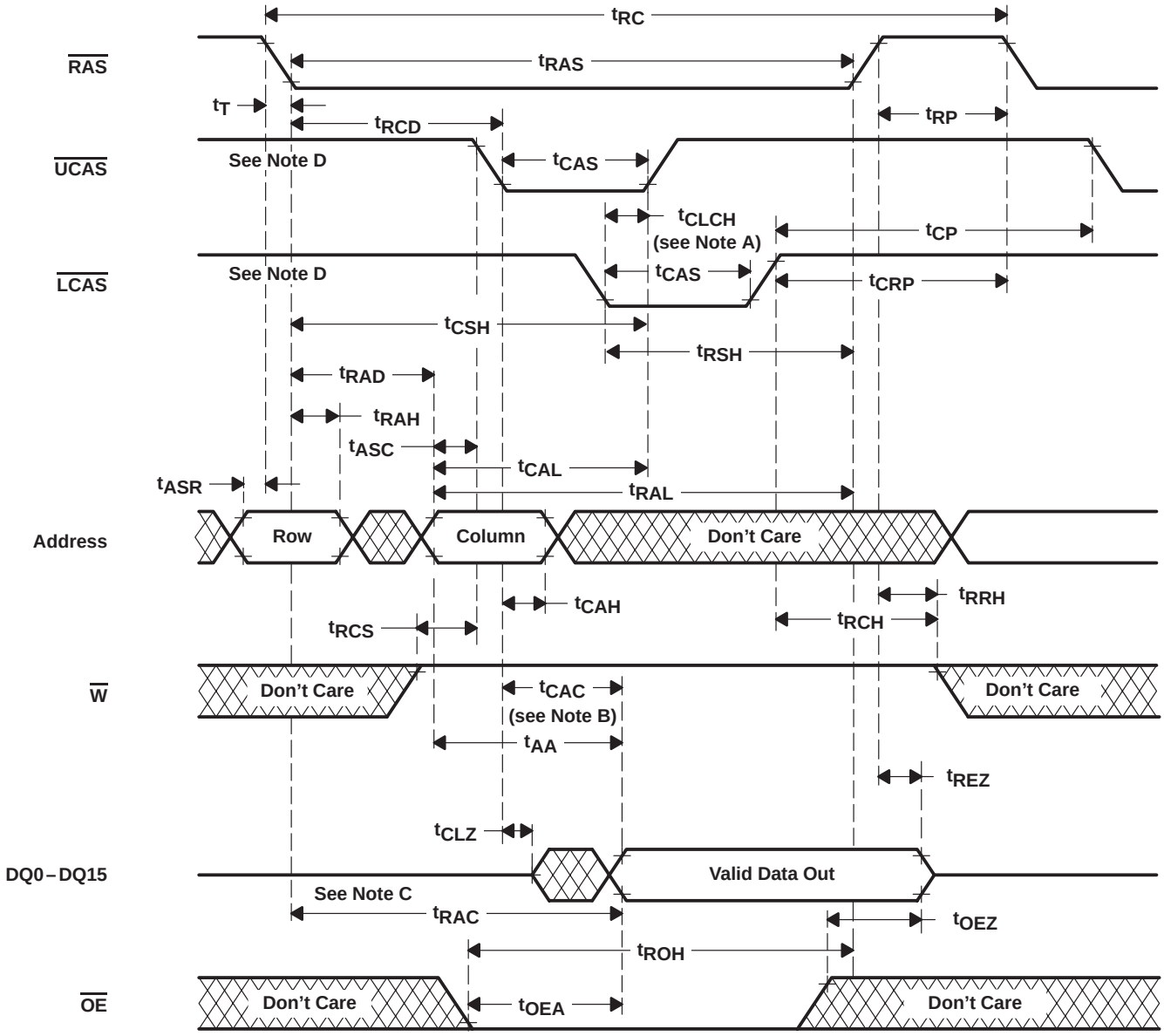
(a) LOAD CIRCUIT **(b) ALTERNATE LOAD CIRCUIT**

NOTE A: C_L includes probe and fixture capacitance.

DEVICE	V_{CC} (V)	R1 (Ω)	R2 (Ω)	V_{TH} (V)	R_L (Ω)
’418169A	5	828	295	1.31	218
’428169A	3.3	1178	868	1.4	500

Figure 2. Load Circuits for Timing Parameters

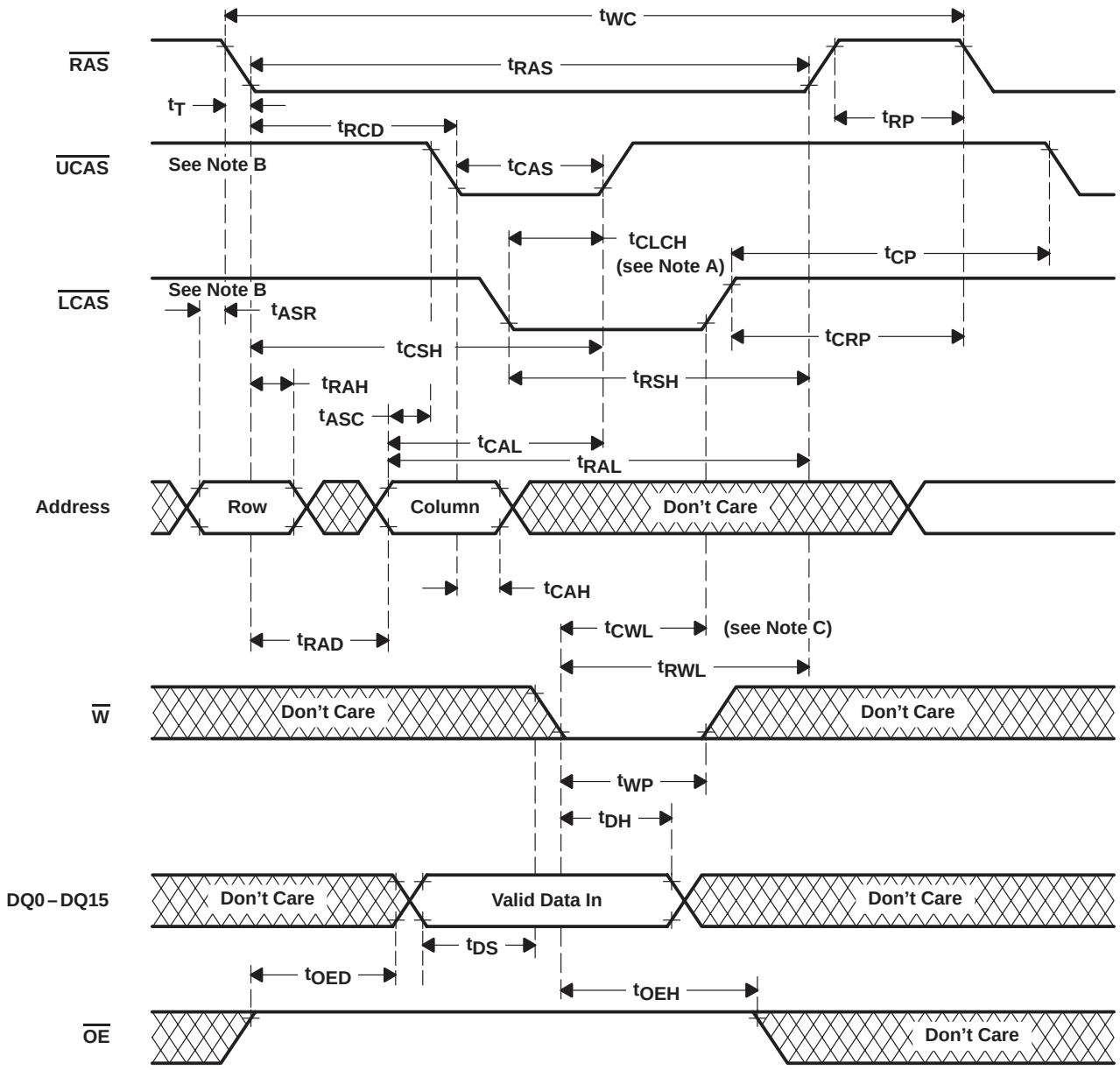
PARAMETER MEASUREMENT INFORMATION



NOTES: A. To hold the address latched by the first $\overline{\text{xCAS}}$ going low, the parameter t_{CLCH} must be met.
B. t_{CAC} is measured from $\overline{\text{xCAS}}$ to its corresponding DQx.
C. Output can go from the high-impedance state to an invalid-data state prior to the specified access time.
D. $\overline{\text{xCAS}}$ order is arbitrary.

Figure 3. Read-Cycle Timing

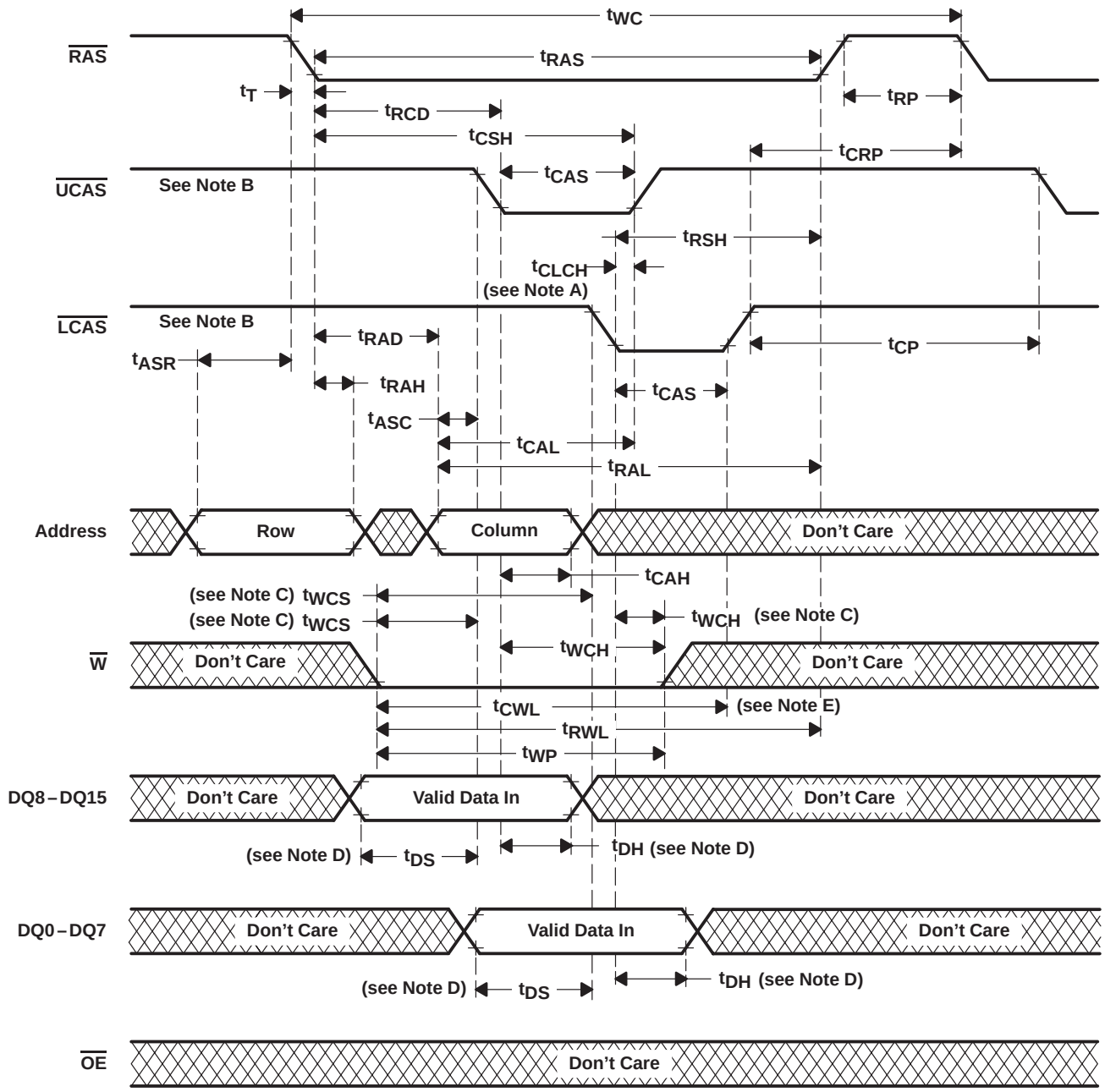
PARAMETER MEASUREMENT INFORMATION



NOTES: A. To hold the address latched by the first $\overline{\text{xCAS}}$ going low, the parameter t_{CLCH} must be met.
B. $\overline{\text{xCAS}}$ order is arbitrary.
C. t_{CWL} must be satisfied for each $\overline{\text{xCAS}}$ to write properly to each byte.

Figure 4. Write-Cycle Timing

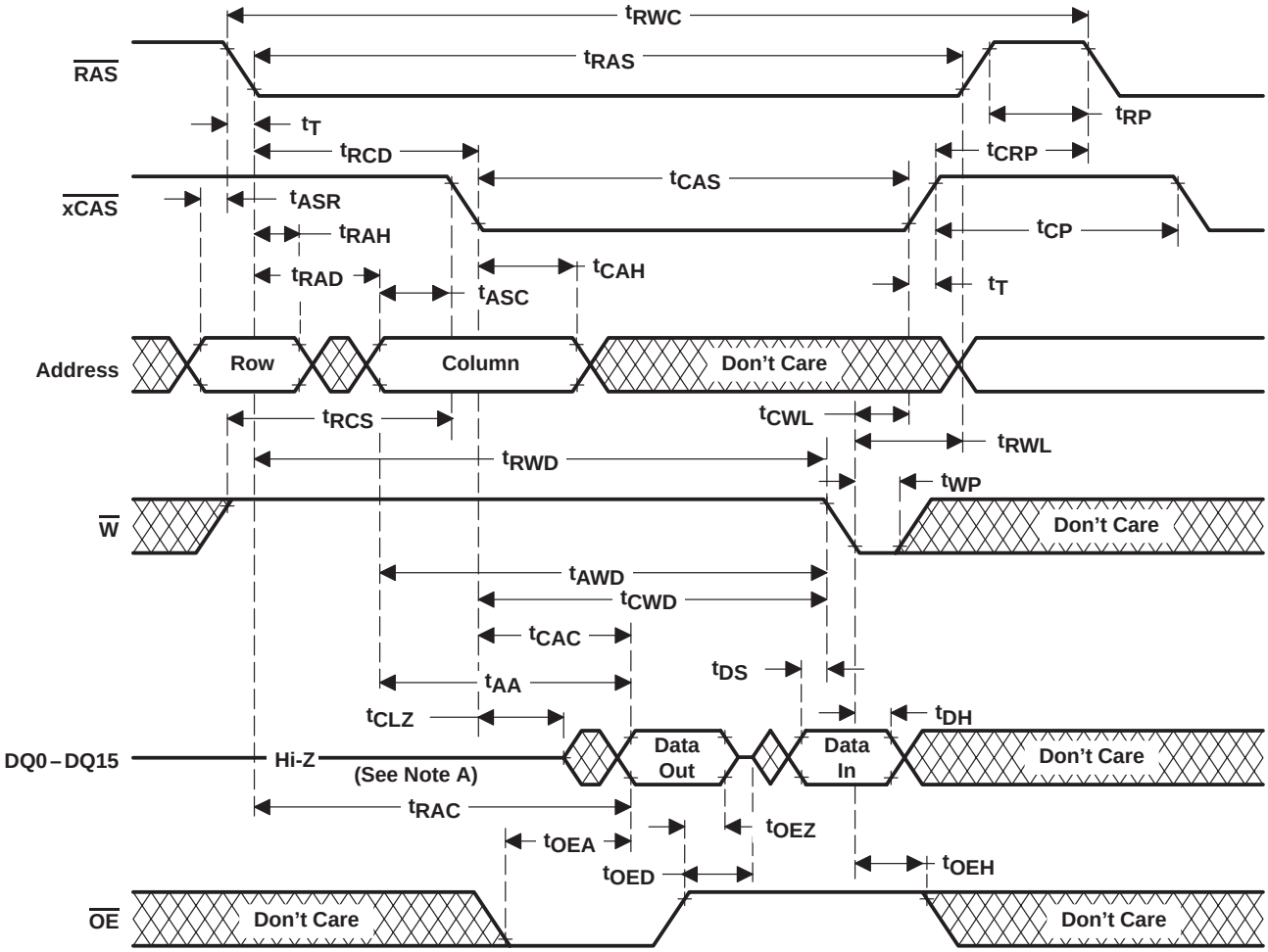
PARAMETER MEASUREMENT INFORMATION



NOTES: A. To hold the address latched by the first $\overline{\text{xCAS}}$ going low, the parameter t_{CLCH} must be met.
B. $\overline{\text{xCAS}}$ order is arbitrary.
C. t_{WCS} and t_{WCH} must be satisfied for each $\overline{\text{xCAS}}$.
D. t_{DS} and t_{DH} of a DQ input is referenced to the corresponding $\overline{\text{xCAS}}$.
E. t_{CWL} must be satisfied for each $\overline{\text{xCAS}}$ to properly write to each byte.

Figure 5. Early-Write-Cycle Timing

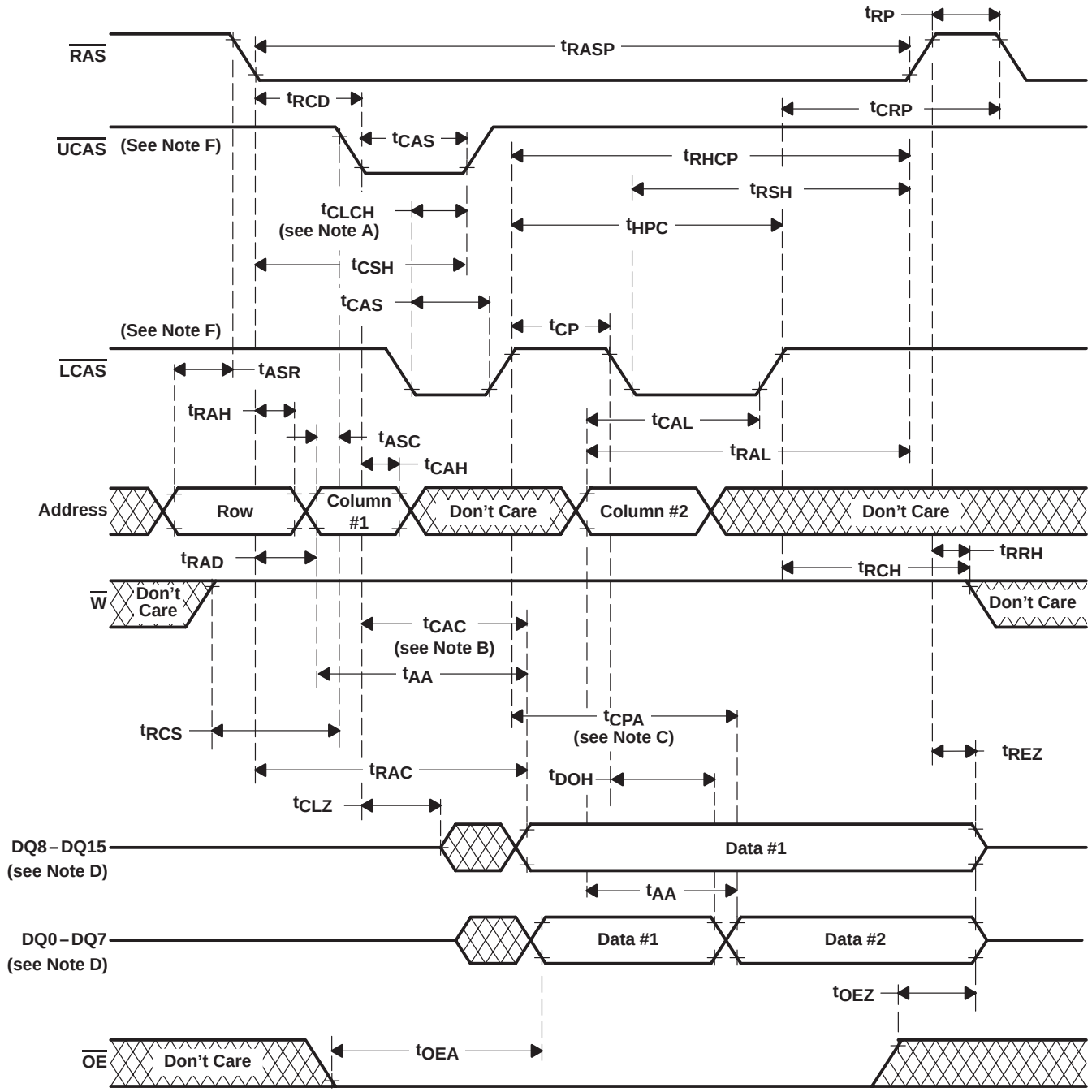
PARAMETER MEASUREMENT INFORMATION



NOTE A: Output can go from the high-impedance state to an invalid-data state prior to the specified access time.

Figure 6. Read-Write-Cycle Timing

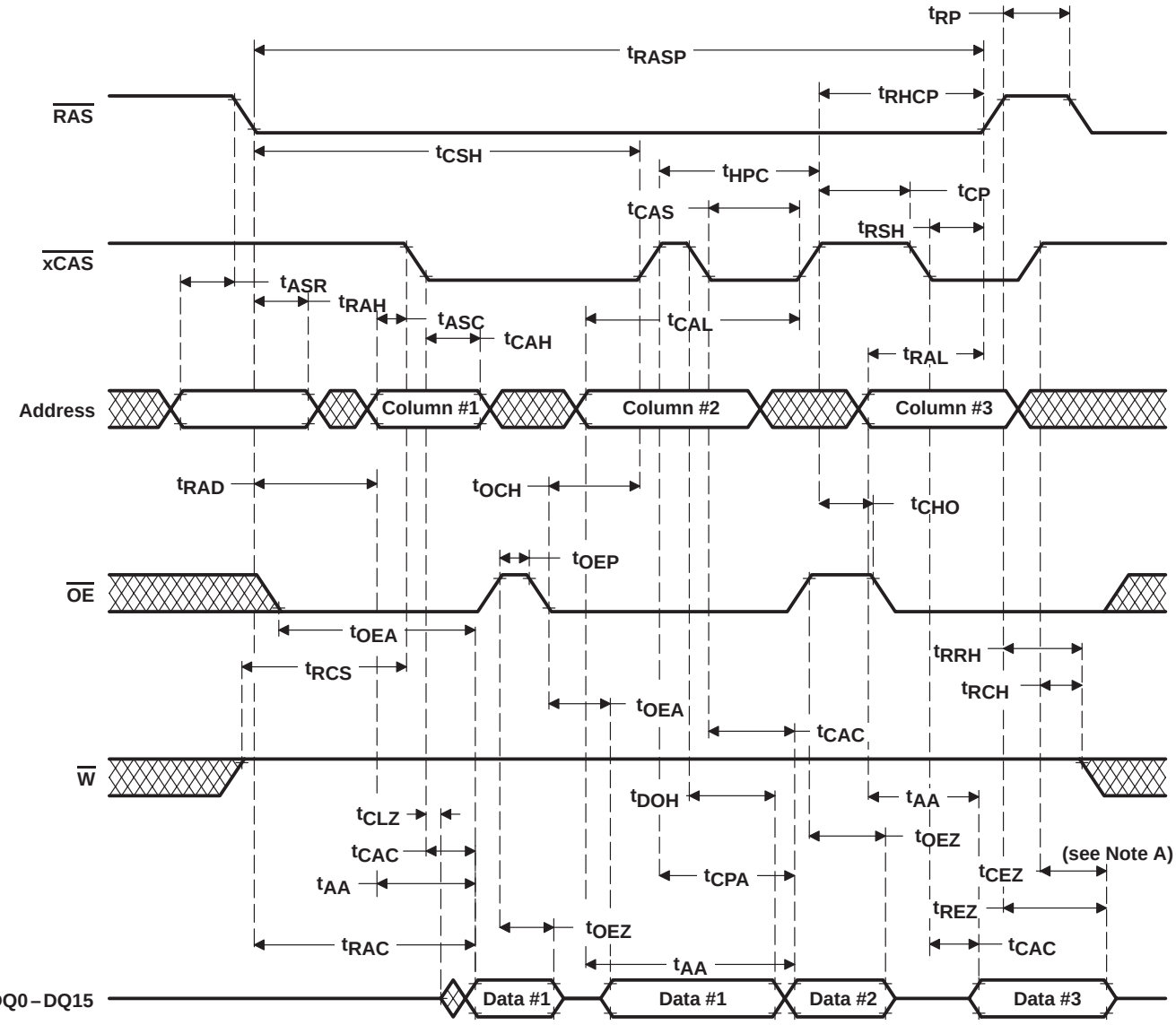
PARAMETER MEASUREMENT INFORMATION



NOTES: A. To hold the address latched by the first xCAS going low, the parameter t_{CLCH} must be met.
B. t_{CAC} is measured from xCAS to its corresponding DQx.
C. Access time is t_{CPA}-, t_{AA}-, or t_{CAC}-dependent.
D. Output can go from the high-impedance state to an invalid-data state prior to the specified access time.
E. A write cycle or read-modify-write cycle can be mixed with the read cycles as long as the write- and read-modify-write timing specifications are not violated.
F. xCAS order is arbitrary.

Figure 7. EDO Read-Cycle Timing (See Note E)

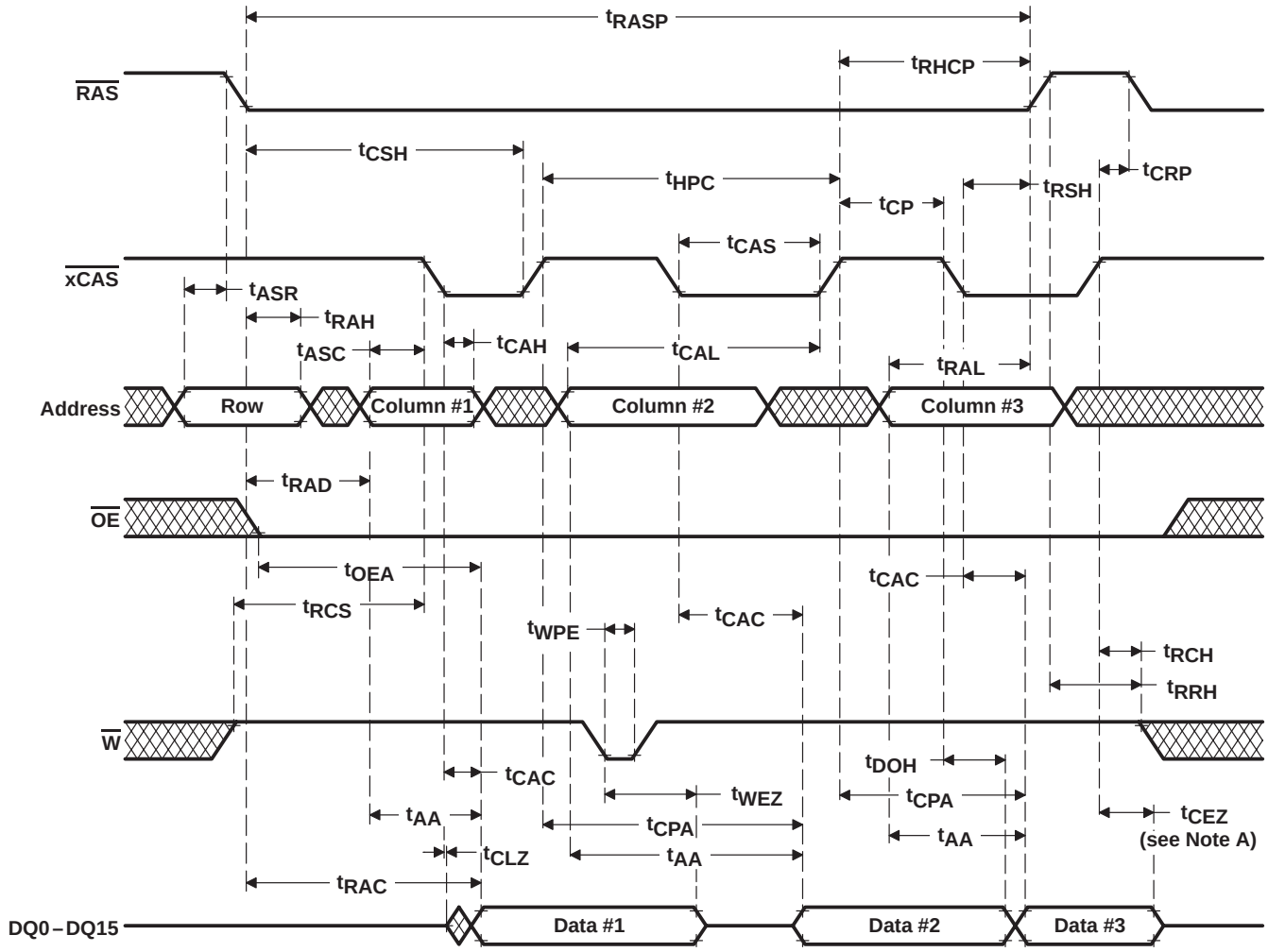
PARAMETER MEASUREMENT INFORMATION



NOTE A: Output is turned off by t_{CEZ} if $\overline{RAS}$ goes high during $\overline{xCAS}$ low.

Figure 8. EDO Read-Cycle Timing With $\overline{OE}$ Control

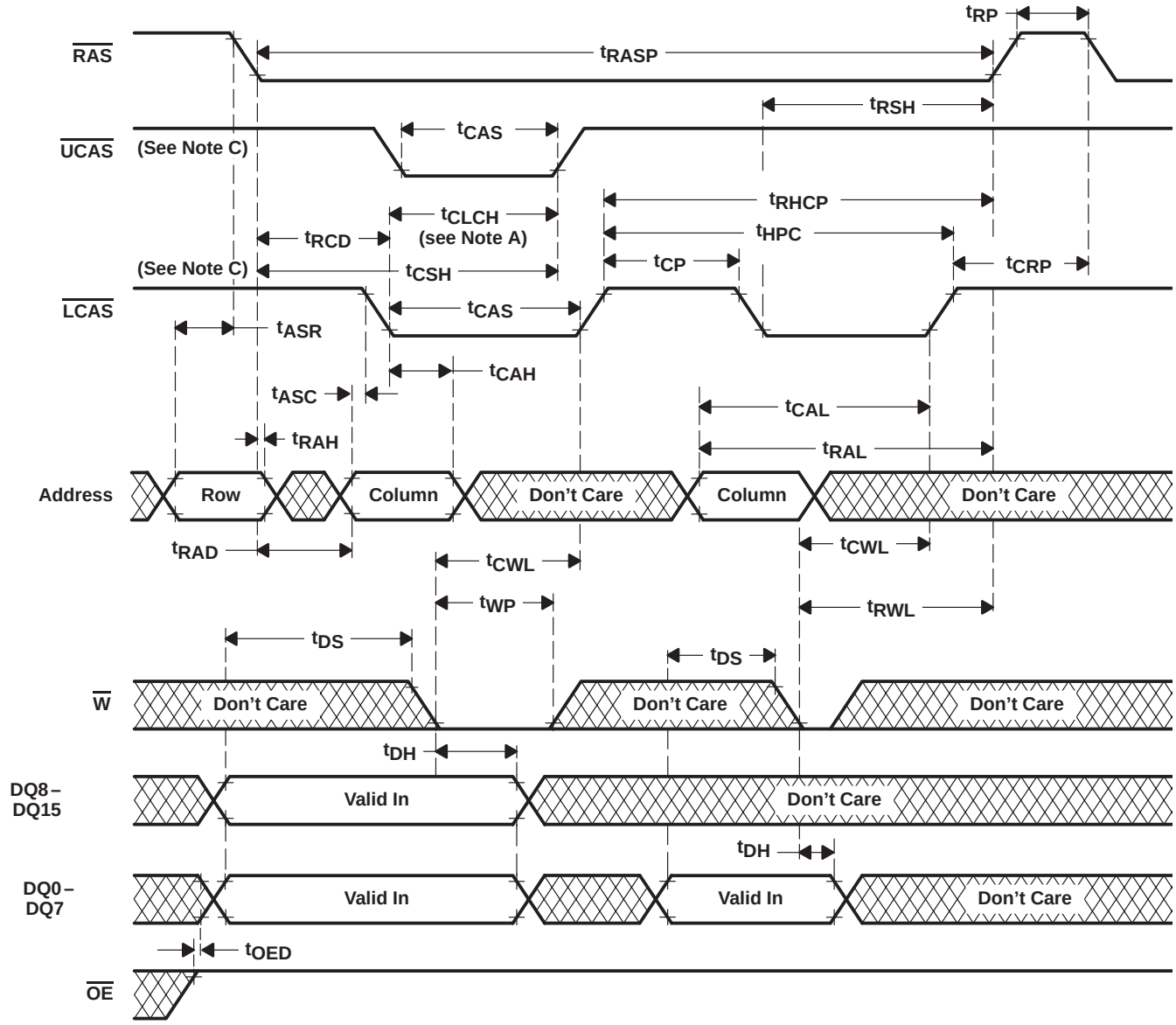
PARAMETER MEASUREMENT INFORMATION



NOTE A: Output is turned off by t_{CEZ} if $\overline{RAS}$ goes high during $\overline{xCAS}$ low.

Figure 9. EDO Read-Cycle Timing With $\overline{W}$ Control

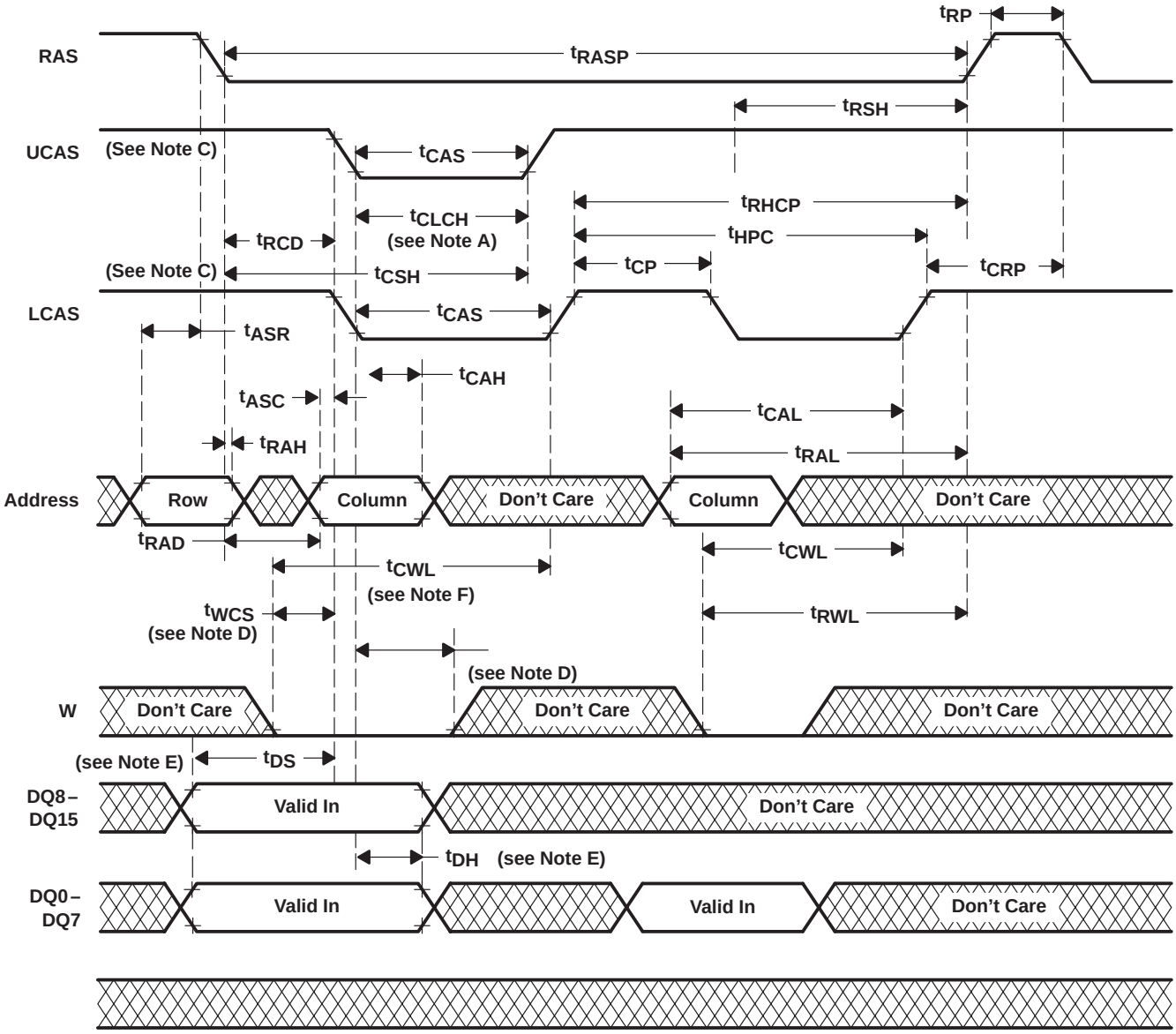
PARAMETER MEASUREMENT INFORMATION



NOTES: A. To hold the address latched by the first $\overline{\text{xCAS}}$ going low, the parameter t_{CLCH} must be met.
B. A read cycle or read-modify-write cycle can be mixed with the write cycles as long as the read- and read-modify-write timing specifications are not violated.
C. $\overline{\text{xCAS}}$ order is arbitrary.

Figure 10. EDO Write-Cycle Timing

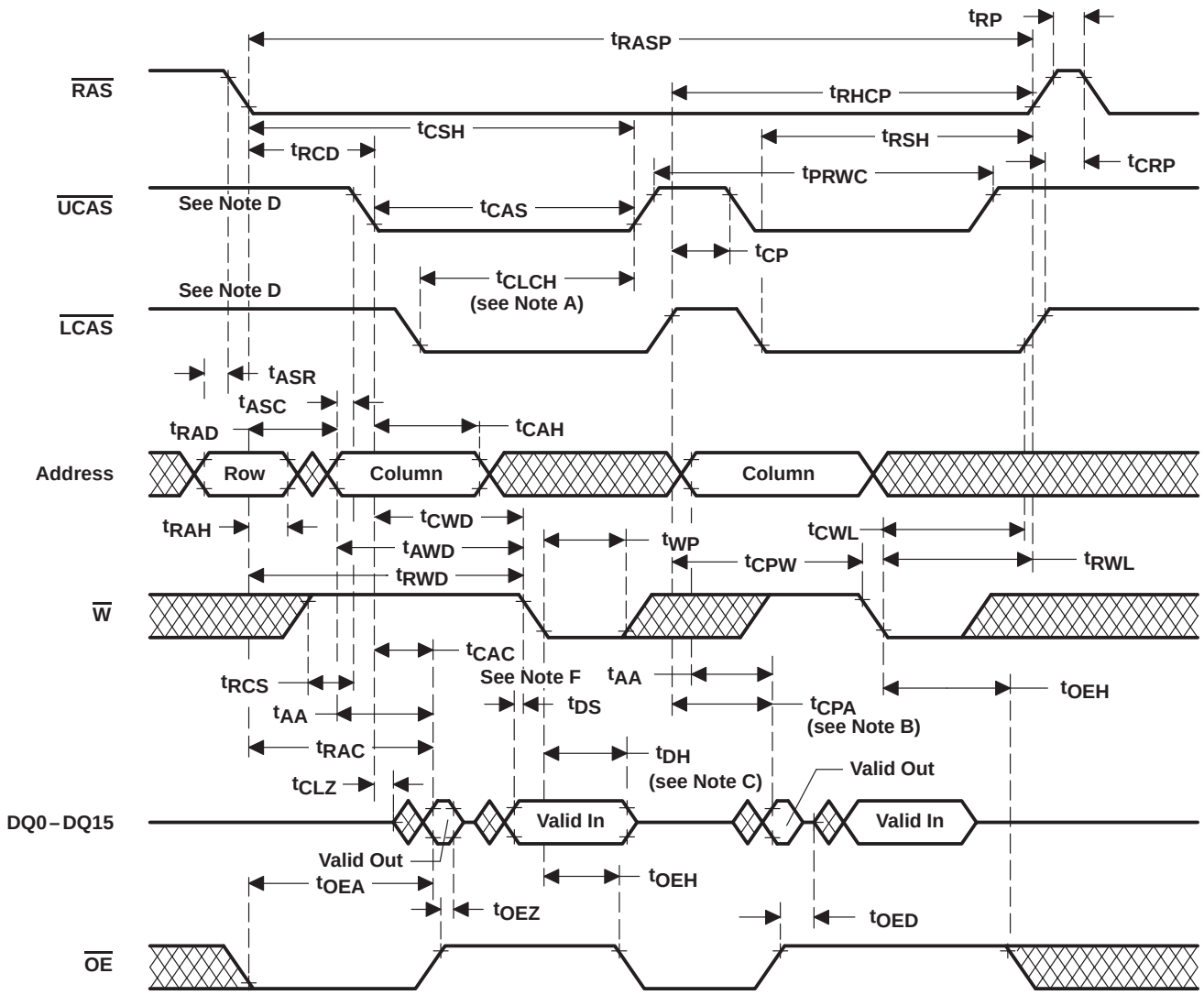
PARAMETER MEASUREMENT INFORMATION



NOTES: A. To hold the address latched by the first $\overline{\text{xCAS}}$ going low, the parameter t_{CLCH} must be met.
B. A read cycle or read-modify-write cycle can be mixed with the write cycles as long as the read- and read-modify-write timing specifications are not violated.
C. $\overline{\text{xCAS}}$ order is arbitrary.
D. t_{WCS} and t_{WCH} must be satisfied for each $\overline{\text{xCAS}}$ in an early-write cycle.
E. t_{DS} and t_{DH} of a DQ input are referenced to the corresponding $\overline{\text{xCAS}}$.
F. t_{CWL} must be satisfied for each $\overline{\text{xCAS}}$ to ensure proper writing to each byte.

Figure 11. EDO Early Write-Cycle Timing (See Note B)

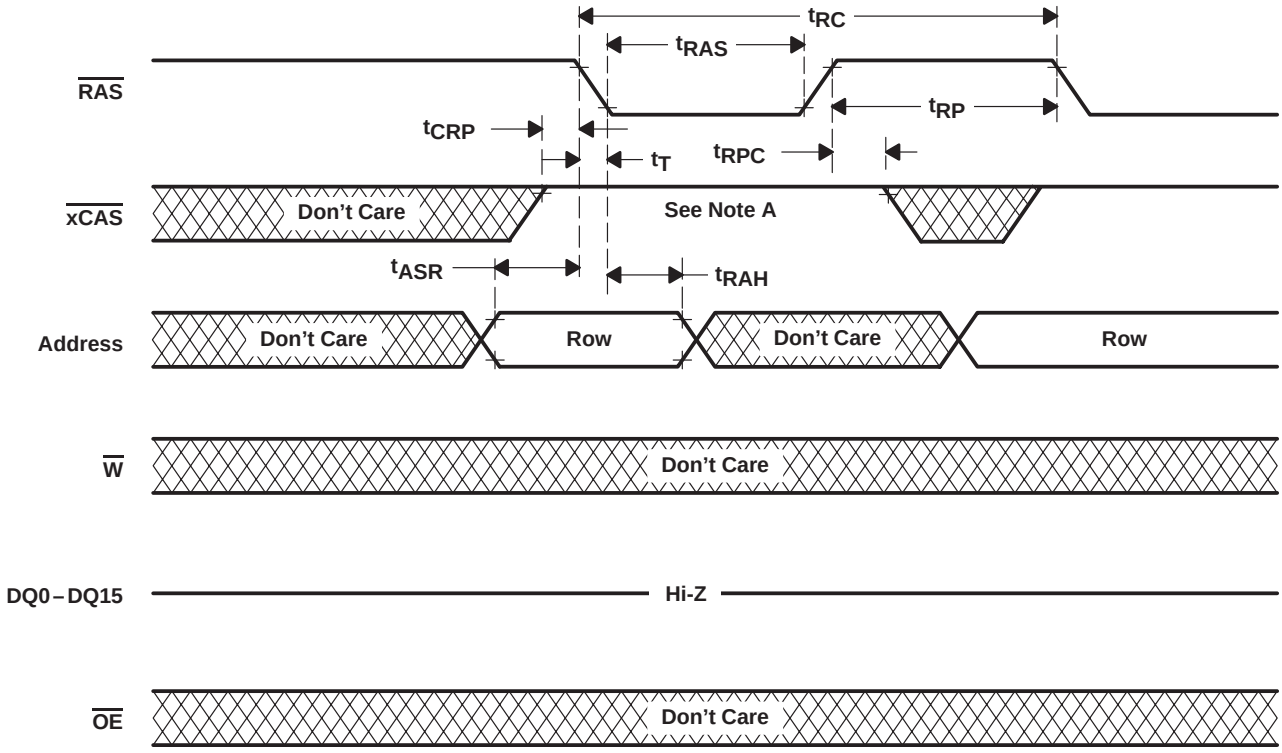
PARAMETER MEASUREMENT INFORMATION



NOTES: A. To hold the address latched by the first $\overline{\text{xCAS}}$ going low, the parameter t_{CLCH} must be met.
B. Access time is t_{CPA}-, t_{AA}-, or t_{CAC}-dependent.
C. Output can go from the high-impedance state to an invalid-data state prior to the specified access time.
D. $\overline{\text{xCAS}}$ order is arbitrary.
E. A read or write cycle can be intermixed with read-modify-write cycles as long as the read- and write-cycle timing specifications are not violated.
F. t_{CAC} is measured from $\overline{\text{xCAS}}$ to its corresponding DQx.

Figure 12. EDO Read-Modify-Write-Cycle Timing (See Note E)

PARAMETER MEASUREMENT INFORMATION



NOTE A: Both $\overline{\text{LCAS}}$ and $\overline{\text{UCAS}}$ must be high.

Figure 13. $\overline{\text{RAS}}$-Only Refresh-Cycle Timing

PARAMETER MEASUREMENT INFORMATION

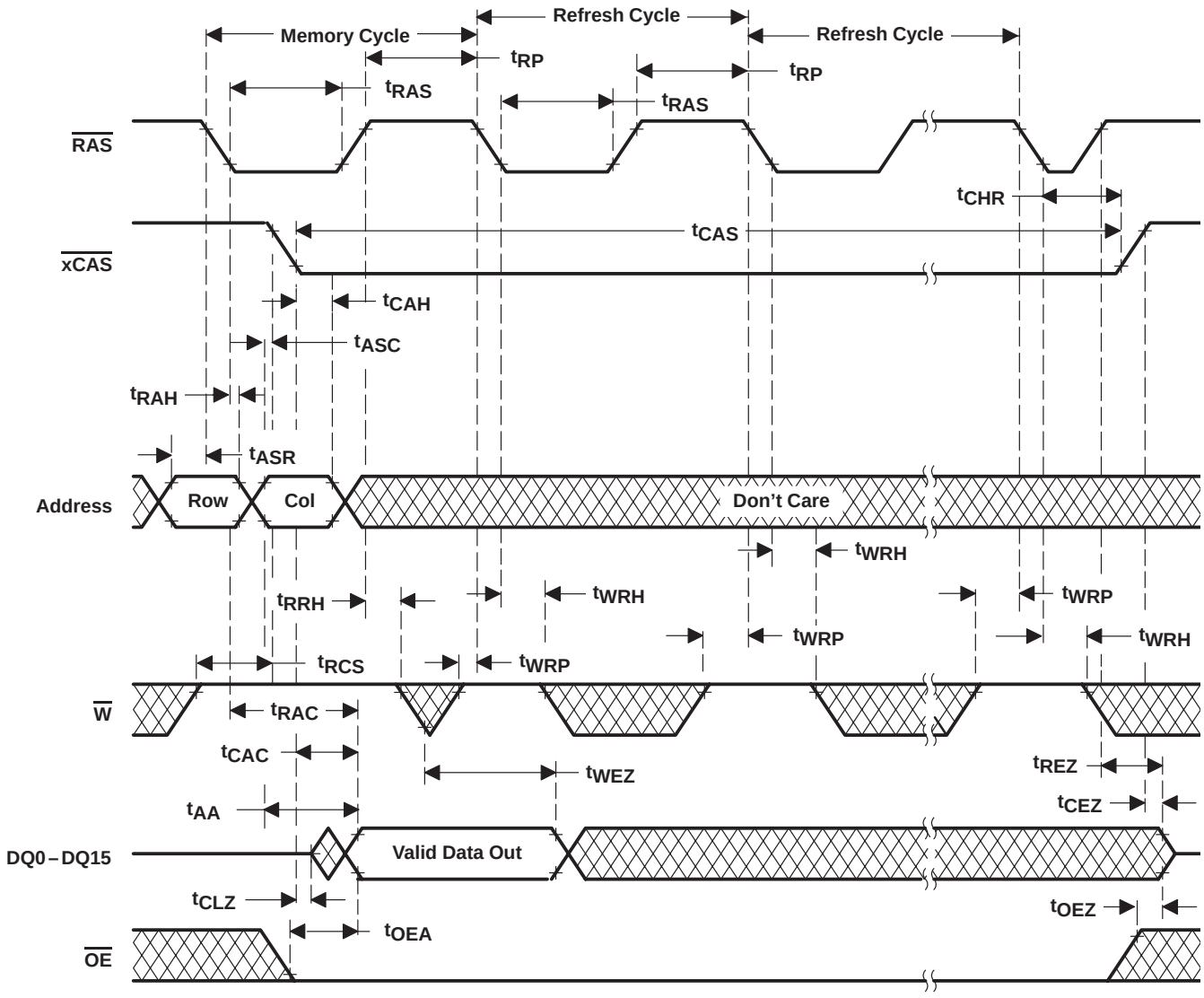


Figure 14. Hidden-Refresh-Cycle (Read) Timing

PARAMETER MEASUREMENT INFORMATION

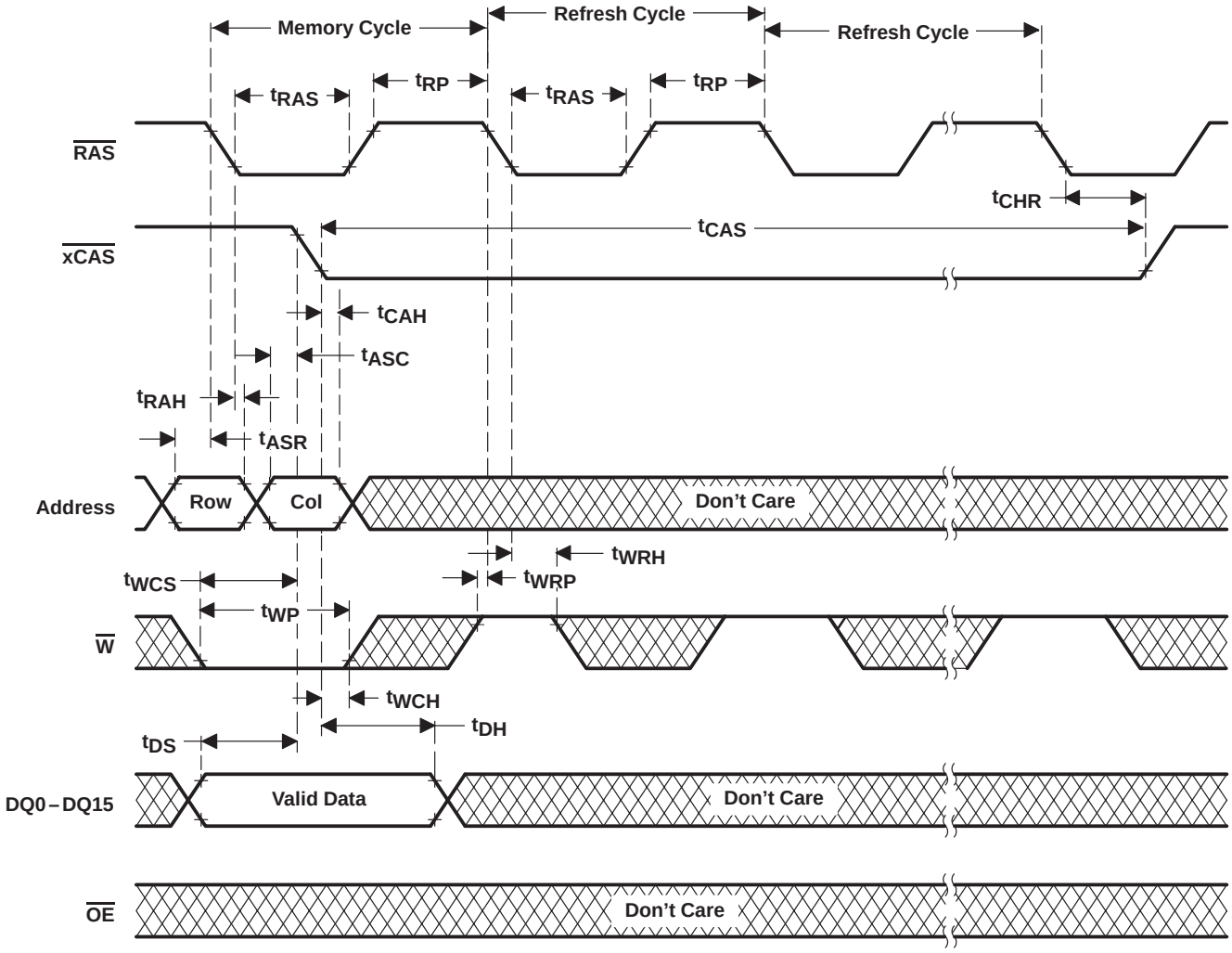
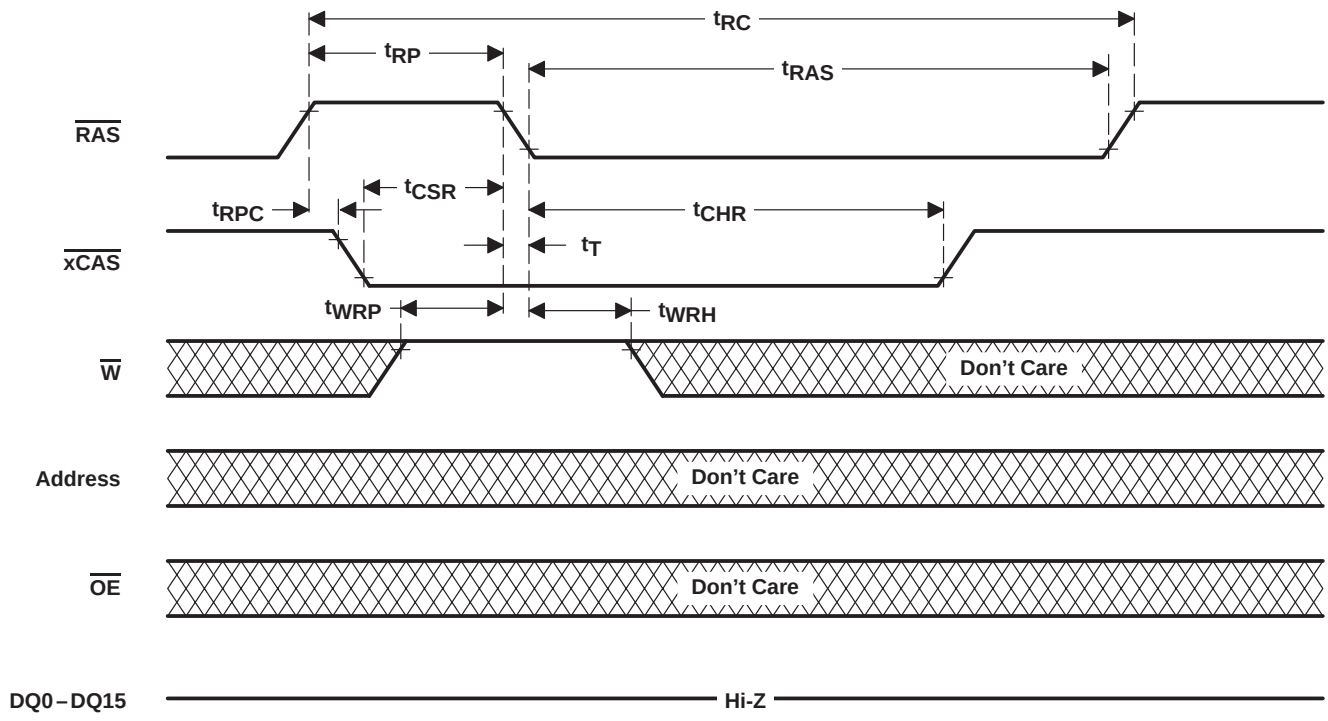


Figure 15. Hidden-Refresh Cycle (Write) Timing

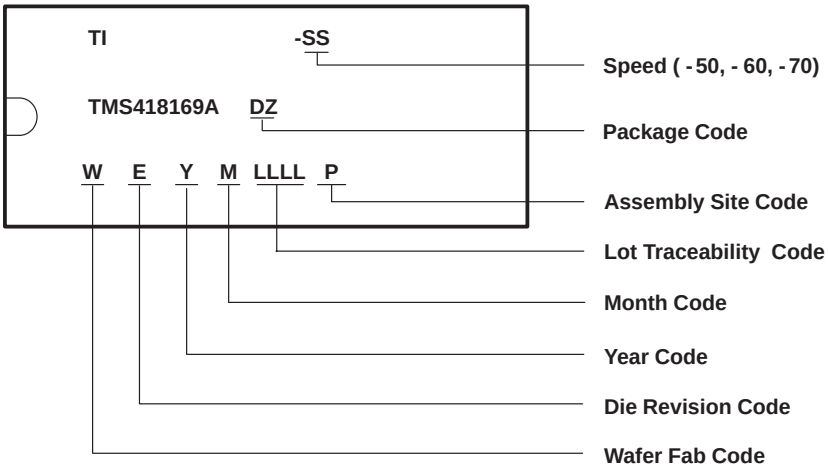
PARAMETER MEASUREMENT INFORMATION



NOTE A: Any $\overline{\text{xCAS}}$ can be used. If both $\overline{\text{UCAS}}$ and $\overline{\text{LCAS}}$ are used, both must satisfy t_{CSR} and t_{CHR}.

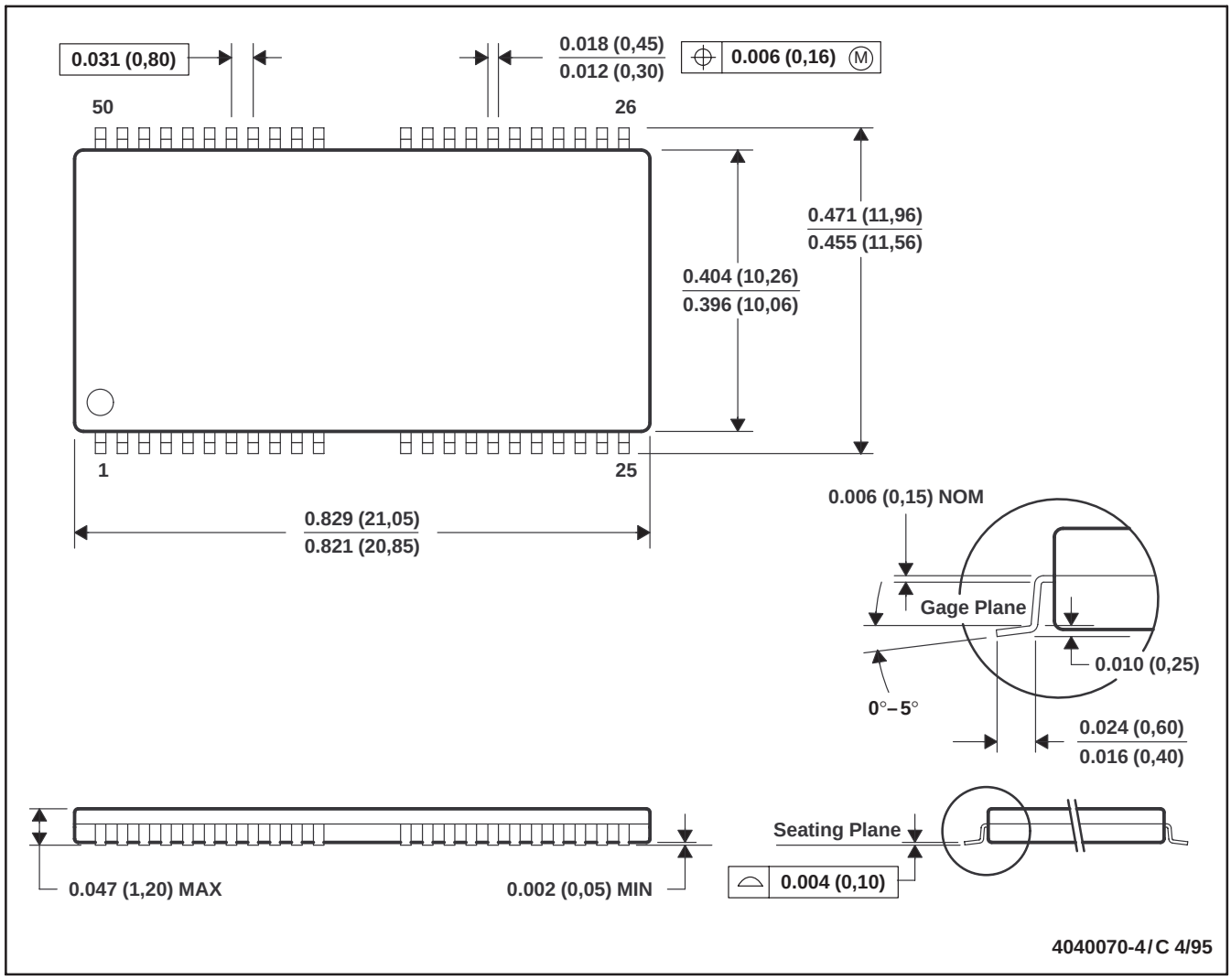
Figure 16. Automatic (xCBR) Refresh-Cycle Timing

device symbolization (TMS418169A illustrated)



MECHANICAL DATA

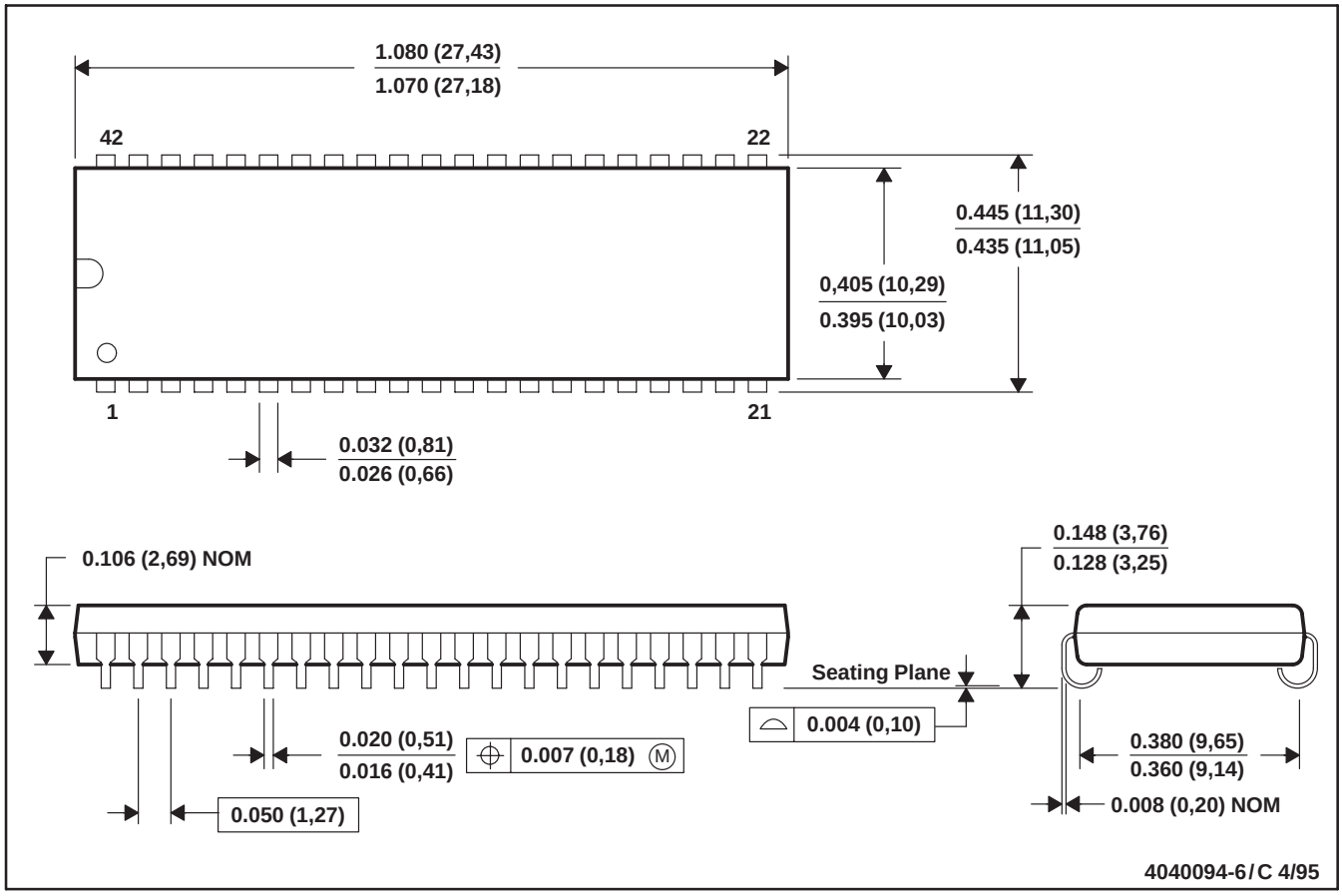
DGE (R-PDSO-G44/50) **PLASTIC SMALL-OUTLINE PACKAGE**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.

MECHANICAL DATA

DZ (R-PDSO-J42) **PLASTIC SMALL-OUTLINE J-LEAD PACKAGE**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Plastic body dimensions do not include mold protrusion. Maximum mold protrusion is 0.005 (0,125).

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