16,384 WORD×4 Bit CMOS Static RAM (With $\overline{OE}$)

FEATURES

- Fast Access Time: 12, 15, 20, 25ns (max.)
- Low Power Dissipation
  Standby (TTL) : 35mA (max.)
  (CMOS): 1mA (max.)
  100μA (max.) L-Version
- Operating KM6466BP/J-12: 140mA (max.)
  KM6466BP/J-15: 130mA (max.)
  KM6466BP/J-20: 120mA (max.)
  KM6466BP/J-25: 110mA (max.)
- Single 5V±10% Power Supply
- TTL Compatible Inputs and Outputs
- Fully Static Operation
  No clock or refresh required
- Three State Outputs
- Low Data Retention Voltage: 2V (min.)
- Standard 24-pin DIP (300 mil.), 24-pin SOJ (300 mil.)

GENERAL DESCRIPTION

The KM6466B/BL is a 65,536-bit high-speed Static Random Access Memory organized as 16,384 words by 4 bits.

The device is fabricated using Samsung's advanced CMOS process.

The KM6466B/BL has a chip select input for the minimum current power down mode.

The KM6466B/BL has been designed for high speed applications. It is particularly well suited for the use in high speed and low power applications in which battery back-up for nonvolatility is required.

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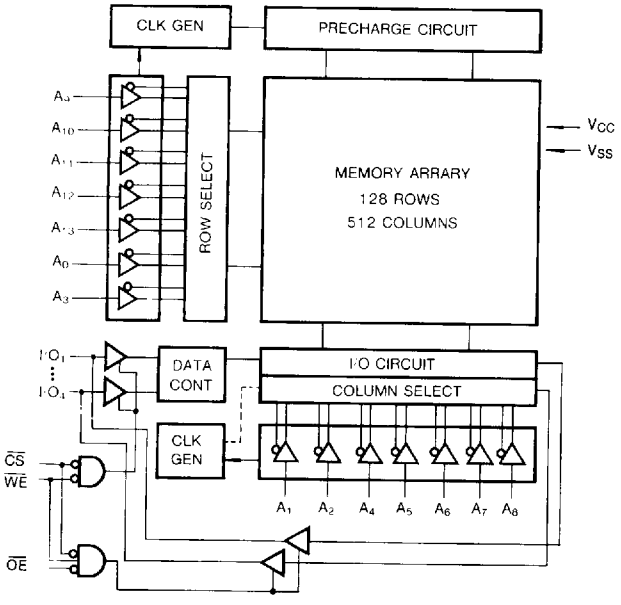
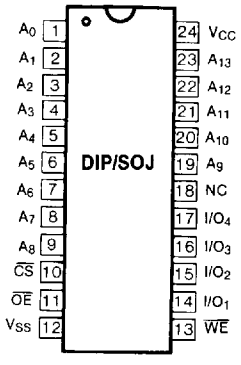
FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION (Top View)



Pin Name	Pin Function
A_0-A_{13}	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
I/O_1-I/O_4	Data Inputs/Outputs
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No Connection

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	−0.5 to 7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−0.5 to 7.0	V
Power Dissipation	P_D	1.0	W
Storage Temperature	T_{STG}	−65 to 150	°C
Operating Temperature	T_A	0 to 70	°C

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.5	V
Input Low Voltage	V_{IL}	−0.5*	—	0.8	V

* V_{IL}(min.) = −3.0V for ≤20ns pulse

DC AND OPERATING CHARACTERISTICS

(T_A = 0 to 70°C, V_{CC} = 5V ± 10%, unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Typ*	Max	Unit
Input Leakage Current	I_{LI}	V_{IN} = V_{SS} to V_{CC}		—	—	1	μA
Output Leakage Current	I_{LO}	$\overline{CS}$ = V_{IH}, $\overline{WE}$ = V_{IL}, $V_{I/O}$ = V_{SS} to V_{CC}, V_{CC} = Max		—	—	1	μA
Average Operating Current	I_{CC}	Min Cycle, 100% Duty, $\overline{CS}$ = V_{IL}, I_{OUT} = 0mA	12ns	—	110	140	mA
			15ns	—	95	130	mA
			20ns	—	85	120	mA
			25ns	—	75	110	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}$ = V_{IH}		—	15	35	mA
	I_{SB1}	$\overline{CS}$ ≥ V_{CC} − 0.2V		—	—	1	mA
		V_{IN} ≥ V_{CC} − 0.2 V or V_{IN} ≤ 0.2V	L		2	100	μA
Output Low Voltage	V_{OL}	I_{OL} = 8.0mA		—	—	0.4	V
Output High Voltage	V_{OH}	I_{OH} = −4.0mA		2.4	—	—	V

* Typ: V_{CC} = 5V, T_A = 25°C

CAPACITANCE ($f = 1MHz$, $T_A = 25°C$)

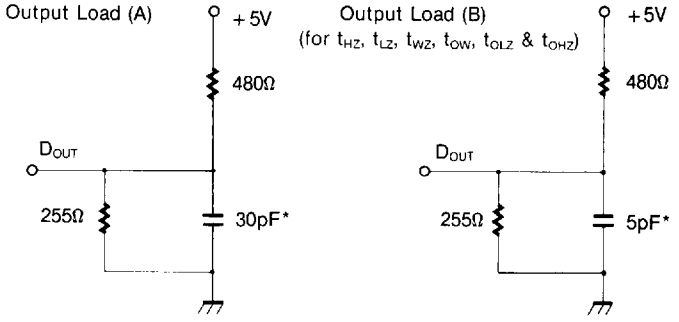
Item	Symbol	Test Conditions	Min	Max	Unit
Input Capacitance	C_{IN}	$V_{IN} = 0V$	—	7	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O} = 0V$	—	7	pF

Note: Capacitance is sampled and not 100% tested.

AC CHARACTERISTICS

TEST CONDITIONS ($T_A = 0$ to $70°C$, $V_{CC} = 5V \pm 10\%$, unless otherwise specified)

Parameter	Value
Input Pulse Level	0 to 3V
Input Rise and Fall Times	3ns
Input and Output Timing Reference Levels	1.5V
Output Loads	See below



* Including Scope and Jig Capacitance

READ CYCLE

Parameter	Symbol	KM6466BP-12 KM6466BJ-12		KM6466BP-15 KM6466BJ-15		KM6466BP-20 KM6466BJ-20		KM6466BP-25 KM6466BJ-25		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	12		15		20		25		ns
Address Access Time	t_{AA}		12		15		20		25	ns
Chip Select to Output	t_{CO}		12		15		20		25	ns
Output Enable to Valid Output	t_{OE}		7		8		9		10	ns
Chip Select to Low-Z Output	t_{LZ}	3		3		3		3		ns
Output Enable to Low-Z Output	t_{OLZ}	0		0		0		0		ns
Chip Disable to High-Z Output	t_{HZ}	0	7	0	8	0	9	0	10	ns
Output Disable to High-Z Output	t_{OHZ}	0	6	0	7	0	8	0	9	ns
Output Hold from Address Change	t_{OH}	3		3		3		3		ns
Chip Selection to Power Up Time	t_{PU}	0		0		0		0		ns
Chip Selection to Power Down Time	t_{PD}		12		15		20		25	ns

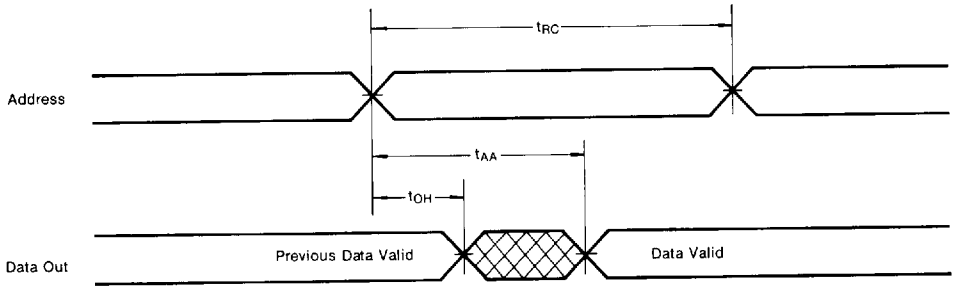
WRITE CYCLE

Parameter	Symbol	KM6466BP-12 KM6466BJ-12		KM6466BP-15 KM6466BJ-15		KM6466BP-20 KM6466BJ-20		KM6466BP-25 KM6466BJ-25		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	12		15		20		25		ns
Chip Select to End of Write	t_{CW}	10		12		13		15		ns
Address Set-up Time	t_{AS}	0		0		0		0		ns
Address Valid to End of Write	t_{AW}	10		12		13		15		ns
Write Pulse Width	t_{WP}	10		12		13		15		ns
Write Recovery Time	t_{WR}	0		0		0		0		ns
Write to Output High-Z	t_{WZ}	0	7	0	8	0	9	0	10	ns
Data to Write Time Overlap	t_{DW}	8		9		10		10		ns
Data Hold from Write Time	t_{DH}	0		0		0		0		ns
End Write to Output Low-Z	t_{OW}	0		0		0		0		ns

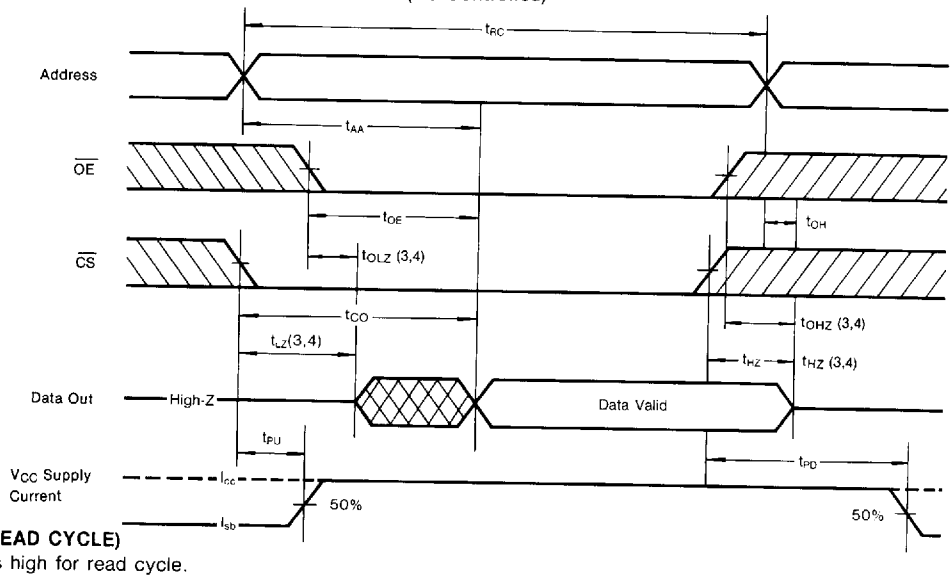
TIMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE (Address Controlled)

($\overline{CS} = V_{IL}$, $\overline{WE} = V_{IH}$, $\overline{OE} = V_{IL}$)



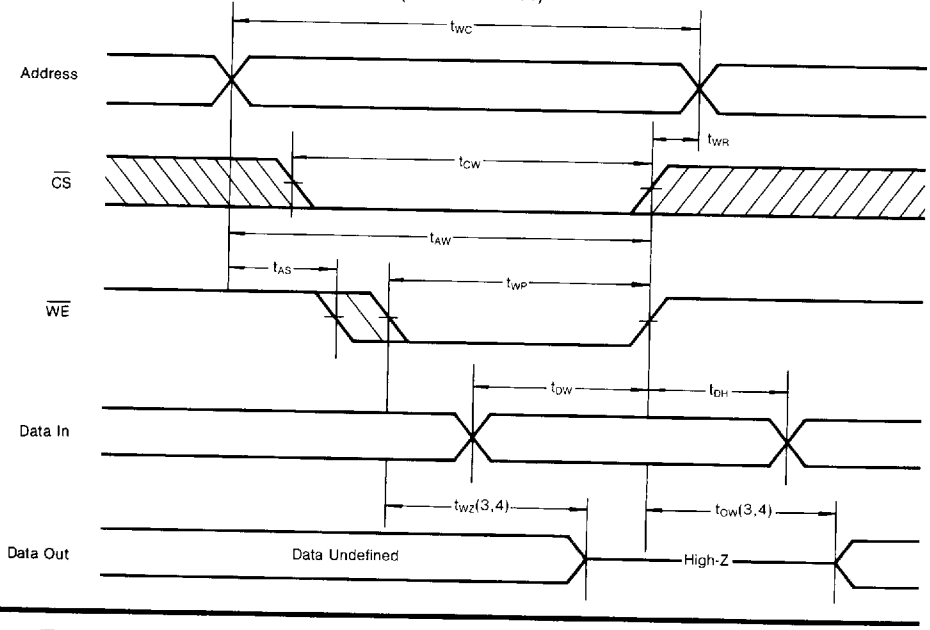
TIMING WAVEFORM OF READ CYCLE ($\overline{CS}$ Controlled)



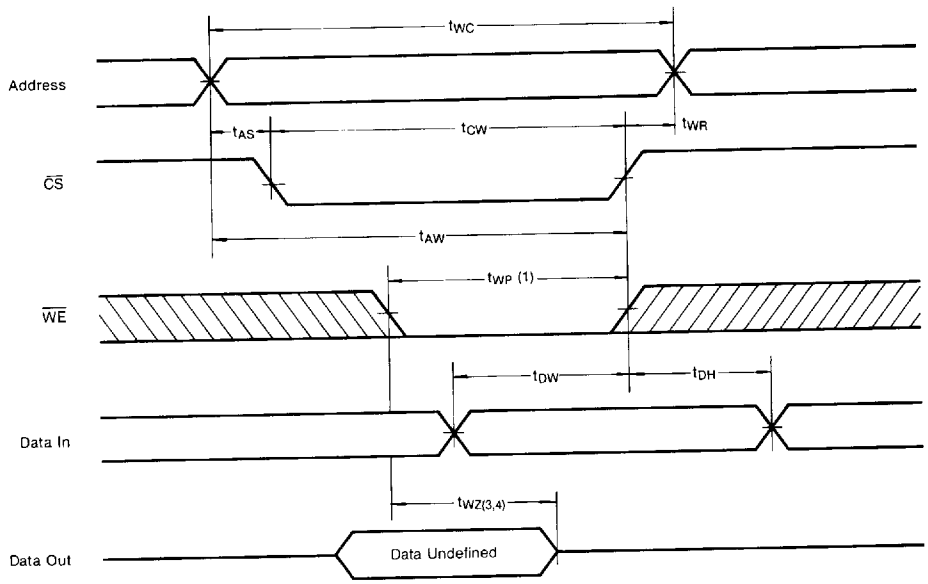
Notes (READ CYCLE)

1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. At any given temperature and voltage condition, t_{HZ}(max.) is less than t_{LZ}(min.) both for a given device and from device to device.
4. Transition is measured ±200mV from steady state voltage with Load (B). This parameter is sampled and not 100% tested.
5. Device is continuously selected with $\overline{CS}$=V_{IL}.
6. Address valid prior to or coincident with $\overline{CS}$ transition low.

TIMING WAVEFORM OF WRITE CYCLE ($\overline{WE}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE ($\overline{CS}$ Controlled)



Notes (WRITE CYCLE)

1. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and low $\overline{WE}$.
2. All write cycle timing is referenced from the last valid address to the first transition address.
3. Transition is measured ±200mV from steady state voltage with Load(B).
4. This parameter is sampled and not 100% tested.
5. At any given temperature and voltage condition, t_{WZ} (max.) is less than t_{OW} (min.) both for a given device and from device to device.
6. $\overline{CS}$ or $\overline{WE}$ must be in high during address transition.
7. $\overline{OE}$ is high for write cycle.

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	I/O Pin	Supply Current	Mode
H	X	X	High-Z	I_{SB}, I_{SB1}	Not Select
L	H	L	D_{OUT}	I_{CC}	Read
L	L	X	D_{IN}	I_{CC}	Write

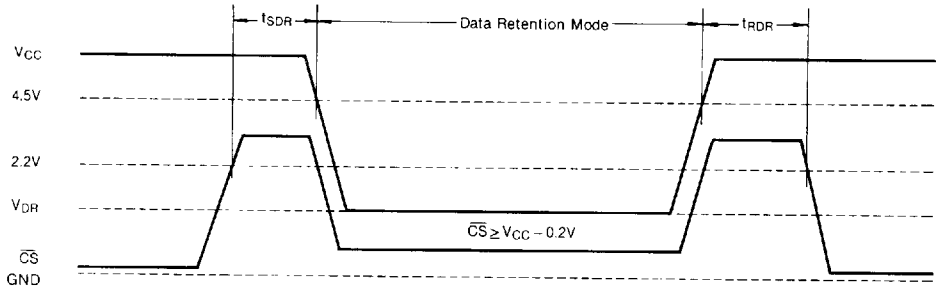
* Note: X means Don't Care.

DATA RETENTION CHARACTERISTICS (T_A = 0 to 70°C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
V_{CC} for Data Retention	V_{DR}	$\overline{CS} \geq V_{CC} - 0.2V$	2		5.5	V
Data Retention Current	I_{DR}	$V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$		1	50*	μA
Data Retention Set-up Time	t_{SDR}	See Data Retention Waveforms (below)	0			ns
Recovery Time	t_{RDR}		t_{RC}**			ns

*: V_{CC} = 3V
**: t_{RC} = Read Cycle Time

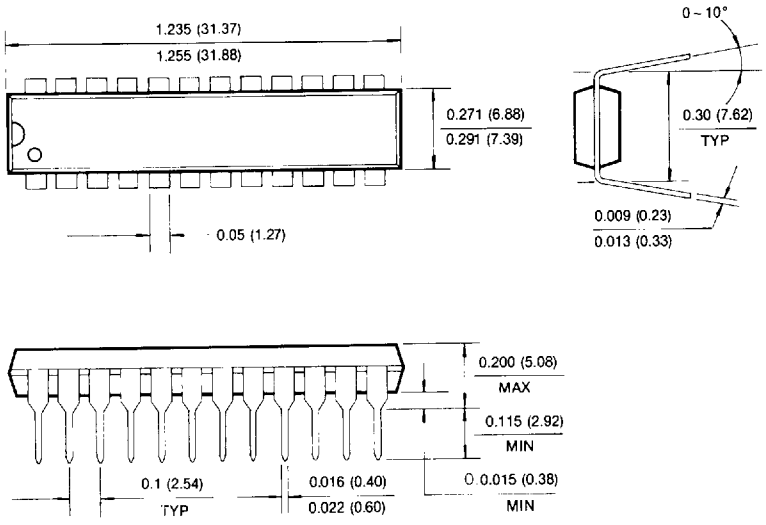
DATA RETENTION WAVEFORM



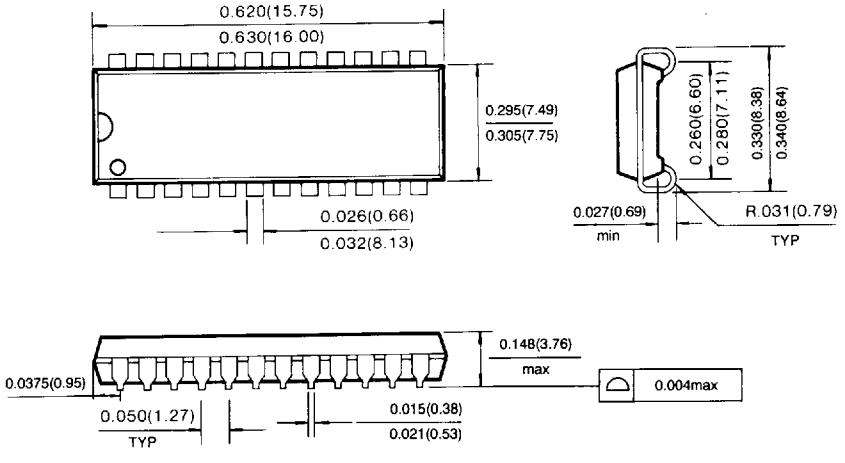
PACKAGE DIMENSIONS

24 PIN PLASTIC DUAL IN LINE PACKAGE

Unit: Inches (millimeters)



24 PIN SMALL OUT LINE J FORM PACKAGE (300mil)



*Note: Do not include mold protrusion

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