SGS-THOMSON MICROELECTRONICS

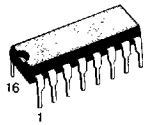
S G S-THOMSON

M54HC175
M74HC175

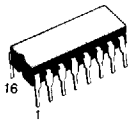
T-46-07-09

QUAD D-TYPE FLIP-FLOP WITH CLEAR

- HIGH SPEED
  t_{PD} = 18 ns (TYP.) at V_{CC} = 5V
- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) at T_A = 25°C
- HIGH NOISE IMMUNITY
  V_{NIH} = V_{NIL} = 28% V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}|$ = I_{OL} = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  t_{PLH} = t_{PHL}
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS175



B1N
Plastic Package



F1
Ceramic Frit Seal Package

M1
Micro Package

C1
Plastic Chip Carrier

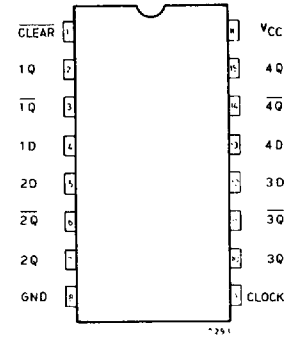
ORDERING NUMBERS:

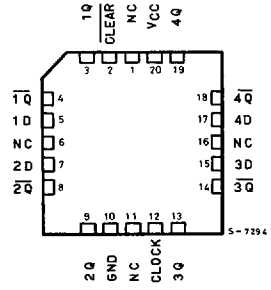
M54HC175 F1
M74HC175 B1N
M74HC175 F1
M74HC175 C1
M74HC175 M1

DESCRIPTION

The M54/74HC175 is a high speed CMOS QUAD D-TYPE FLIP-FLOP WITH CLEAR fabricated in silicon gate CMOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption.
These four flip-flops are controlled by a clock input (CLOCK) and a clear input (CLEAR). The information data applied to the D inputs (1D to 4D) are transfered to the outputs (1Q to 4Q and $\overline{1Q}$ to $\overline{4Q}$) on the positive-going edge of the clock pulse. The reset function is accomplished when the clear input is taken low and all Q outputs are kept low regardless of other input conditions. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

PIN CONNECTIONS (top view)





NC = No Internal Connection

TRUTH TABLE

INPUTS			OUTPUTS		FUNCTION
CLEAR	D	CLOCK	Q	$\overline{Q}$	
L	X	X	L	H	CLEAR
H	L	↑	L	H	—
H	H	↑	H	L	—
H	X	↓	Qn	$\overline{Qn}$	NO CHANGE

X: DON'T CARE

LOGIC DIAGRAM

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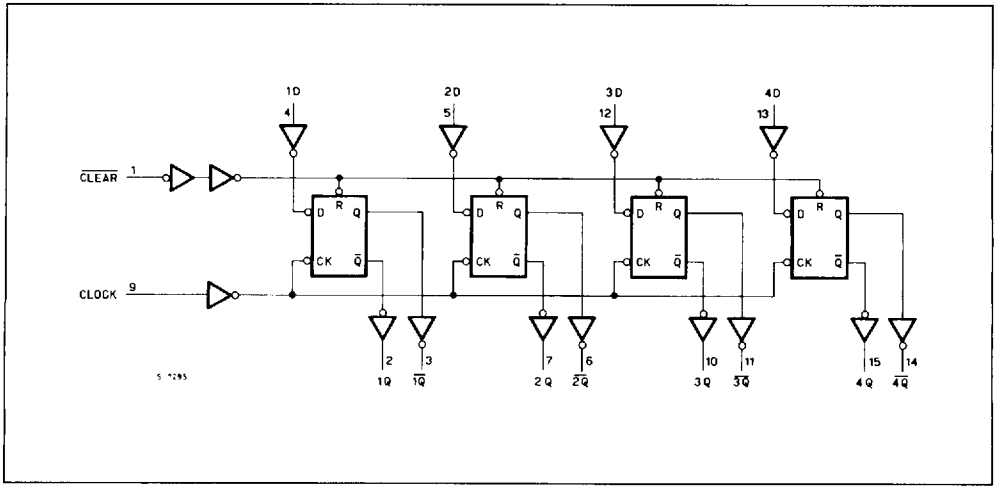

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	DC Input Voltage	−0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	−65 to 150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≅ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value		Unit
V_{CC}	Supply Voltage	2 to 6		V
V_I	Input Voltage	0 to V_{CC}		V
V_O	Output Voltage	0 to V_{CC}		V
T_A	Operating Temperature 74HC Series 54HC Series	−40 to 85 −55 to 125		°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5V	0 to 500	
		V_{CC} = 6 V	0 to 400	

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DC SPECIFICATIONS

Symbol	Parameter	V_{CC}	Test Condition		$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5	—	—	1.5	—	1.5	—	V
		4.5			3.15	—	—	3.15	—	3.15	—	
		6.0			4.2	—	—	4.2	—	4.2	—	
V_{IL}	Low Level Input Voltage	2.0			—	—	0.5	—	0.5	—	0.5	V
		4.5			—	—	1.35	—	1.35	—	1.35	
		6.0			—	—	1.8	—	1.8	—	1.8	
V_{OH}	High Level Output Voltage	2.0	V_I	I_O	1.9	2.0	—	1.9	—	1.9	—	V
		4.5	V_{IH} or V_{IL}	−20 μA	4.4	4.5	—	4.4	—	4.4	—	
		6.0			5.9	6.0	—	5.9	—	5.9	—	
		4.5		−4.0 mA	4.18	4.31	—	4.13	—	4.10	—	
		6.0		−5.2 mA	5.68	5.8	—	5.63	—	5.60	—	
V_{OL}	Low Level Output Voltage	2.0	V_{IH} or V_{IL}	20 μA	—	0.0	0.1	—	0.1	—	0.1	V
		4.5			—	0.0	0.1	—	0.1	—	0.1	
		6.0			—	0.0	0.1	—	0.1	—	0.1	
		4.5		4.0 mA	—	0.17	0.26	—	0.33	—	0.40	
		6.0		5.2 mA	—	0.18	0.26	—	0.33	—	0.40	
I_I	Input Leakage Current	6.0	$V_I = V_{CC}$ or GND		—	—	±0.1	—	±1.0	—	±1.0	μA
I_{CC}	Quiescent Supply Current	6.0	$V_I = V_{CC}$ or GND		—	—	4	—	40	—	80	μA

AC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5V$, $T_A = 25°C$, $C_L = 15pF$, Input $t_r = t_f = 6ns$)

Symbol	Parameter	54HC and 74HC			Unit
		Min.	Typ.	Max.	
t_{TLH} t_{THL}	Output Transition Time		4	8	ns
t_{PLH} t_{PHL}	Propagation Delay Time (CLOCK-Q, $\overline{Q}$)		18	28	ns
t_{PHL}	Propagation Delay Time ($\overline{CLEAR}$-Q, $\overline{Q}$)		20	32	ns
f_{MAX}	Maximum Clock Frequency	33	53		MHz

AC ELECTRICAL CHARACTERISTICS ($C_L = 50pF$, Input $t_r = t_f = 6ns$)

Symbol	Parameter	V_{CC}	Test Condition	T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0		—	30	75	—	95	—	110	ns
		4.5		—	8	15	—	19	—	22	
		6.0		—	7	13	—	16	—	19	
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{CLOCK}$-Q, $\overline{Q}$)	2.0		—	105	165	—	205	—	250	ns
		4.5		—	21	33	—	41	—	50	
		6.0		—	18	28	—	35	—	43	
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{CLEAR}$-Q, $\overline{Q}$)	2.0		—	115	185	—	230	—	280	ns
		4.5		—	23	37	—	46	—	56	
		6.0		—	20	31	—	39	—	48	
f_{MAX}	Maximum Clock Frequency	2.0		6	12	—	4.8	—	4	—	MHz
		4.5		30	48	—	24	—	20	—	
		6.0		35	56	—	28	—	24	—	
$t_{W(H)}$ $t_{W(L)}$	Minimum Pulse Width ($\overline{CLOCK}$)	2.0		—	30	75	—	95	—	110	ns
		4.5		—	8	15	—	19	—	22	
		6.0		—	7	13	—	16	—	19	
$t_{W(L)}$	Minimum Pulse Width $\overline{CLEAR}$	2.0		—	30	75	—	95	—	110	ns
		4.5		—	8	15	—	19	—	22	
		6.0		—	7	13	—	16	—	19	
t_s	Minimum Set-up Time	2.0		—	10	50	—	65	—	75	ns
		4.5		—	3	10	—	13	—	15	
		6.0		—	3	9	—	11	—	13	
t_h	Minimum Hold Time	2.0		—	—	0	—	0	—	0	ns
		4.5		—	—	0	—	0	—	0	
		6.0		—	—	0	—	0	—	0	
t_{REM}	Minimum Removal Time ($\overline{CLEAR}$)	2.0		—	0	75	—	95	—	110	ns
		4.5		—	0	15	—	19	—	22	
		6.0		—	0	13	—	16	—	19	
C_{IN}	Input Capacitance			—	5	10	—	10	—	10	pF
C_{PD} (*)	Power Dissipation Capacitance			—	71	—	—	—	—	—	pF

Note (*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the following equation.
$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4$ (for Flip/Flop).

And the total C_{PD} at the time when n pcs of Flip-Flop operate can be gained C_{PD} (total) = $43 + 28 \times n$

SWITCHING CHARACTERISTICS TEST WAVEFORM

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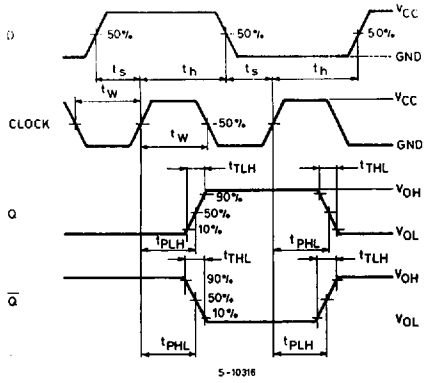

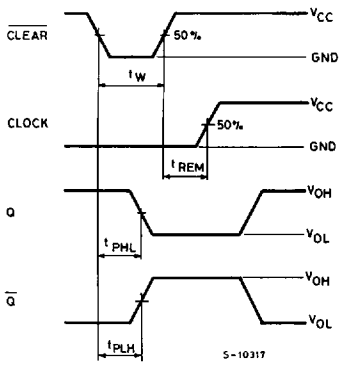

TEST CIRCUIT I_{CC} (Opr.)