



Integrated Device Technology, Inc.

# FAST CMOS 8-INPUT UNIVERSAL SHIFT REGISTER

IDT54/74/FCT299  
IDT54/74/FCT299A

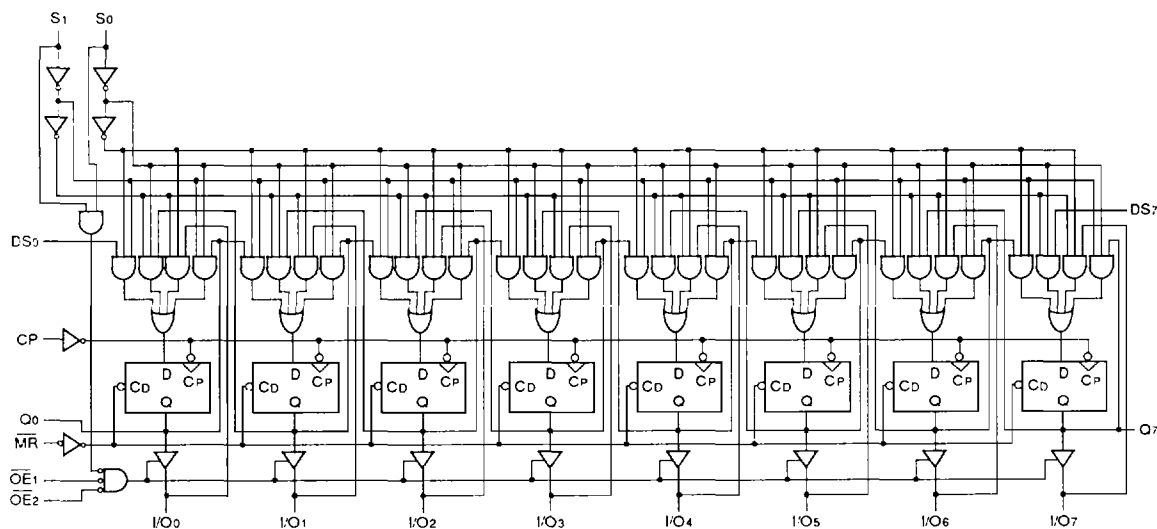
## FEATURES:

- IDT54/74FCT299 equivalent to FAST™ speed
- IDT54/74FCT299A 25% faster than FAST™
- Equivalent to FAST™ output drive over full temperature and voltage supply extremes
- IOL = 48mA (commercial) and 32mA (military)
- CMOS power levels (1mW typ. static)
- TTL input and output level compatible
- CMOS output level compatible
- Substantially lower input current levels than FAST™ (5µA max.)
- 8-input universal shift register
- JEDEC standard pinout for DIP and LCC
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B
- Standard Military Drawing# 5962-86862 is listed on this function. Refer to section 2

## DESCRIPTION:

The IDT54/74FCT299 and IDT54/74FCT299A are built using advanced CEMOS™, a dual-metal CMOS technology. The IDT54/74FCT299 and IDT54/74FCT299A are 8-input universal shift/storage registers with 3-state outputs. Four modes of operation are possible: hold (store), shift left, shift right and load data. The parallel load inputs and flip-flop outputs are multiplexed to reduce the total number of package pins. Additional outputs are provided for flip-flops Q0 and Q7 to allow easy serial cascading. A separate active LOW Master Reset is used to reset the register.

## FUNCTIONAL BLOCK DIAGRAM



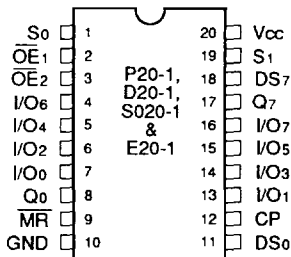
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CEMOS is a trademark of Integrated Device Technology, Inc.  
FAST is a registered trademark of National Semiconductor Co.

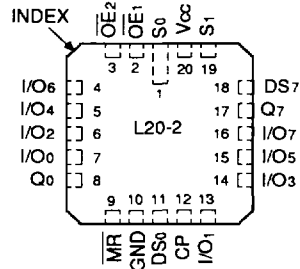
MILITARY AND COMMERCIAL TEMPERATURE RANGES

JUNE 1990

PIN CONFIGURATIONS



DIP/SOIC/CERPACK  
TOP VIEW



LCC  
TOP VIEW

2561 drw 02

PIN DESCRIPTION

Pin Names	Description
CP	Clock Pulse Input (Active Edge Rising)
DS0	Serial Data Input for Right Shift
DS7	Serial Data Input for Left Shift
S0, S1	Mode Select Inputs
MR	Asynchronous Master Reset Input (Active LOW)
OE1, OE2	3-State Output Enable Inputs (Active LOW)
I/O0-I/O7	Parallel Data Inputs or 3-State Parallel Outputs
Q0, Q7	Serial Outputs

2561 tbl 05

FUNCTION TABLE<sup>(1)</sup>

Inputs				Response
MR	S1	S0	CP	
L	X	X	X	Asynchronous Reset Q0-Q7 = LOW
H	H	H	/	Parallel Load; I/On → Qn
H	L	H	/	Shift Right; DS0 → Q0, Q0 → Q1, etc.
H	H	L	/	Shift Left; DS7 → Q7, Q7 → Q6, etc.
H	L	L	X	Hold

2561 tbl 06

NOTE:

- H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Don't Care  
/ = LOW-to-HIGH clock transition

ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

Symbol	Rating	Commercial	Military	Unit
VTERM <sup>(2)</sup>	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
VTERM <sup>(3)</sup>	Terminal Voltage with Respect to GND	-0.5 to Vcc	-0.5 to Vcc	V
TA	Operating Temperature	0 to +70	-55 to +125	°C
TBIAS	Temperature Under Bias	-55 to +125	-65 to +135	°C
TSTG	Storage Temperature	-55 to +125	-65 to +150	°C
PT	Power Dissipation	0.5	0.5	W
IOUT	DC Output Current	120	120	mA

NOTES:

2561 tbl 01

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed Vcc by +0.5 unless otherwise noted.
- Inputs and Vcc terminals only.
- Outputs and I/O terminals only.

CAPACITANCE (TA = +25°C, f = 1.0MHz)

Symbol	Parameter <sup>(1)</sup>	Conditions	Typ.	Max.	Unit
CIN	Input Capacitance	VIN = 0V	6	10	pF
CIO	I/O Capacitance	VOUT = 0V	8	12	pF

NOTE:

2561 tbl 02

- This parameter is guaranteed by characterization data and not tested.

### DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:  $V_{LC} = 0.2V$ ;  $V_{HC} = V_{CC} - 0.2V$

Commercial:  $T_A = 0^\circ C$  to  $+70^\circ C$ ,  $V_{CC} = 5.0V \pm 5\%$ ; Military:  $T_A = -55^\circ C$  to  $+125^\circ C$ ,  $V_{CC} = 5.0V \pm 10\%$

Symbol	Parameter	Test Conditions <sup>(1)</sup>	Min.	Typ. <sup>(2)</sup>	Max.	Unit	
$V_{IH}$	Input HIGH Level	Guaranteed Logic HIGH Level	2.0	—	—	V	
$V_{IL}$	Input LOW Level	Guaranteed Logic LOW Level	—	—	0.8	V	
$I_{IH}$	Input HIGH Current (Except I/O Pins)	$V_{CC} = \text{Max.}$	$V_I = V_{CC}$	—	—	5	$\mu A$
			$V_I = 2.7V$	—	—	5 <sup>(4)</sup>	
$I_{IL}$	Input LOW Current (Except I/O Pins)	$V_{CC} = \text{Max.}$	$V_I = 0.5V$	—	—	-5 <sup>(4)</sup>	$\mu A$
			$V_I = \text{GND}$	—	—	-5	
$I_{IH}$	Input HIGH Current (I/O Pins Only)	$V_{CC} = \text{Max.}$	$V_I = V_{CC}$	—	—	15	$\mu A$
			$V_I = 2.7V$	—	—	15 <sup>(4)</sup>	
$I_{IL}$	Input LOW Current (I/O Pins Only)	$V_{CC} = \text{Max.}$	$V_I = 0.5V$	—	—	-15 <sup>(4)</sup>	$\mu A$
			$V_I = \text{GND}$	—	—	-15	
$V_{IK}$	Clamp Diode Voltage	$V_{CC} = \text{Min.}, I_N = -18mA$	—	-0.7	-1.2	V	
$I_{OS}$	Short Circuit Current	$V_{CC} = \text{Max.}^{(3)}, V_O = \text{GND}$	-60	-120	—	mA	
$V_{OH}$	Output HIGH Voltage	$V_{CC} = 3V, V_{IN} = V_{LC} \text{ or } V_{HC}, I_{OH} = -32\mu A$	$V_{HC}$	$V_{CC}$	—	V	
		$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OH} = -300\mu A$	$V_{HC}$	$V_{CC}$		—
			$I_{OH} = -12mA \text{ MIL.}$	2.4	4.3		—
			$I_{OH} = -15mA \text{ COM'L.}$	2.4	4.3		—
$V_{OL}$	Output LOW Voltage	$V_{CC} = 3V, V_{IN} = V_{LC} \text{ or } V_{HC}, I_{OL} = 300\mu A$	—	GND	$V_{LC}$	V	
		$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OL} = 300\mu A$	—	GND		$V_{LC}^{(4)}$
			$I_{OL} = 32mA \text{ MIL.}$	—	0.3		0.5
			$I_{OL} = 48mA \text{ COM'L.}$	—	0.3		0.5

**NOTES:**

- 1 For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type
- 2 Typical values are at  $V_{CC} = 5.0V, +25^\circ C$  ambient and maximum loading.
- 3 Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second
- 4 This parameter is guaranteed but not tested.

2561 fb 05

### POWER SUPPLY CHARACTERISTICS

$V_{LC} = 0.2V$ ;  $V_{HC} = V_{CC} - 0.2V$

Symbol	Parameter	Test Conditions <sup>(1)</sup>		Min.	Typ. <sup>(2)</sup>	Max.	Unit
I <sub>CC</sub>	Quiescent Power Supply Current	V <sub>CC</sub> = Max. V <sub>IN</sub> ≥ V <sub>HC</sub> ; V <sub>IN</sub> ≤ V <sub>LC</sub>		—	0.2	1.5	mA
ΔI <sub>CC</sub>	Quiescent Power Supply Current TTL Inputs HIGH	V <sub>CC</sub> = Max. V <sub>IN</sub> = 3.4V <sup>(3)</sup>		—	0.5	2.0	mA
I <sub>CCD</sub>	Dynamic Power Supply Current <sup>(4)</sup>	V <sub>CC</sub> = Max. Outputs Open $\overline{OE}_1 = \overline{OE}_2 = GND$ $\overline{MR} = V_{CC}$ S <sub>0</sub> = S <sub>1</sub> = V <sub>CC</sub> DS <sub>0</sub> = DS <sub>1</sub> = GND One Input Toggling 50% Duty Cycle	V <sub>IN</sub> ≥ V <sub>HC</sub> V <sub>IN</sub> ≤ V <sub>LC</sub>	—	0.15	0.25	mA/MHz
I <sub>C</sub>	Total Power Supply Current <sup>(5)</sup>	V <sub>CC</sub> = Max. Outputs Open f <sub>CP</sub> = 10MHz 50% Duty Cycle $\overline{OE}_1 = \overline{OE}_2 = GND$ $\overline{MR} = V_{CC}$ S <sub>0</sub> = S <sub>1</sub> = V <sub>CC</sub> DS <sub>0</sub> = DS <sub>7</sub> = GND One Bit Toggling at f <sub>i</sub> = 5MHz 50% Duty Cycle	V <sub>IN</sub> ≥ V <sub>HC</sub> V <sub>IN</sub> ≤ V <sub>LC</sub> (FCT)	—	1.7	4.0	mA
			V <sub>IN</sub> = 3.4V V <sub>IN</sub> = GND	—	2.2	6.0	
		V <sub>CC</sub> = Max. Outputs Open f <sub>CP</sub> = 10MHz 50% Duty Cycle $\overline{OE}_1 = \overline{OE}_2 = GND$ $\overline{MR} = V_{CC}$ S <sub>0</sub> = S <sub>7</sub> = V <sub>CC</sub> DS <sub>0</sub> = DS <sub>7</sub> = GND Eight Bits Toggling at f <sub>i</sub> = 2.5MHz 50% Duty Cycle	V <sub>IN</sub> ≥ V <sub>HC</sub> V <sub>IN</sub> ≤ V <sub>LC</sub> (FCT)	—	4.0	7.8 <sup>(5)</sup>	
			V <sub>IN</sub> = 3.4V V <sub>IN</sub> = GND	—	6.2	16.8 <sup>(5)</sup>	

**NOTES:**

2561 tbl 06

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at V<sub>CC</sub> = 5.0V, +25°C ambient.
- Per TTL driven input (V<sub>IN</sub> = 3.4V); all other inputs at V<sub>CC</sub> or GND
- This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
- Values for these conditions are examples of the I<sub>CC</sub> formula. These limits are guaranteed but not tested.
- $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$   
 $I_C = I_{CC} + \Delta I_{CC} \cdot DH + I_{CCD} (f_{CP}/2 + f_i N_i)$   
 I<sub>CC</sub> = Quiescent Current  
 ΔI<sub>CC</sub> = Power Supply Current for a TTL High Input (V<sub>IN</sub> = 3.4V)  
 DH = Duty Cycle for TTL Inputs High  
 N<sub>T</sub> = Number of TTL Inputs at DH  
 I<sub>CCD</sub> = Dynamic Current Caused by an Output Transition Pair (HLH or LHL)  
 f<sub>CP</sub> = Clock Frequency for Register Devices (Zero for Non-Register Devices)  
 f<sub>i</sub> = Input Frequency  
 N<sub>i</sub> = Number of Inputs at f<sub>i</sub>  
 All currents are in milliamps and all frequencies are in megahertz.



**SWITCHING CHARACTERISTICS OVER OPERATING RANGE**

Symbol	Parameter	Condition <sup>(1)</sup>	IDT54/74FCT299				IDT54/74FCT299A				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min. <sup>(2)</sup>	Max.	Min. <sup>(2)</sup>	Max.	Min. <sup>(2)</sup>	Max.	Min. <sup>(2)</sup>	Max.	
tPLH tPHL	Propagation Delay CP to Q <sub>0</sub> or Q <sub>7</sub>	C <sub>L</sub> = 50pF R <sub>L</sub> = 500Ω	2.0	10.0	2.0	14.0	2.0	7.2	2.0	9.5	ns
tPLH tPHL	Propagation Delay CP to I/O <sub>n</sub>		2.0	12.0	2.0	12.0	2.0	7.2	2.0	9.5	ns
tPHL	Propagation Delay MR to Q <sub>0</sub> or Q <sub>7</sub>		2.0	10.0	2.0	10.5	2.0	7.2	2.0	9.5	ns
tPHL	Propagation Delay MR to I/O <sub>n</sub>		2.0	15.0	2.0	15.0	2.0	8.7	2.0	11.5	ns
tPZH tPZL	Output Enable Time OE <sub>n</sub> to I/O <sub>n</sub>		1.5	11.0	1.5	15.0	1.5	6.5	1.5	7.5	ns
tPHZ tPLZ	Output Disable Time OE <sub>n</sub> to I/O <sub>n</sub>		1.5	7.0	1.5	9.0	1.5	5.5	1.5	6.5	ns
tSU	Set-up Time HIGH or LOW S <sub>0</sub> or S <sub>1</sub> to CP		7.5	—	7.5	—	3.5	—	4.0	—	ns
tH	Hold Time HIGH or LOW S <sub>0</sub> or S <sub>1</sub> to CP		1.0	—	1.0	—	1.0	—	1.0	—	ns
tSU	Set-up Time HIGH or LOW I/O <sub>n</sub> , DS <sub>0</sub> or DS <sub>7</sub> to CP		5.5	—	5.5	—	4.0	—	4.5	—	ns
tH	Hold Time HIGH or LOW I/O <sub>n</sub> , DS <sub>0</sub> or DS <sub>7</sub> to CP		1.5	—	1.5	—	1.5	—	1.5	—	ns
tW	CP Pulse Width HIGH or LOW		7.0	—	7.0	—	5.0	—	6.0	—	ns
tW	MR Pulse Width LOW		7.0	—	7.0	—	5.0	—	6.0	—	ns
tREM	Recovery Time MR to CP		7.0	—	7.0	—	5.0	—	6.0	—	ns

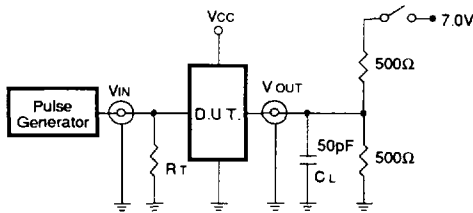
**NOTES:**

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.

2561 tbi 07

## TEST CIRCUITS AND WAVEFORMS

### TEST CIRCUITS FOR ALL OUTPUTS



### SWITCH POSITION

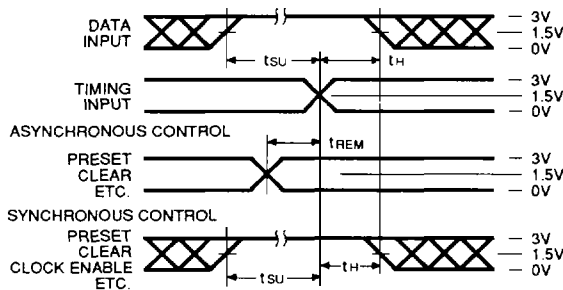
Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Outputs	Open

#### DEFINITIONS:

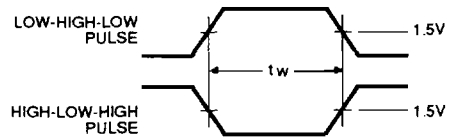
CL = Load capacitance: includes jig and probe capacitance.  
RT = Termination resistance: should be equal to ZOUT of the Pulse Generator.

2561 01 08

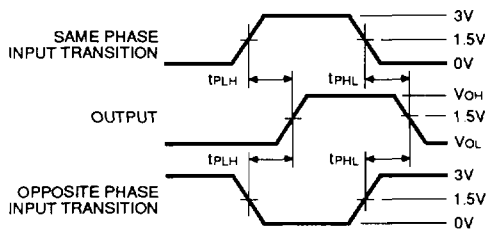
### SET-UP, HOLD AND RELEASE TIMES



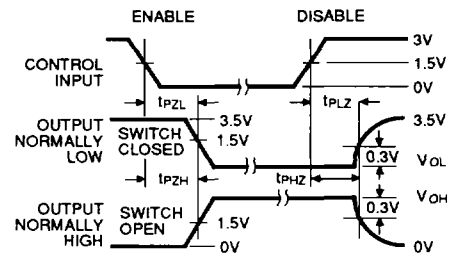
### PULSE WIDTH



### PROPAGATION DELAY



### ENABLE AND DISABLE TIMES

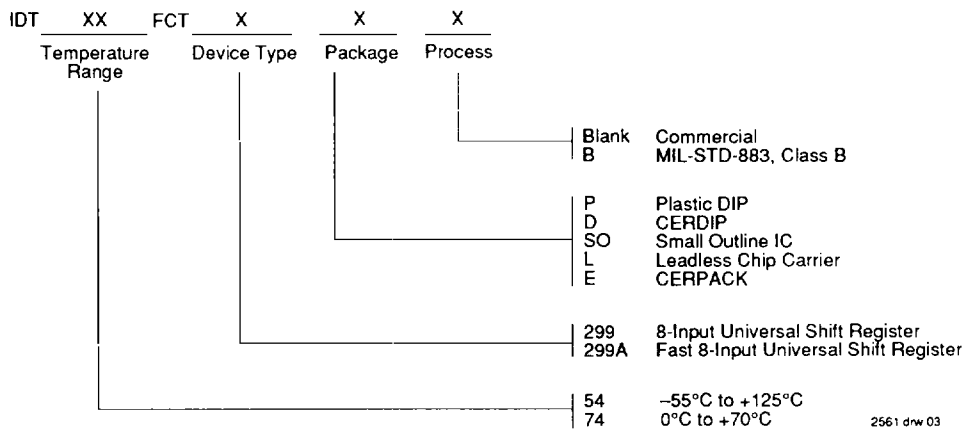


#### NOTES

- Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
- Pulse Generator for All Pulses: Rate  $\leq 1.0$  MHz;  $Z_0 \leq 50\Omega$ ;  $t_f \leq 2.5$  ns;  $t_r \leq 2.5$  ns.

2561 drw 04

**ORDERING INFORMATION**



2561 drw 03