



# MX26L6420

## 64M-BIT [4M x 16] CMOS MULTIPLE-TIME-PROGRAMMABLE EPROM

### FEATURES

- 4,194,304 x 16 byte structure
- Single Power Supply Operation
  - 3.0 to 3.6 volt for read, erase and program operations
- Low VCC write inhibit is equal to or less than 2.5V
- Compatible with JEDEC standard
- High Performance
  - Fast access time: 90/100/120ns (typ.)
  - Fast program time: 140s/chip (typ.)
  - Fast erase time: 150s/chip (typ.)
- Low Power Consumption
  - Low active read current: 17mA (typ.) at 5MHz
  - Low standby current: 30uA (typ.)
- Minimum 100 erase/program cycle
- Status Reply
  - Data polling & Toggle bits provide detection of program and erase operation completion
- 12V ACC input pin provides accelerated program capability
- Output voltages and input voltages on the device is determined by the voltage on the VI/O pin.
  - VI/O voltage range: 1.65V~3.6V
- 10 years data retention
- Package
  - 44-Pin SOP
  - 48-Pin TSOP

### GENERAL DESCRIPTION

The MX26L6420 is a 64M bit MTP EPROM™ organized as 4M bytes of 16 bits. MXIC's MTP EPROM™ offer the most cost-effective and reliable read/write non-volatile random access memory. The MX26L6420 is packaged in 44-pin SOP and 48-pin TSOP. It is designed to be reprogrammed and erased in system or in standard EPROM programmers.

The standard MX26L6420 offers access time as fast as 90ns, allowing operation of high-speed microprocessors without wait states. To eliminate bus contention, the MX26L6420 has separate chip enable ( $\overline{CE}$ ) and output enable ( $\overline{OE}$ ) controls. MXIC's MTP EPROM™ augment EPROM functionality with in-circuit electrical erasure and programming. The MX26L6420 uses a command register to manage this functionality.

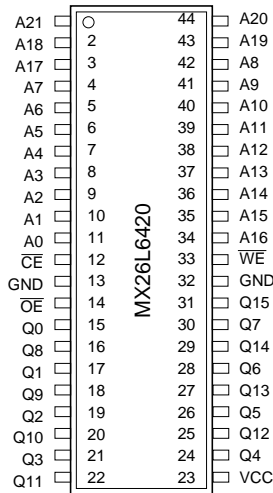
MXIC's MTP EPROM™ technology reliably stores memory contents even after 100 erase and program cycles. The MXIC cell is designed to optimize the erase and program mechanisms. In addition, the combination of advanced tunnel oxide processing and low internal electric fields for erase and programming operations produces reliable cycling.

The MX26L6420 uses a 3.0V to 3.6V VCC supply to perform the High Reliability Erase and auto Program/Erase algorithms.

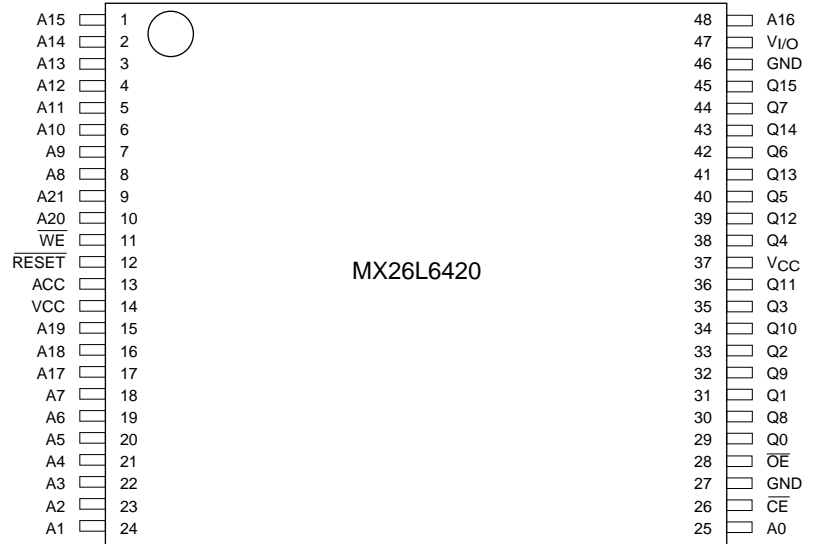
The highest degree of latch-up protection is achieved with MXIC's proprietary non-epi process. Latch-up protection is proved for stresses up to 100 milliamps on address and data pin from -1V to VCC +1V.

## PIN CONFIGURATION

### 44 SOP



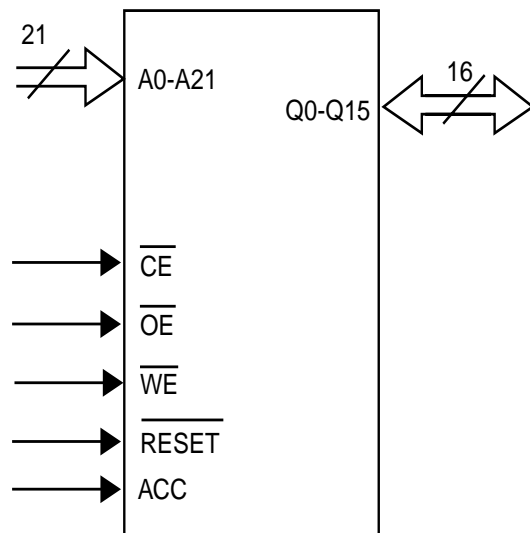
### 48 TSOP

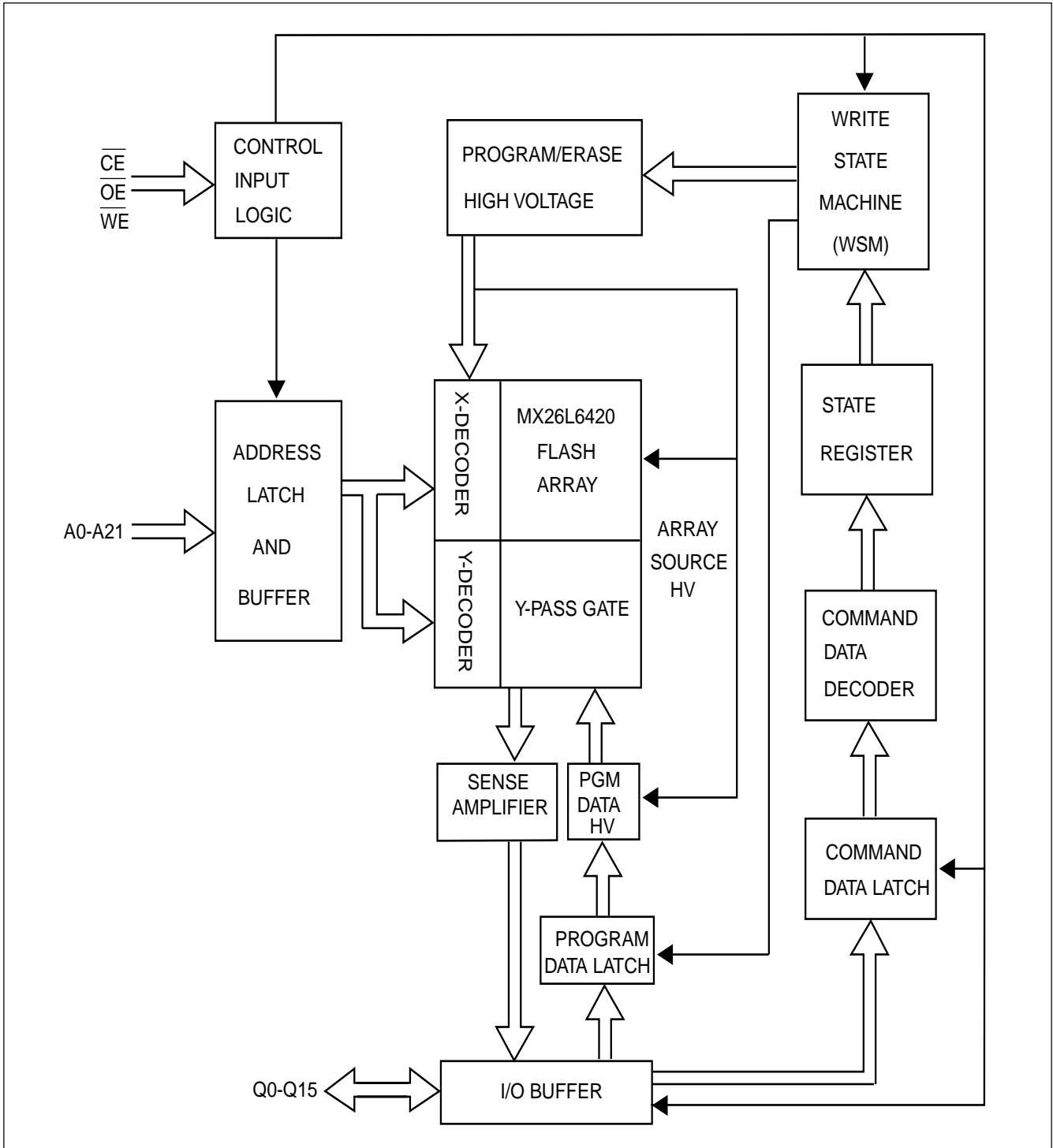


## PIN DESCRIPTION

SYMBOL	PIN NAME
A0~A21	Address Input
Q0~Q15	Data Inputs/Outputs
CE	Chip Enable Input
WE	Write Enable Input
OE	Output Enable Input
RESET	Hardware Reset Pin, Active Low (for 48 TSOP only)
VCC	Power supply
ACC	Hardware Acceleration Pin (for 48 TSOP only)
VI/O	I/O power supply (for 48 TSOP only)
GND	Device Ground

## LOGIC SYMBOL



**BLOCK DIAGRAM**


## **AUTOMATIC PROGRAMMING**

The MX26L6420 is word programmable using the Automatic Programming algorithm. The Automatic Programming algorithm makes the external system do not need to have time out sequence nor to verify the data programmed. The typical chip programming time at room temperature of the MX26L6420 is around 140 seconds.

## **AUTOMATIC PROGRAMMING ALGORITHM**

MXIC's Automatic Programming algorithm require the user to only write program set-up commands (including 2 unlock write cycle and A0H) and a program command (program data and address). The device automatically times the programming pulse width, provides the program verification, and counts the number of sequences. A status bit similar to  $\overline{\text{DATA}}$  polling and a status bit toggling between consecutive read cycles, provide feedback to the user as to the status of the programming operation.

## **AUTOMATIC CHIP ERASE**

The entire chip is bulk erased using 50 ms erase pulses according to MXIC's Automatic Chip Erase algorithm. Typical erasure at room temperature is around 150 seconds. The Automatic Erase algorithm automatically programs the entire array prior to electrical erase. The timing and verification of electrical erase are controlled internally within the device.

## **AUTOMATIC ERASE ALGORITHM**

MXIC's Automatic Erase algorithm requires the user to write commands to the command register using standard microprocessor write timings. The device will automatically pre-program and verify the entire array. Then the device automatically times the erase pulse width, provides the erase verification, and counts the number of sequences. A status bit toggling between consecutive read cycles provides feedback to the user as to the status of the programming operation.

Register contents serve as inputs to an internal state-machine which controls the erase and programming circuitry. During write cycles, the command register internally latches address and data needed for the program-

ming and erase operations. All address are latched on the falling edge of  $\overline{\text{WE}}$  or  $\overline{\text{CE}}$ , whichever happens later. All data are latched on rising edge of  $\overline{\text{WE}}$  or  $\overline{\text{CE}}$ , whichever happens first.

MXIC's Flash technology combines years of EPROM experience to produce the highest levels of quality, reliability, and cost effectiveness. The MX26L6420 electrically erases all bits simultaneously using Fowler-Nordheim tunneling. The bytes are programmed by using the EPROM programming mechanism of hot electron injection.

During a program cycle, the state-machine will control the program sequences and command register will not respond to any command set. After the state machine has completed its task, it will allow the command register to respond to its full command set.

**Table 1**
**BUS OPERATION (1)**

Operation	$\overline{\text{CE}}$	$\overline{\text{OE}}$	$\overline{\text{WE}}$	$\overline{\text{RESET}}$	Address	Q15~Q0
Read	L	L	H	H	A <sub>IN</sub>	D <sub>OUT</sub>
Write(Note 1)	L	H	L	H	A <sub>IN</sub>	D <sub>IN</sub>
Standby	VCC±0.3V	X	X	VCC±0.3V	X	High-Z
Output Disable	L	H	H	H	X	High-Z
Reset	X	X	X	L	X	High-Z

Legend:

 L=Logic LOW= $V_{IL}$ , H=Logic High= $V_{IH}$ ,  $V_{ID}=12.0\pm 0.5V$ , X=Don't Care, A<sub>IN</sub>=Address IN, D<sub>IN</sub>=Data IN, D<sub>OUT</sub>=Data OUT

Notes:

1. When the ACC pin is at  $V_{HH}$ , the device enters the accelerated program mode. See "Accelerated Program Operations" for more information.

**Table 2. AUTOSELECT CODES (High Voltage Method)**

Operation	$\overline{\text{CE}}$	$\overline{\text{OE}}$	$\overline{\text{WE}}$	A0	A1	A5 to A2	A6	A8 to A7	A9	A14 to A10	A15~A21	Q15~Q0
Read Silicon ID Manufactures Code	L	L	H	L	L	X	L	X	$V_{ID}$	X	X	00C2H
Read Silicon ID Device Code	L	L	H	H	L	X	L	X	$V_{ID}$	X	X	22FCH

## REQUIREMENTS FOR READING ARRAY DATA

To read array data from the outputs, the system must drive the  $\overline{CE}$  and  $\overline{OE}$  pins to VIL.  $\overline{CE}$  is the power control and selects the device.  $\overline{OE}$  is the output control and gates array data to the output pins.  $\overline{WE}$  should remain at VIH.

The internal state machine is set for reading array data upon device power-up, or after a hardware reset. This ensures that no spurious alteration of the memory content occurs during the power transition. No command is necessary in this mode to obtain array data. Standard microprocessor read cycles that assert valid address on the device address inputs produce valid data on the device data outputs. The device remains enabled for read access until the command register contents are altered.

## WRITE COMMANDS/COMMAND SEQUENCES

To program data to the device or erase memory, the system must drive  $\overline{WE}$  and  $\overline{CE}$  to VIL, and  $\overline{OE}$  to VIH.

An erase operation can erase the entire device. The "Writing specific address and data commands or sequences into the command register initiates device operations. Table 1 defines the valid register command sequences. Writing incorrect address and data values or writing them in the improper sequence resets the device to reading array data. Section has details on erasing the entire chip.

After the system writes the autoselect command sequence, the device enters the autoselect mode. The system can then read autoselect codes from the internal register (which is separate from the memory array) on Q15-Q0. Standard read cycle timings apply in this mode. Refer to the Autoselect Mode and Autoselect Command Sequence section for more information.

ICC2 in the DC Characteristics table represents the active current specification for the write mode. The "AC Characteristics" section contains timing specification table and timing diagrams for write operations.

## STANDBY MODE

MX26L6420 can be set into Standby mode with two different approaches. One is using both  $\overline{CE}$  and  $\overline{RESET}$  pins and the other one is using  $\overline{RESET}$  pin only.

When using both pins of  $\overline{CE}$  and  $\overline{RESET}$ , a CMOS Standby mode is achieved with both pins held at  $VCC \pm 0.3V$ . Under this condition, the current consumed is less than 50uA (typ.). If both of the  $\overline{CE}$  and  $\overline{RESET}$  are held at VIH, but not within the range of  $VCC \pm 0.3V$ , the device will still be in the standby mode, but the standby current will be larger. During Auto Algorithm operation, VCC active current (Icc2) is required even  $\overline{CE} = "H"$  until the operation is completed. The device can be read with standard access time ( $t_{CE}$ ) from either of these standby modes.

When using only  $\overline{RESET}$ , a CMOS standby mode is achieved with  $\overline{RESET}$  input held at  $V_{SS} \pm 0.3V$ . Under this condition the current is consumed less than 50uA (typ.). Once the  $\overline{RESET}$  pin is taken high. The device is back to active without recovery delay.

In the standby mode the outputs are in the high impedance state, independent of the  $\overline{OE}$  input.

MX26L6420 is capable to provide the Automatic Standby Mode to restrain power consumption during readout of data. This mode can be used effectively with an application requested low power consumption such as handy terminals.

To active this mode, MX26L6420 automatically switch themselves to low power mode when MX26L6420 addresses remain stable during access time of  $t_{ACC}+30ns$ . It is not necessary to control  $\overline{CE}$ ,  $\overline{WE}$ , and  $\overline{OE}$  on the mode. Under the mode, the current consumed is typically 50uA (CMOS level).

## OUTPUT DISABLE

With the  $\overline{OE}$  input at a logic high level (VIH), output from the devices are disabled. This will cause the output pins to be in a high impedance state.

## RESET OPERATION

The  $\overline{\text{RESET}}$  pin provides a hardware method of resetting the device to reading array data. When the  $\overline{\text{RESET}}$  pin is driven low for at least a period of  $t_{\text{RP}}$ , the device immediately terminates any operation in progress, tri-states all output pins, and ignores all read/write commands for the duration of the  $\overline{\text{RESET}}$  pulse. The device also resets the internal state machine to reading array data. The operation that was interrupted should be reinitiated once the device is ready to accept another command sequence, to ensure data integrity.

Current is reduced for the duration of the  $\overline{\text{RESET}}$  pulse. When  $\overline{\text{RESET}}$  is held at  $V_{\text{SS}} \pm 0.3\text{V}$ , the device draws CMOS standby current ( $I_{\text{CC4}}$ ). If  $\overline{\text{RESET}}$  is held at  $V_{\text{IL}}$  but not within  $V_{\text{SS}} \pm 0.3\text{V}$ , the standby current will be greater.

The  $\overline{\text{RESET}}$  pin may be tied to system reset circuitry. A system reset would that also reset the MTP EPROM.

Refer to the AC Characteristics tables for  $\overline{\text{RESET}}$  parameters and to Figure 14 for the timing diagram.

## SILICON ID READ OPERATION

MTP EPROM are intended for use in applications where the local CPU alters memory contents. As such, manufacturer and device codes must be accessible while the device resides in the target system. EPROM programmers typically access signature codes by raising A9 to a high voltage. However, multiplexing high voltage onto address lines is not generally desired system design practice.

MX26L6420 provides hardware method to access the silicon ID read operation. Which method requires  $V_{\text{ID}}$  on A9 pin,  $V_{\text{IL}}$  on  $\overline{\text{CE}}$ ,  $\overline{\text{OE}}$ , A6, and A1 pins. Which apply  $V_{\text{IL}}$  on A0 pin, the device will output MXIC's manufacture code of C2H. Which apply  $V_{\text{IH}}$  on A0 pin, the device will output MX26L6420 device code of 22FCH.

## VI/O PIN OPERATION

MX26L6420 is capable to provide the I/O power supply ( $V_{\text{I/O}}$ ) pin to control Input/Output voltage levels of the device. The data outputs and voltage tolerated at its data input is determined by the voltage on the  $V_{\text{I/O}}$  pin. This device is allows to operate in 1.8V or 3V system as required.

**Table 3**

Part No.	VCC / VI/O Voltage Range	
	VCC=3.0V to 3.6V	VCC=3.0V to 3.6V
	VI/O=3.0V to 3.6V	VI/O=1.65V to 2.9V
MX26L6420-90	90ns	100ns
MX26L6420-10	100ns	110ns
MX26L6420-12	120ns	130ns

Notes: Typical values measured at  $V_{\text{CC}}=3.0\text{V}$  to  $3.6\text{V}$ ,  $V_{\text{I/O}}=3.0\text{V}$  to  $3.6\text{V}$

## DATA PROTECTION

The MX26L6420 is designed to offer protection against accidental erasure or programming caused by spurious system level signals that may exist during power transition. During power up the device automatically resets the state machine in the Read mode. In addition, with its control register architecture, alteration of the memory contents only occurs after successful completion of specific command sequences. The device also incorporates several features to prevent inadvertent write cycles resulting from  $V_{\text{CC}}$  power-up and power-down transition or system noise.

**LOW VCC WRITE INHIBIT**

When VCC is less than VLKO the device does not accept any write cycles. This protects data during VCC power-up and power-down. The command register and all internal program/erase circuits are disabled, and the device resets. Subsequent writes are ignored until VCC is greater than VLKO. The system must provide the proper signals to the control pins to prevent unintentional write when VCC is greater than VLKO.

**WRITE PULSE "GLITCH" PROTECTION**

Noise pulses of less than 5ns(typical) on  $\overline{CE}$  or  $\overline{WE}$  will not initiate a write cycle.

**LOGICAL INHIBIT**

Writing is inhibited by holding any one of  $\overline{OE} = VIL$ ,  $\overline{CE} = VIH$  or  $\overline{WE} = VIH$ . To initiate a write cycle  $\overline{CE}$  and  $\overline{WE}$  must be a logical zero while  $\overline{OE}$  is a logical one.

**POWER-UP SEQUENCE**

The MX26L6420 powers up in the Read only mode. In addition, the memory contents may only be altered after successful completion of the predefined command sequences.



**SOFTWARE COMMAND DEFINITIONS**

Device operations are selected by writing specific address and data sequences into the command register. Writing incorrect address and data values or writing them in the improper sequence will reset the device to the read mode. Table 4 defines the valid register command sequences. Either of the two reset command sequences

will reset the device (when applicable).

All addresses are latched on the falling edge of  $\overline{WE}$  or  $\overline{CE}$ , whichever happens later. All data are latched on rising edge of  $\overline{WE}$  or  $\overline{CE}$ , whichever happens first.

**TABLE 4. MX26L6420 COMMAND DEFINITIONS**

Command	Bus Cycle	First Bus Cycle		Second Bus Cycle		Third Bus Cycle		Fourth Bus Cycle		Fifth Bus Cycle		Sixth Bus Cycle	
		Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read(Note 5)	1	RA	RD										
Reset(Note 6)	1	XXX	F0										
Autoselect(Note 7)													
Manufacturer ID	4	555	AA	2AA	55	555	90	X00	C2				
Device ID	4	555	AA	2AA	55	555	90	X01	22FC				
Program	4	555	AA	2AA	55	555	A0	PA	PD				
Chip Erase	6	555	AA	2AA	55	555	80	555	AA	2AA	55	555	10

**Legend:**

X=Don't care

RA=Address of the memory location to be read.

RD=Data read from location RA during read operation.

PA=Address of the memory location to be programmed.

Addresses are latched on the falling edge of the  $\overline{WE}$  or  $\overline{CE}$  pulse.

PD=Data to be programmed at location PA. Data is latched on the rising edge of  $\overline{WE}$  or  $\overline{CE}$  pulse.

**Notes:**

1. See Table 1 for descriptions of bus operations.
2. All values are in hexadecimal.
3. Except when reading array or autoselect data, all bus cycles are write operation.
4. Address bits are don't care for unlock and command cycles, except when PA is required.
5. No unlock or command cycles required when device is in read mode.
6. The Reset command is required to return to the read mode when the device is in the autoselect mode or if Q5 goes high.
7. The fourth cycle of the autoselect command sequence is a read cycle.
8. Command is valid when device is ready to read array data or when device is in autoselect mode.

## READING ARRAY DATA

The device is automatically set to reading array data after device power-up. No commands are required to retrieve data. The device is also ready to read array data after completing an Automatic Program or Automatic Erase algorithm.

The system must issue the reset command to re-enable the device for reading array data if Q5 goes high, or while in the autoselect mode. See the "Reset Command" section, next.

## RESET COMMAND

Writing the reset command to the device resets the device to reading array data. Address bits are don't care for this command.

The reset command may be written between the sequence cycles in an erase command sequence before erasing begins. This resets the device to reading array data. Once erasure begins, however, the device ignores reset commands until the operation is complete.

The reset command may be written between the sequence cycles in a program command sequence before programming begins. This resets the device to reading array data. Once programming begins, however, the device ignores reset commands until the operation is complete.

The reset command may be written between the sequence cycles in an SILICON ID READ command sequence. Once in the SILICON ID READ mode, the reset command must be written to return to reading array data.

If Q5 goes high during a program or erase operation, writing the reset command returns the device to reading array data.

## SILICON ID READ COMMAND SEQUENCE

The SILICON ID READ command sequence allows the host system to access the manufacturer and device codes, and determine whether or not. Table 4 shows the address and data requirements. This method is an alternative to that shown in Table 1, which is intended for EPROM programmers and requires V<sub>ID</sub> on address bit A9.

The SILICON ID READ command sequence is initiated by writing two unlock cycles, followed by the SILICON ID READ command. The device then enters the SILICON ID READ mode, and the system may read at any address any number of times, without initiating another command sequence. A read cycle at address XX00h retrieves the manufacturer code. A read cycle at address XX01h returns the device code.

The system must write the reset command to exit the autoselect mode and return to reading array data.

## WORD PROGRAM COMMAND SEQUENCE

The command sequence requires four bus cycles, and is initiated by writing two unlock write cycles, followed by the program set-up command. The program address and data are written next, which in turn initiate the Embedded Program algorithm. The system is not required to provide further controls or timings. The device automatically generates the program pulses and verifies the programmed cell margin. Table 4 shows the address and data requirements for the byte program command sequence.

When the Embedded Program algorithm is complete, the device then returns to reading array data and addresses are no longer latched. The system can determine the status of the program operation by using Q7, Q6. See "Write Operation Status" for information on these status bits.

Any commands written to the device during the Embedded Program Algorithm are ignored. Note that a hardware reset immediately terminates the programming operation. The Word Program command sequence should be reinitiated once the device has reset to reading array data, to ensure data integrity.

Programming is allowed in any sequence. A bit cannot be programmed from a "0" back to a "1". Cause the Data Polling algorithm to indicate the operation was successful. However, a succeeding read will show that the data is still "0". Only erase operations can convert a "0" to a "1".

### ACCELERATED PROGRAM OPERATIONS

The device offers accelerated program operations through the ACC pin. When the system asserts  $V_{HH}$  on the ACC pin, the device automatically bypass the two "Unlock" write cycle. The device uses the higher voltage on the ACC pin to accelerate the operation. Removing  $V_{HH}$  from the ACC pin returns the device to normal operation. Under normal operation ACC can be VCC or GND. Note that the ACC pin must not be at  $V_{HH}$  any operation other than accelerated programming, or device damage may result.

### SETUP AUTOMATIC CHIP ERASE

Chip erase is a six-bus cycle operation. There are two "unlock" write cycles. These are followed by writing the "set-up" command 80H. Two more "unlock" write cycles are then followed by the chip erase command 10H.

The MX26L6420 contains a Silicon-ID-Read operation to supplement traditional PROM programming methodology. The operation is initiated by writing the read silicon ID command sequence into the command register. Following the command write, a read cycle with A6=VIL, A1=VIL, A0=VIL retrieves the manufacturer code of C2H. A read cycle with A6=VIL, A1=VIL, A0=VIH returns the device code of 22FCH for MX26L6420.

### AUTOMATIC CHIP ERASE COMMAND

The device does not require the system to preprogram prior to erase. The Automatic Erase algorithm automatically preprogram and verifies the entire memory for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations. Table 4 shows the address and data requirements for the chip erase command sequence.

Any commands written to the chip during the Automatic Erase algorithm are ignored. Note that a hardware reset during the chip erase operation immediately terminates the operation. The Chip Erase command sequence should be reinitiated once the device has returned to reading array data, to ensure data integrity.

The system can determine the status of the erase operation by using Q7, Q6. See "Write Operation Status" for information on these status bits. When the Automatic Erase algorithm is complete, the device returns to reading array data and addresses are no longer latched.

Figure 5 illustrates the algorithm for the erase operation. See the Erase/Program Operations tables in "AC Characteristics" for parameters, and to Figure 4 for timing diagrams.

**TABLE 5. SILICON ID CODE**

Pins	A0	A1	A6	Q15	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0	Code(Hex)
				Q8									
Manufacture code	VIL	VIL	VIL	00H	1	1	0	0	0	0	1	0	00C2H
Device code for MX26L6420	VIH	VIL	VIL	22H	1	1	1	1	1	1	0	0	22FCH

**WRITE OPERATION STATUS**

The device provides several bits to determine the status of a write operation: Q5, Q6, Q7. Table 10 and the following subsections describe the functions of these bits. Q7, and Q6 each offer a method for determining whether a program or erase operation is complete or in progress. These three bits are discussed first.

**Table 6. Write Operation Status**

	Status	Q7	Q6 Note1	Q5
In Progress	Word Program in Auto Program Algorithm	$\overline{Q7}$	Toggle	0
	Auto Erase Algorithm	0	Toggle	0
Exceeded Time Limits	Word Program in Auto Program Algorithm	$\overline{Q7}$	Toggle	1
	Auto Erase Algorithm	0	Toggle	1

Notes:

1. Performing successive read operations from any address will cause Q6 to toggle.

### **Q7: Data Polling**

The Data Polling bit, Q7, indicates to the host system whether an Automatic Algorithm is in progress or completed. Data Polling is valid after the rising edge of the final  $\overline{WE}$  pulse in the program or erase command sequence.

During the Automatic Program algorithm, the device outputs on Q7 the complement of the datum programmed to Q7. This Q7 status also applies to programming during Erase Suspend. When the Automatic Program algorithm is complete, the device outputs the datum programmed to Q7. The system must provide the program address to read valid status information on Q7.

During the Automatic Erase algorithm, Data Polling produces a "0" on Q7. When the Automatic Erase algorithm is complete, Data Polling produces a "1" on Q7. This is analogous to the complement/true datum output described for the Automatic Program algorithm: the erase function changes all the bits to "1" prior to this, the device outputs the "complement," or "0".

After an erase command sequence is written, if all sectors selected for erasing are protected, Data Polling on Q7 is active for approximately 100 us, then the device returns to reading array data.

When the system detects Q7 has changed from the complement to true data, it can read valid data at Q7-Q0 on the following read cycles. This is because Q7 may change asynchronously with Q0-Q6 while Output Enable ( $\overline{OE}$ ) is asserted low.

### **Q6: Toggle BIT I**

Toggle Bit I on Q6 indicates whether an Automatic Program or Erase algorithm is in progress or complete. Toggle Bit I may be read at any address, and is valid after the rising edge of the final  $\overline{WE}$  or  $\overline{CE}$ , whichever happens first pulse in the command sequence (prior to the program or erase operation).

During an Automatic Program or Erase algorithm operation, successive read cycles to any address cause Q6 to toggle. The system may use either  $\overline{OE}$  or  $\overline{CE}$  to control the read cycles. When the operation is complete, Q6 stops toggling.

Table 6 shows the outputs for Toggle Bit I on Q6.

### **Q5: Program/Erase Timing**

Q5 will indicate if the program or erase time has exceeded the specified limits (internal pulse count). Under these conditions Q5 will produce a "1". This time-out condition indicates that the program or erase cycle was not successfully completed. Data Polling and Toggle Bit are the only operating functions of the device under this condition.

If this time-out condition occurs during chip erase operation, it specifies that device is bad and it may not be reused. Write the Reset command sequence to the device, and then execute program or erase command sequence. This allows the system to continue to use the other active sectors in the device.

If this time-out condition occurs during the chip erase operation, it specifies that the entire chip is bad.

If this time-out condition occurs during the word programming operation, the word is bad and may not be reused, (other word are still functional and can be reused).

**ABSOLUTE MAXIMUM RATINGS**

Storage Temperature	
Plastic Packages . . . . .	-65°C to +150°C
Ambient Temperature	
with Power Applied. . . . .	-65°C to +125°C
Voltage with Respect to Ground	
VCC (Note 1) . . . . .	-0.5 V to +4.0 V
A9, $\overline{OE}$ , ACC and	
RESET (Note 2) . . . . .	-0.5 V to +12.5 V
All other pins (Note 1) . . . . .	-0.5 V to VCC +0.5 V
Output Short Circuit Current (Note 3) . . . . .	200 mA

## Notes:

1. Minimum DC voltage on input or I/O pins is -0.5 V. During voltage transitions, input or I/O pins may overshoot VSS to -2.0 V for periods of up to 20 ns. See Figure 6. Maximum DC voltage on input or I/O pins is VCC +0.5 V. During voltage transitions, input or I/O pins may overshoot to VCC +2.0 V for periods up to 20 ns. See Figure 7.
2. Minimum DC input voltage on pins A9,  $\overline{OE}$ , ACC and RESET is -0.5 V. During voltage transitions, A9,  $\overline{OE}$ , ACC and RESET may overshoot VSS to -2.0 V for periods of up to 20 ns. See Figure 6. Maximum DC input voltage on pin A9 is +12.5 V which may overshoot to 14.0 V for periods up to 20 ns.
3. No more than one output may be shorted to ground at a time. Duration of the short circuit should not be greater than one second.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this data sheet is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

**OPERATING RATINGS****Commercial (C) Devices**Ambient Temperature (T<sub>A</sub>) . . . . . 0°C to +70°C**Industrial (I) Devices**Ambient Temperature (T<sub>A</sub>) . . . . . -40°C to +85°C**V<sub>CC</sub> Supply Voltages**V<sub>CC</sub> for full voltage range . . . . . +3.0V to +3.6 V

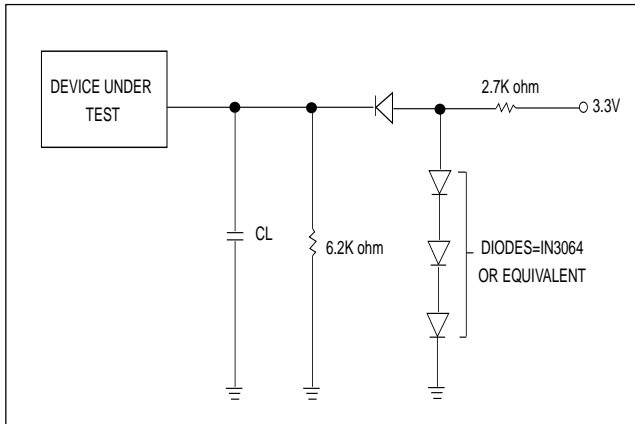
Operating ranges define those limits between which the functionality of the device is guaranteed.

**DC CHARACTERISTICS TA=0°C to 70°C, VCC=3.0V~3.6V**

Parameter	Description	Test Conditions	V <sub>I/O</sub> =3.0V~3.6V			V <sub>I/O</sub> =1.65V~2.9V			Unit
			Min	Typ	Max	Min	Typ	Max	
I <sub>LI</sub>	Input Load Current (Note 1)	V <sub>IN</sub> = V <sub>SS</sub> to V <sub>CC</sub> , V <sub>CC</sub> = V <sub>CC</sub> max			±1.0			±1.0	uA
I <sub>LIT</sub>	A9 Input Load Current	V <sub>CC</sub> =V <sub>CC</sub> max; A9 = 12.5V			80			80	uA
I <sub>LO</sub>	Output Leakage Current	V <sub>OUT</sub> = V <sub>SS</sub> to V <sub>CC</sub> , V <sub>CC</sub> = V <sub>CC</sub> max			±1.0			±1.0	uA
ICC1	VCC Active Read Current (Notes1, 2)	$\overline{CE}$ =V <sub>IL</sub> , $\overline{OE}$ = V <sub>IH</sub> 5 MHz		17	25		17	25	mA
				4	7		4	7	mA
ICC2	VCC Active Write Current (Notes 1, 3, 4)	$\overline{CE}$ =V <sub>IL</sub> , $\overline{OE}$ = V <sub>IH</sub>		26	30		26	30	mA
ICC3	VCC Standby Current (CMOS) (Note 1)	$\overline{CE}$ , $\overline{RESET}$ , ACC=V <sub>CC</sub> ± 0.3V		30	100		30	100	uA
ICC4	VCC Standby Current (TTL) (Note 1)	$\overline{CE}$ =V <sub>IH</sub>		0.5	1		0.5	1.8	mA
ICC5	VCC Reset Current (Note 1)	$\overline{RESET}$ = V <sub>SS</sub> ± 0.3 V, ACC = V <sub>CC</sub> ± 0.3 V		0.2	5		0.2	5	uA
IACC	ACC Accelerated Program Current, Word	$\overline{CE}$ =V <sub>IL</sub> , $\overline{OE}$ =V <sub>IH</sub> ACC pin		5	10		5	10	mA
		VCC pin		15	30		15	30	mA
V <sub>IL</sub>	Input Low Voltage		-0.5		0.8			0.4	V
V <sub>IH</sub>	Input High Voltage		0.7xV <sub>cc</sub>		V <sub>cc</sub> +0.3	V <sub>I/O</sub> -0.4			V
V <sub>HH</sub>	Voltage for ACC Program Acceleration	V <sub>CC</sub> = 3.0 V ± 10%	11.5		12.5	11.5		12.5	V
V <sub>ID</sub>	Voltage for Autoselect	V <sub>CC</sub> = 3.0 V ± 10%	11.5		12.5	11.5		12.5	V
V <sub>OL</sub>	Output Low Voltage	I <sub>OL</sub> = 4.0mA, V <sub>CC</sub> =V <sub>CC</sub> min			0.45			0.45	V
VOH1	Output High Voltage	I <sub>OH</sub> =-2.0mA, V <sub>CC</sub> =V <sub>CC</sub> min	0.85V <sub>I/O</sub>			0.85V <sub>I/O</sub>			V
VOH2		I <sub>OH</sub> =-100uA, V <sub>CC</sub> =V <sub>CC</sub> min	V <sub>I/O</sub> -0.4			V <sub>I/O</sub> -0.4			V
VLKO	Low VCC Lock-Out Voltage (Note 4)		2.3		2.5	2.3		2.5	V

**Notes:**

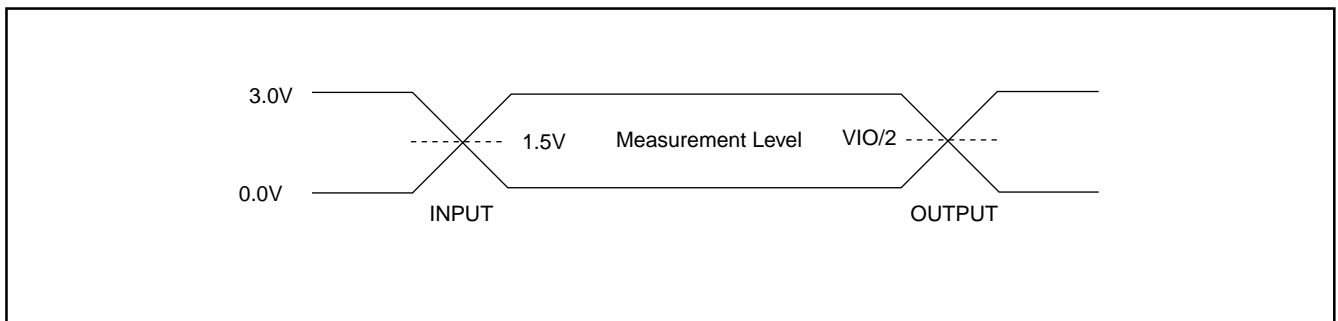
1. Maximum ICC specifications are tested with V<sub>CC</sub> = V<sub>CC</sub>max.
2. Typical specifications are for V<sub>CC</sub> = 3.0 V.
3. ICC active while Embedded Erase or Embedded Program is in progress.
4. Not 100% tested.

**SWITCHING TEST CIRCUITS**

**TEST SPECIFICATIONS**

Test Condition	90ns	100ns	120ns	Unit
Output Load	1 TTL gate			
Output Load Capacitance, CL (including jig capacitance)	30	30	100	pF
Input Rise and Fall Times	5			ns
Input Pulse Levels	0.0-3.0			V
Input timing measurement reference levels	1.5			V
Output timing measurement reference levels	1.5			V

**KEY TO SWITCHING WAVEFORMS**

WAVEFORM	INPUTS	OUTPUTS
	Steady	
	Changing from H to L	
	Changing from L to H	
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High Impedance State (High Z)

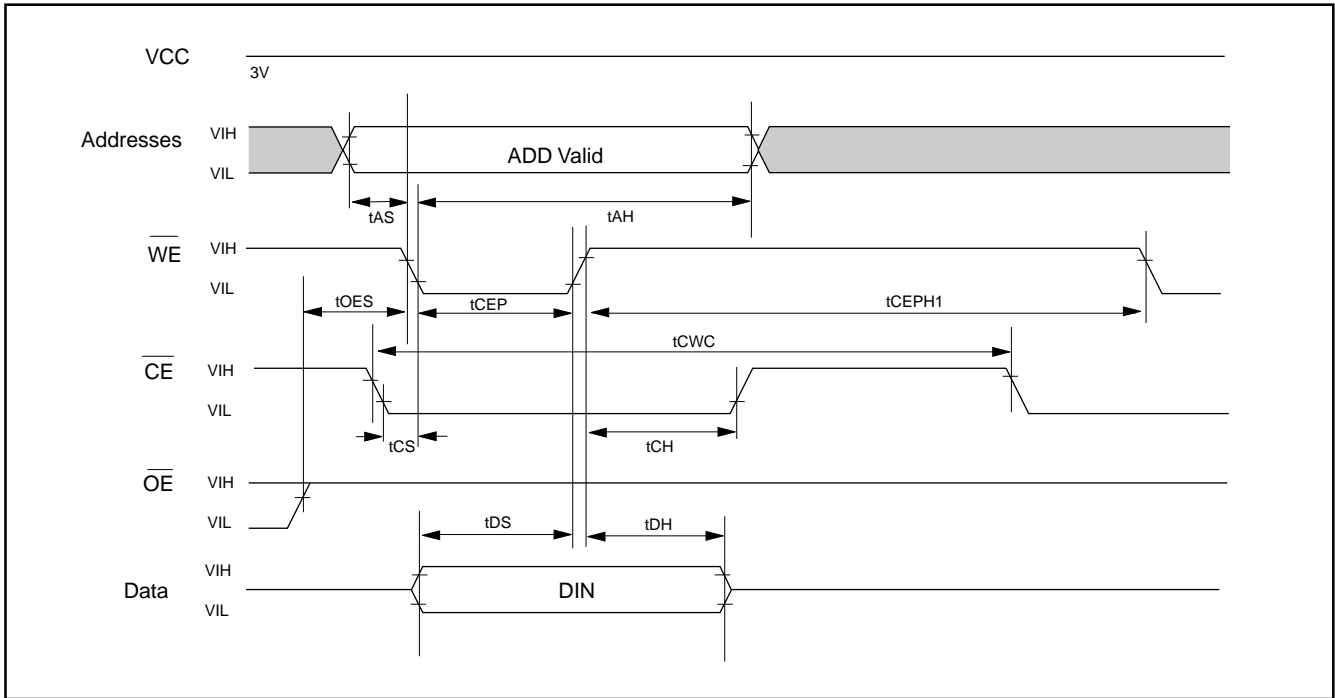
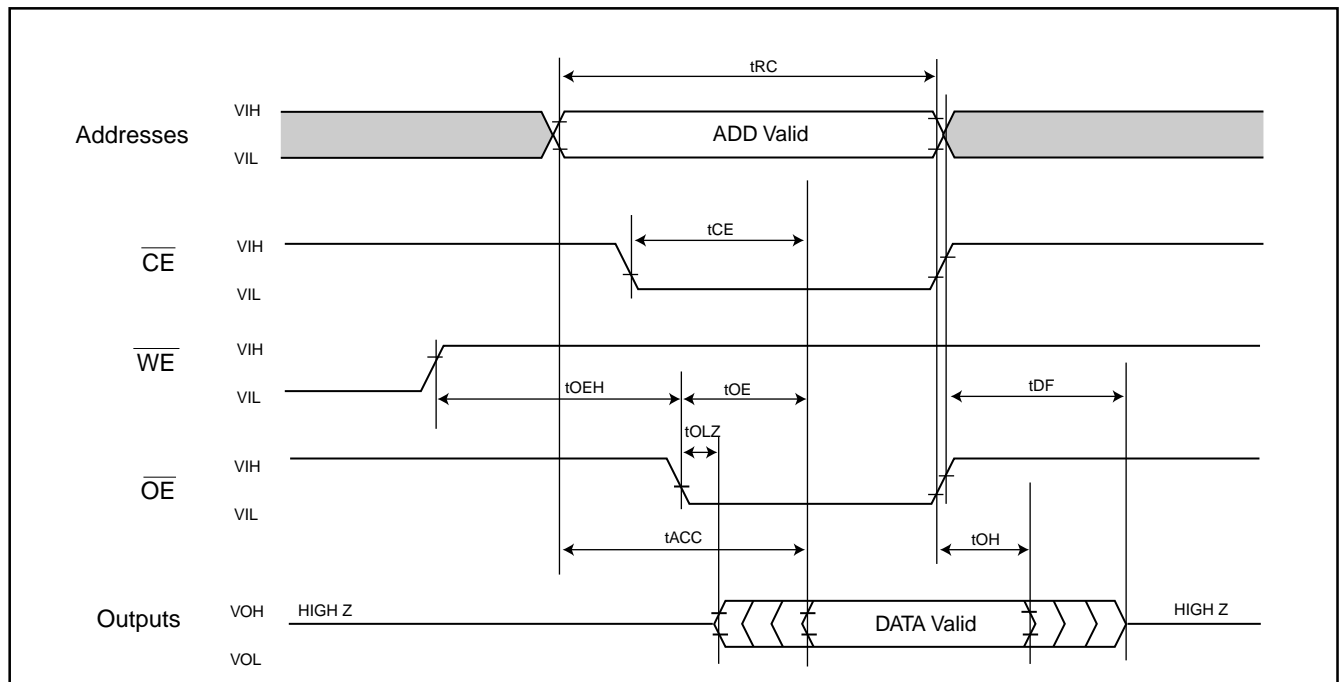
**SWITCHING TEST WAVEFORMS**




**AC CHARACTERISTICS TA=0°C to 70°C, VCC=3.0V~3.6V**

Symbol	DESCRIPTION	CONDITION	90ns	100ns	120ns	Unit	
tACC	Address to output delay	$\overline{CE}=VIL$ $\overline{OE}=VIL$	MAX	90	100	120	ns
tCE	Chip enable to output delay	$\overline{OE}=VIL$	MAX	90	100	120	ns
tOE	Output enable to output delay		MAX	34	34	44	ns
tDF	$\overline{OE}$ High to output float(Note1)		MAX	25	25	35	ns
tOH	Output hold time of from the rising edge of Address, $\overline{CE}$ , or $\overline{OE}$ , whichever happens first		MIN	0	0	0	ns
tRC	Read cycle time (Note 1)		MIN	90	100	120	ns
tWC	Write cycle time (Note 1)		MIN	90	100	120	ns
tCWC	Command write cycle time(Note 1)		MIN	90	100	120	ns
tAS	Address setup time		MIN	0	0	0	ns
tAH	Address hold time		MIN	45	45	50	ns
tDS	Data setup time		MIN	45	45	50	ns
tDH	Data hold time		MIN	0	0	0	ns
tVCS	VCC setup time(Note 1)		MIN	50	50	50	us
tCS	Chip enable setup time		MIN	0	0	0	ns
tCH	Chip enable hold time		MIN	0	0	0	ns
tOES	Output enable setup time (Note 1)		MIN	0	0	0	ns
tOEH	Output enable hold time (Note 1)	Read	MIN	0	0	0	ns
		Toggle & Data Polling	MIN	10	10	10	ns
tWES	$\overline{WE}$ setup time		MIN	0	0	0	ns
tWEH	$\overline{WE}$ hold time		MIN	0	0	0	ns
tCEP	$\overline{CE}$ pulse width		MIN	45	45	50	ns
tCEPH	$\overline{CE}$ pulse width high		MIN	30	30	30	ns
tWP	$\overline{WE}$ pulse width		MIN	35	35	50	ns
tWPH	$\overline{WE}$ pulse width high		MIN	30	30	30	ns
tOLZ	Output enable to output low Z		MAX	30	30	40	ns
tWHGL	$\overline{WE}$ high to $\overline{OE}$ going low		MIN	30	30	30	ns
tWHWH1	Word Programming Operation (Note 3)		TYP	11	11	11	us
tWHWH1	Accelerated Word Programming Operation(Note3)		TYP	7	7	7	us
tWHWH2	Chip Erase Operation (Note3)		TYP	150	150	150	sec

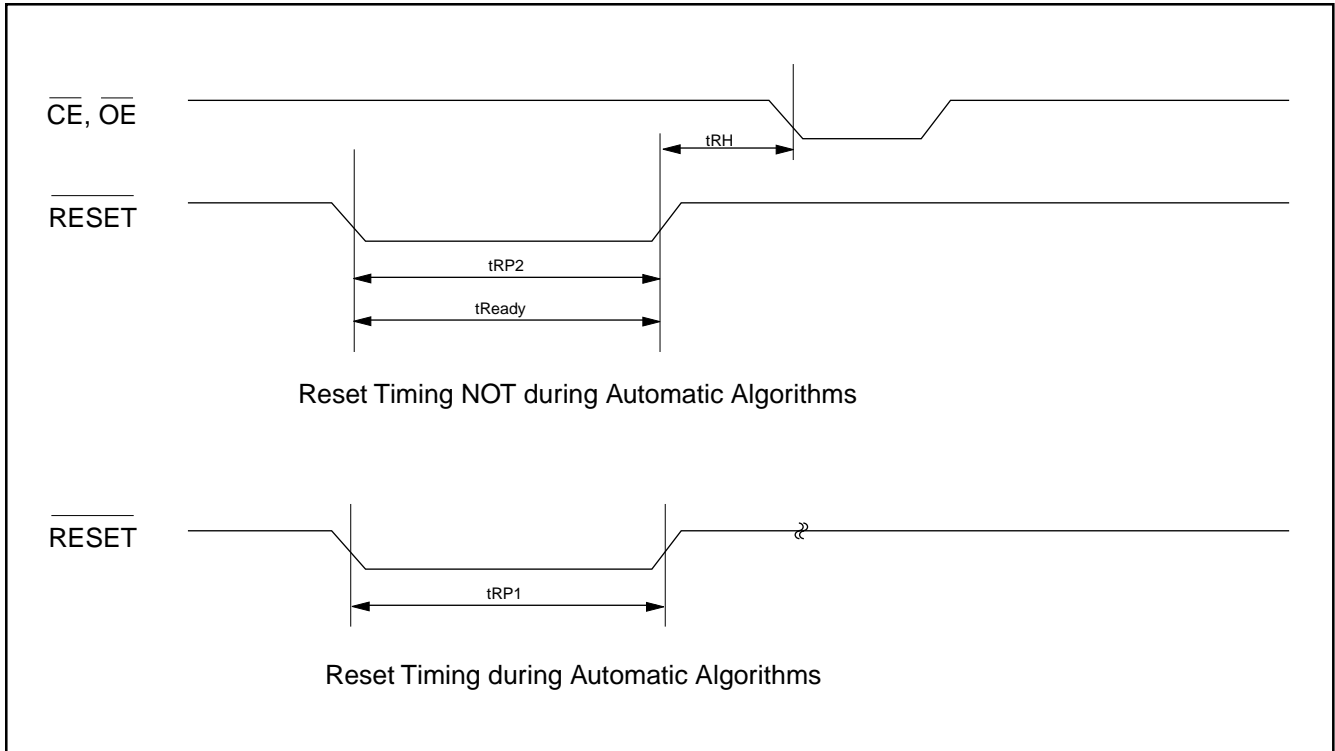
Note: 1. Not 100% Tested  
 2.  $t_r = t_f = 5ns$   
 3. See the "Erase and Program Performance" section for more information.

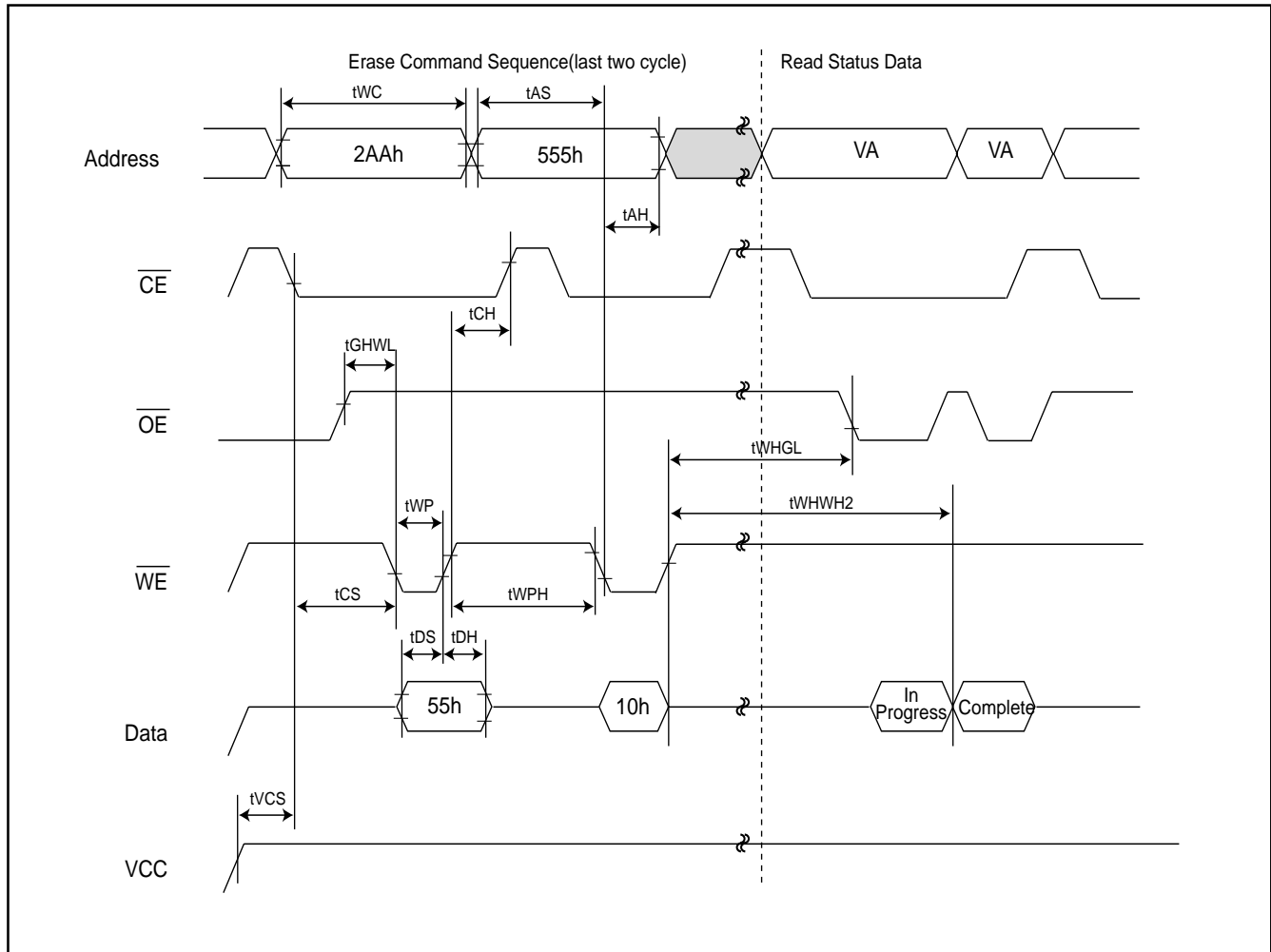
**Fig 1. COMMAND WRITE OPERATION**

**READ/RESET OPERATION**
**Fig 2. READ TIMING WAVEFORMS**


**AC CHARACTERISTICS TA=0°C to 70°C, VCC=3.0V~3.6V**

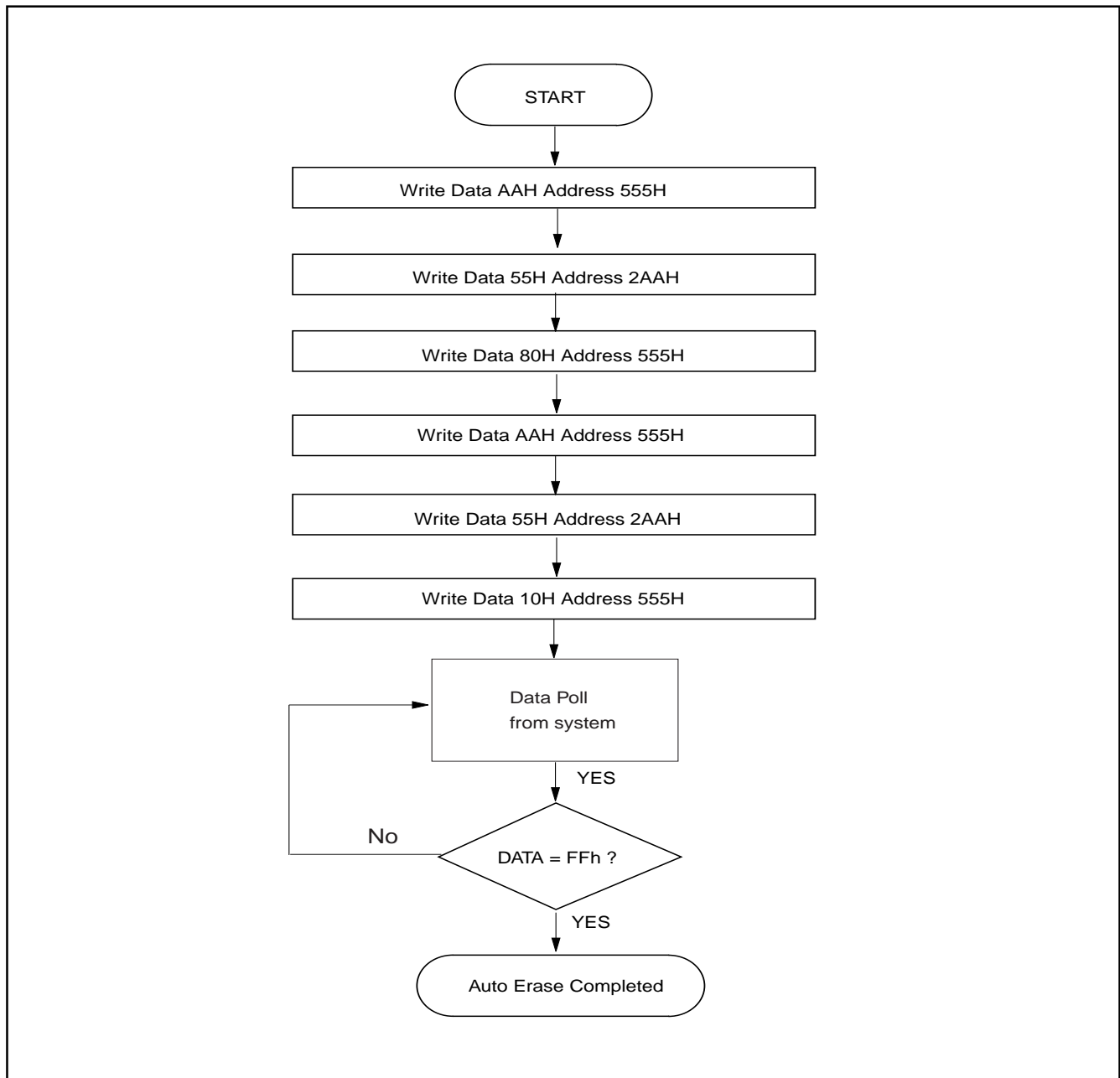
Parameter	Description	Test Setup	All Speed Options	Unit
tREADY	RESET PIN Low (NOT During Automatic Algorithms) to Read or Write (See Note)	MAX	500	ns
tRP1	RESET Pulse Width (During Automatic Algorithms)	MIN	10	us
tRP2	RESET Pulse Width (NOT During Automatic Algorithms)	MIN	500	ns
tRH	RESET High Time Before Read (See Note)	MIN	50	ns

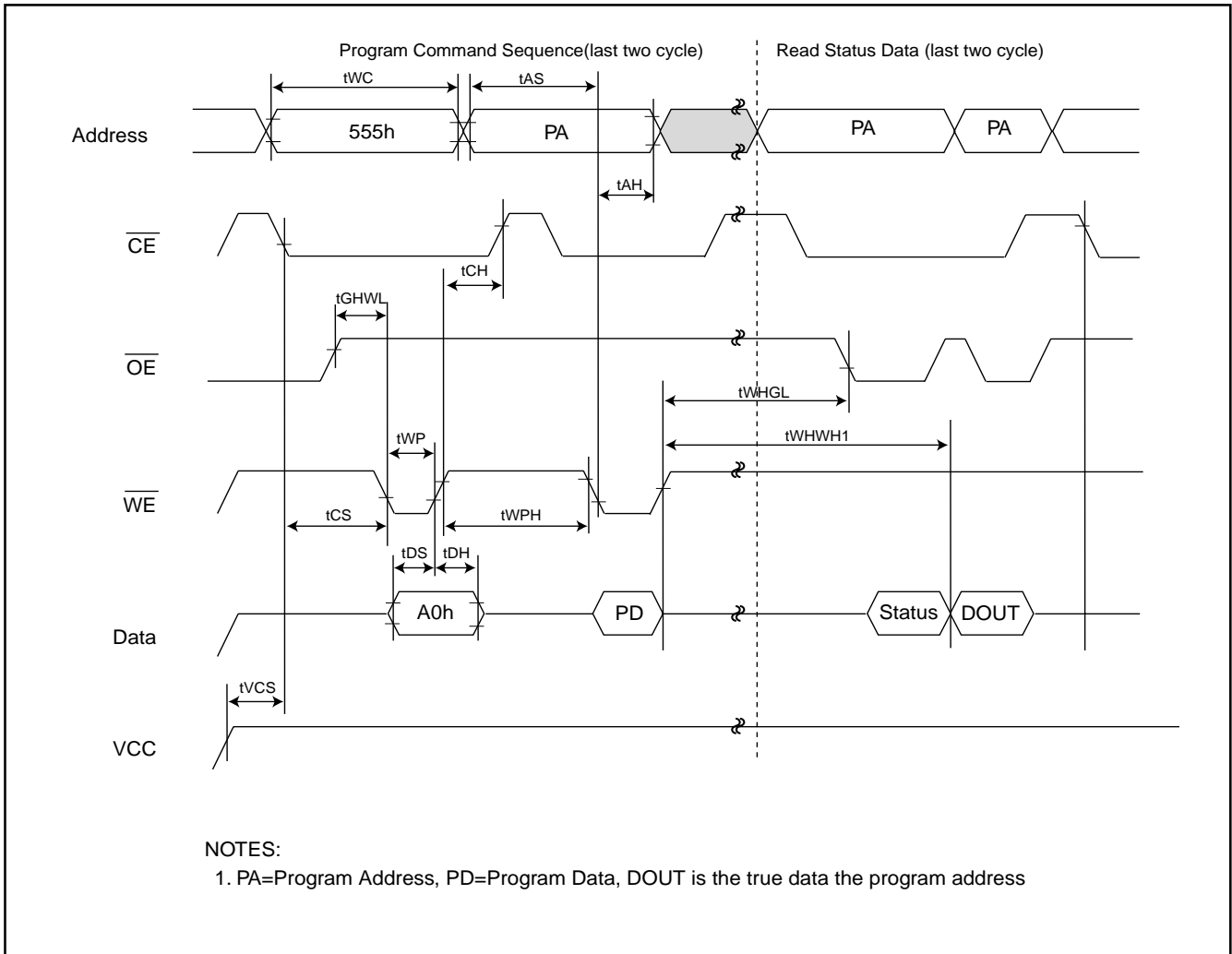
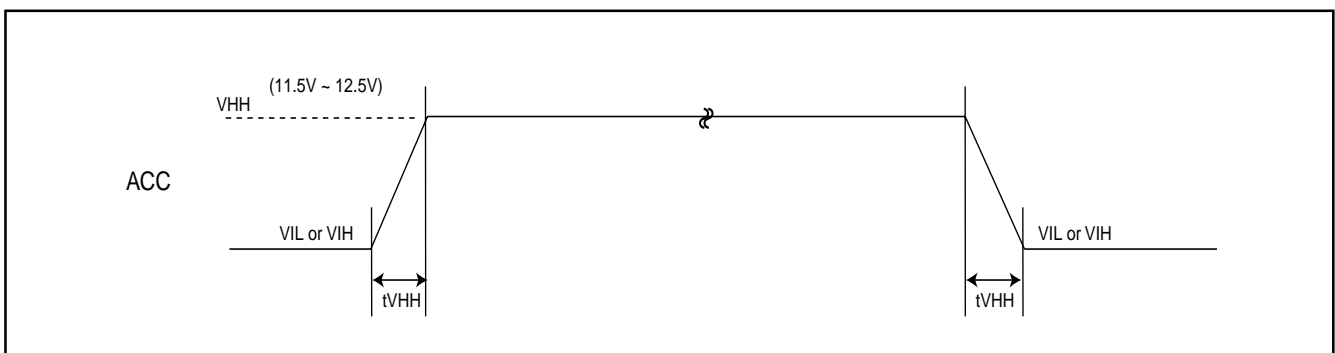
Note:Not 100% tested

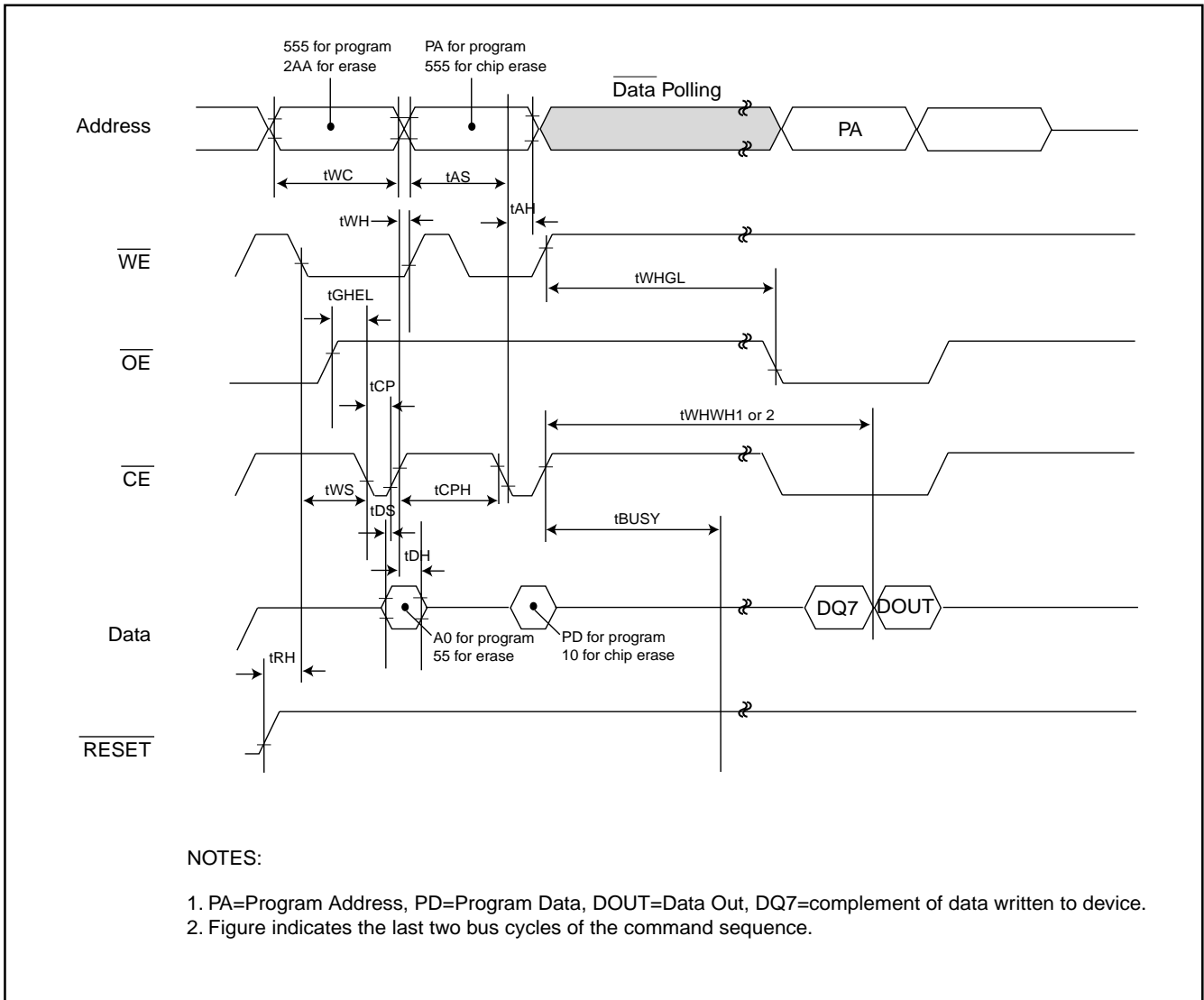
**Fig 3. RESET TIMING WAVEFORM**


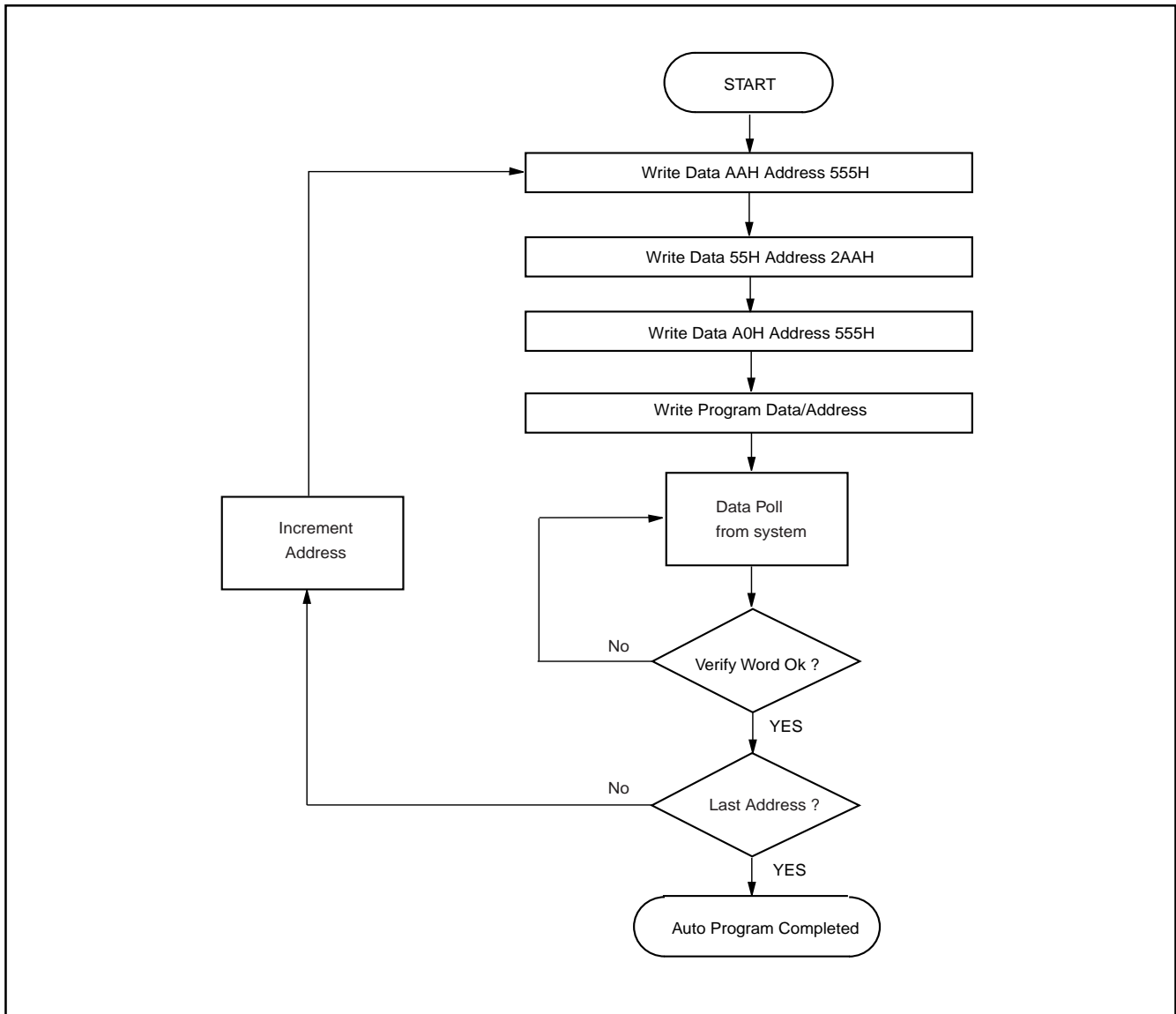
**ERASE/PROGRAM OPERATION**
**Fig 4. AUTOMATIC CHIP ERASE TIMING WAVEFORM**

**Notes:**

1. VA = Valid Address for reading status data (see "Write Operation Status").

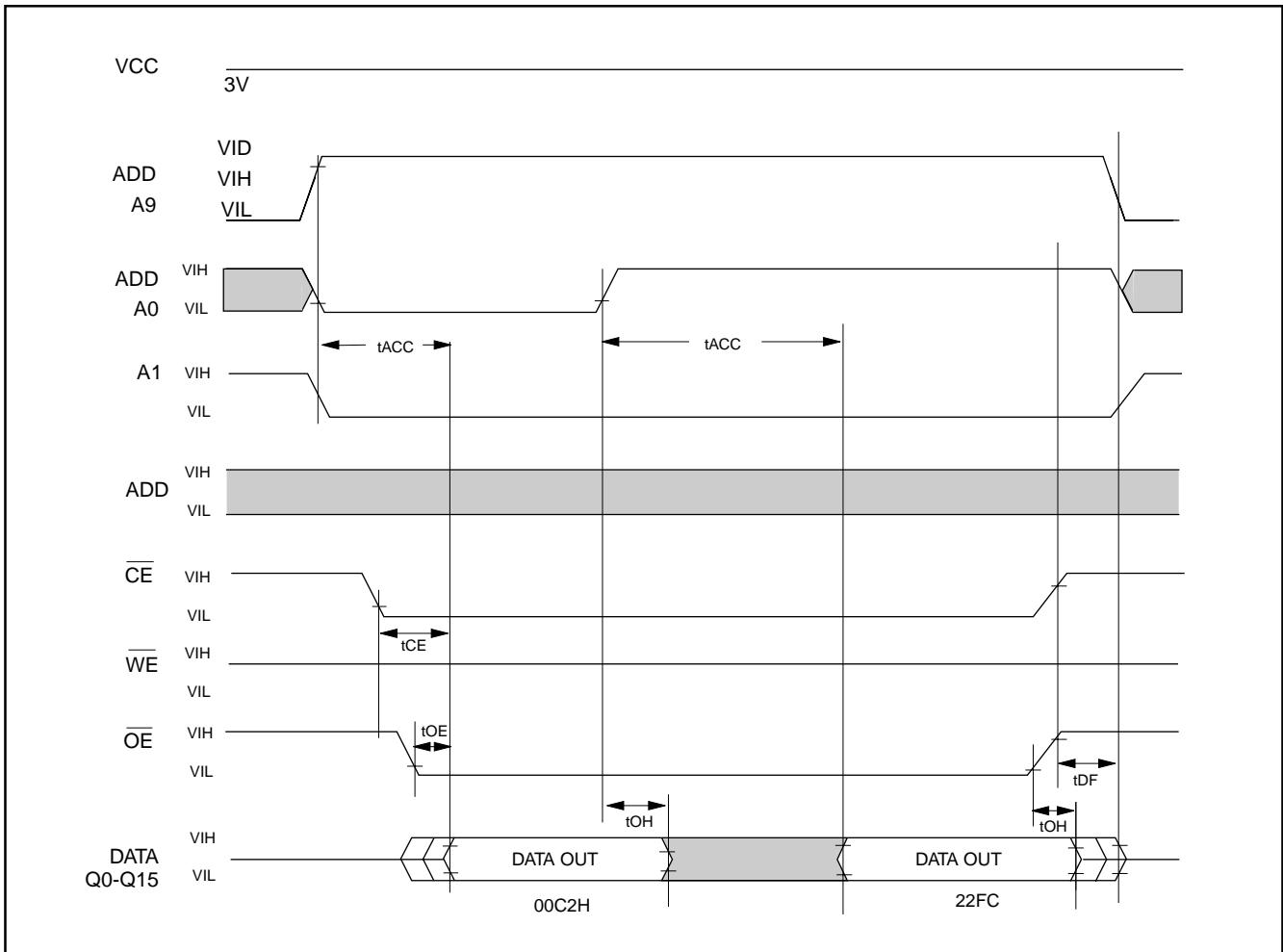
**Fig 5. AUTOMATIC CHIP ERASE ALGORITHM FLOWCHART**

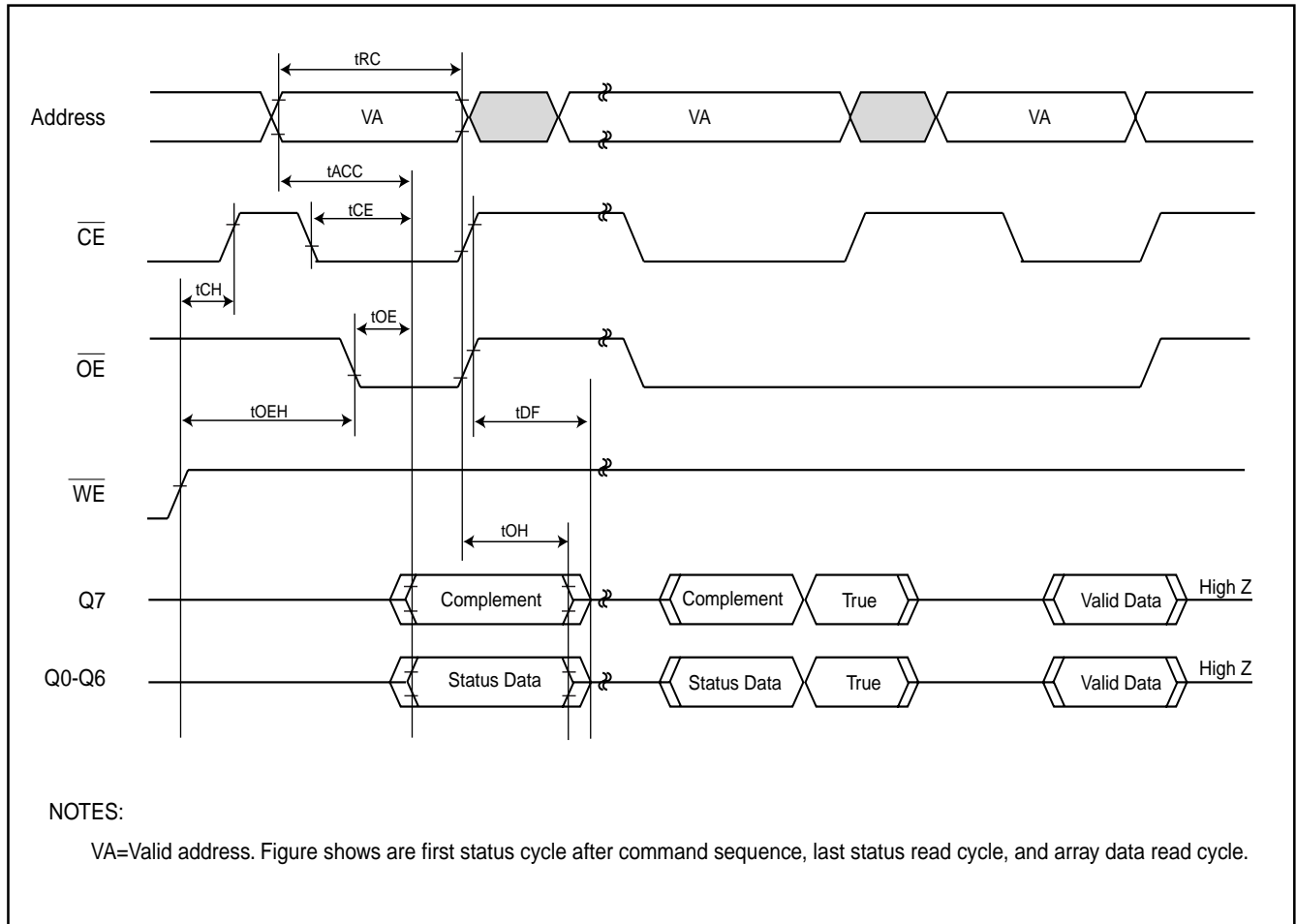
**Fig 6. AUTOMATIC PROGRAM TIMING WAVEFORMS**

**Fig 7. ACCELERATED PROGRAM TIMING DIAGRAM**


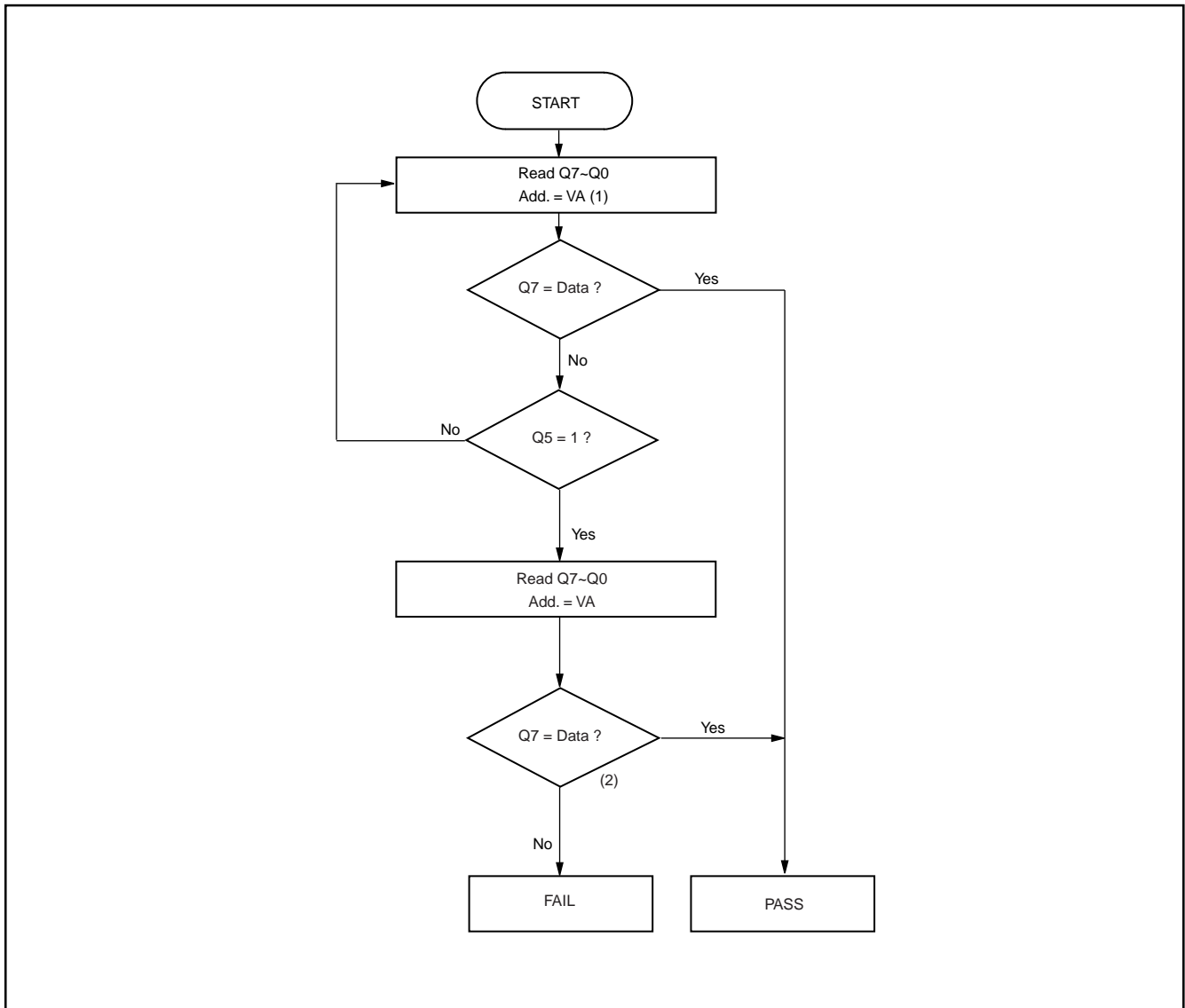
**Fig 8.  $\overline{CE}$  CONTROLLED PROGRAM TIMING WAVEFORM**


**Fig 9. AUTOMATIC PROGRAMMING ALGORITHM FLOWCHART**



**Fig 10. SILICON ID READ TIMING WAVEFORM**


**WRITE OPERATION STATUS**
**Fig 11. DATA POLLING TIMING WAVEFORMS (DURING AUTOMATIC ALGORITHMS)**


**Fig 12. DATA POLLING ALGORITHM**

**Notes:**

1. VA=valid address for programming.
2. Q7 should be rechecked even Q5="1" because Q7 may change simultaneously with Q5.

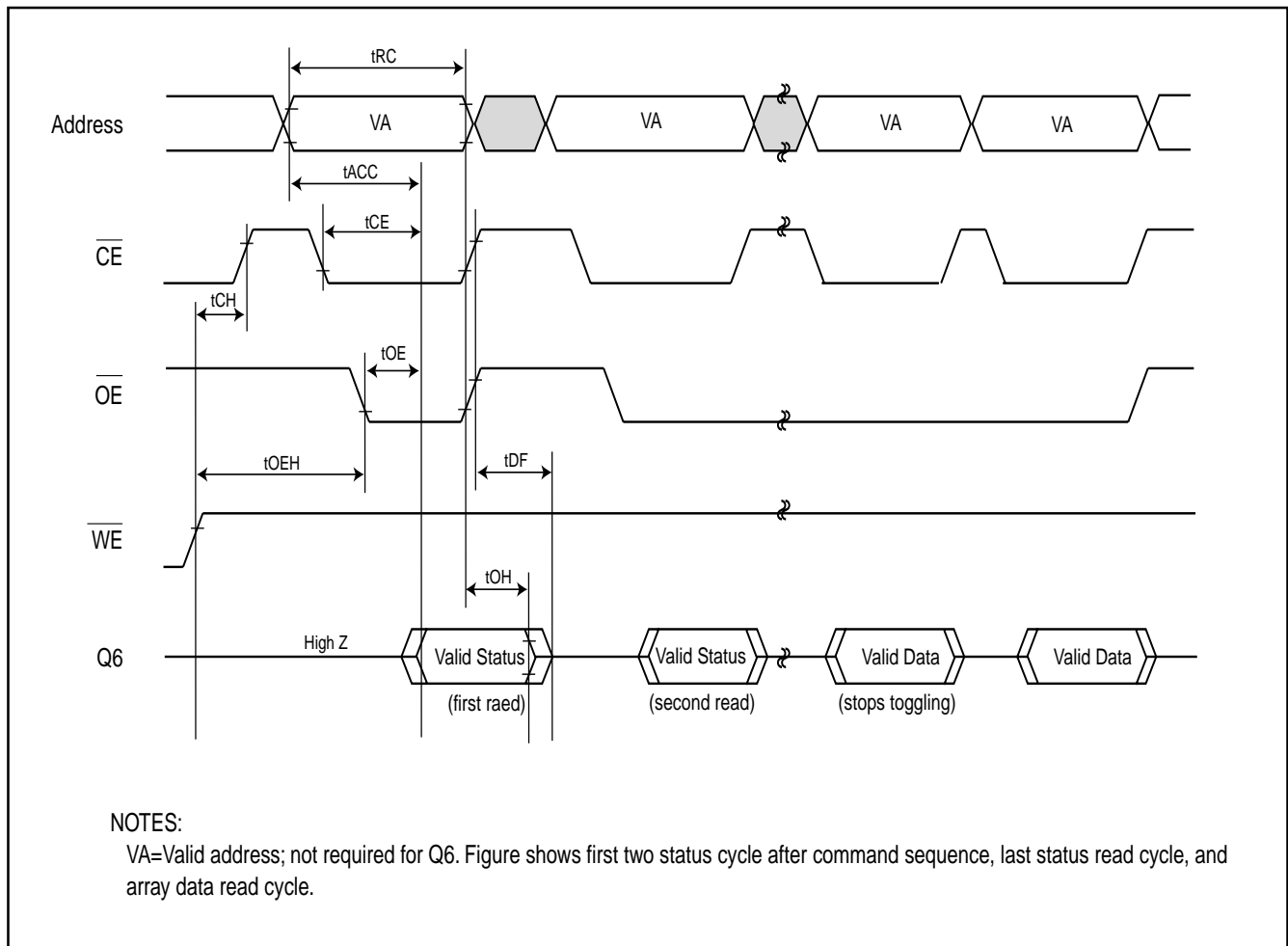
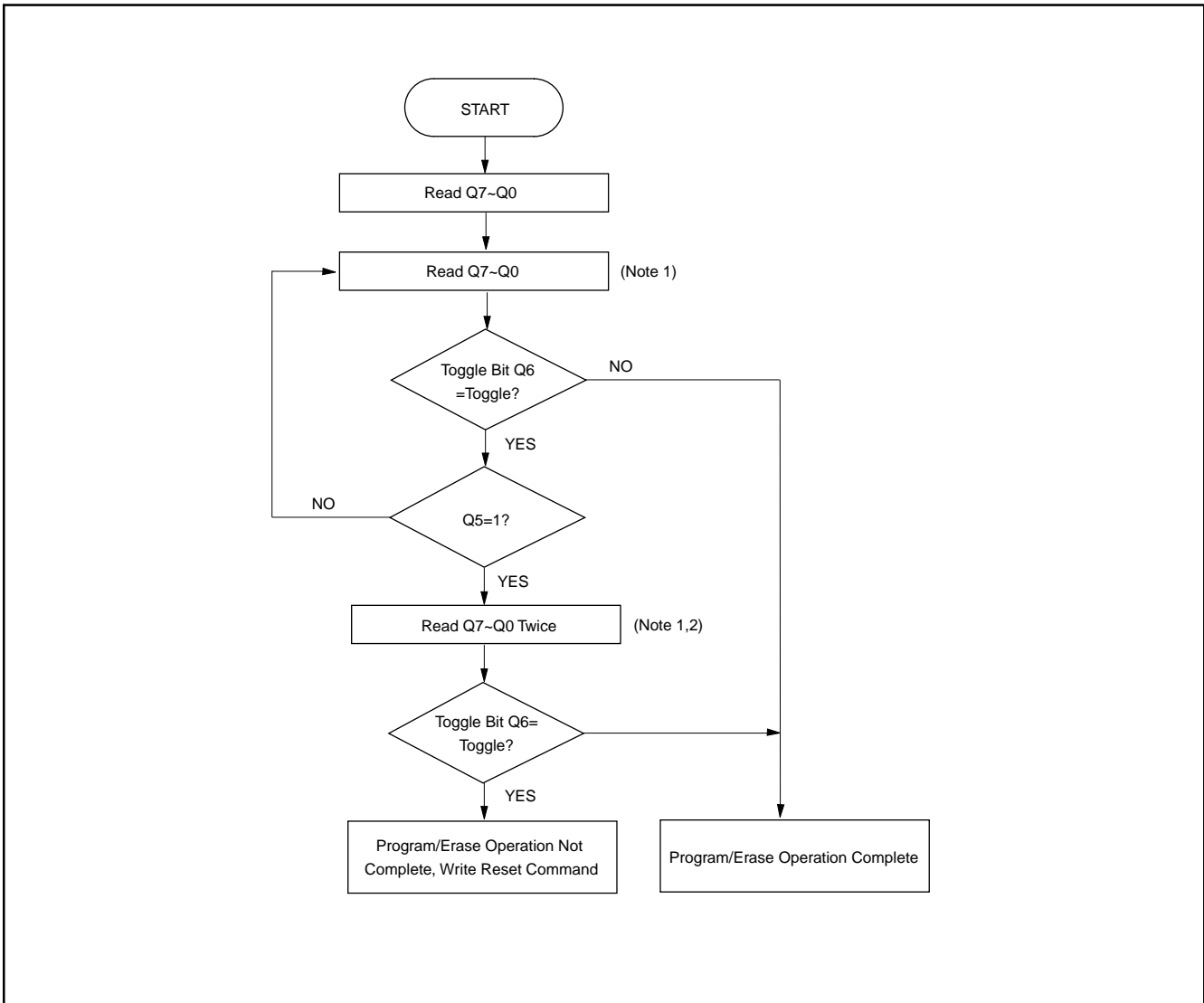
**Fig 13. TOGGLE BIT TIMING WAVEFORMS (DURING AUTOMATIC ALGORITHMS)**


Fig 14. TOGGLE BIT ALGORITHM



Note:

1. Read toggle bit twice to determine whether or not it is toggling.
2. Recheck toggle bit because it may stop toggling as Q5 changes to "1".

**ERASE AND PROGRAMMING PERFORMANCE (1)**

PARAMETER	LIMITS			UNITS
	MIN.	TYP.(2)	MAX.	
Chip Erase Time		230	650	sec
Word Programming Time		48	400	us
Chip Programming Time		210	360	sec
Accelerated Chip Erase Time		190	420	sec
Accelerated Word Program Time		47	256	us
Accelerated Chip Program Time		200	300	sec
Erase/Program Cycles	100			Cycles

Note: 1. Not 100% Tested, Excludes external system level over head.  
 2. Typical values measured at 25°C,3.3V. Additionally programming typically assume checkerboard pattern.

**LATCH-UP CHARACTERISTICS**

	MIN.	MAX.
Input Voltage with respect to GND on ACC, $\overline{OE}$ , $\overline{RESET}$ , A9	-1.0V	12.5V
Input Voltage with respect to GND on all power pins, Address pins, $\overline{CE}$ and $\overline{WE}$	-1.0V	2VCCmax
Input Voltage with respect to GND on all I/O pins	-1.0V	2VCCmax
Current	-100mA	+100mA
Includes all pins except VCC. Test conditions: VCC = 3.0V, one pin at a time.		

**CAPACITANCE TA=0°C to 70°C, VCC=3.0V~3.6V**

Parameter Symbol	Parameter Description	Test Set	TYP	MAX	UNIT
CIN	Input Capacitance	VIN=0	6	7.5	pF
COUT	Output Capacitance	VOUT=0	8.5	12	pF
CIN2	Control Pin Capacitance	VIN=0	7.5	9	pF

**Notes:**

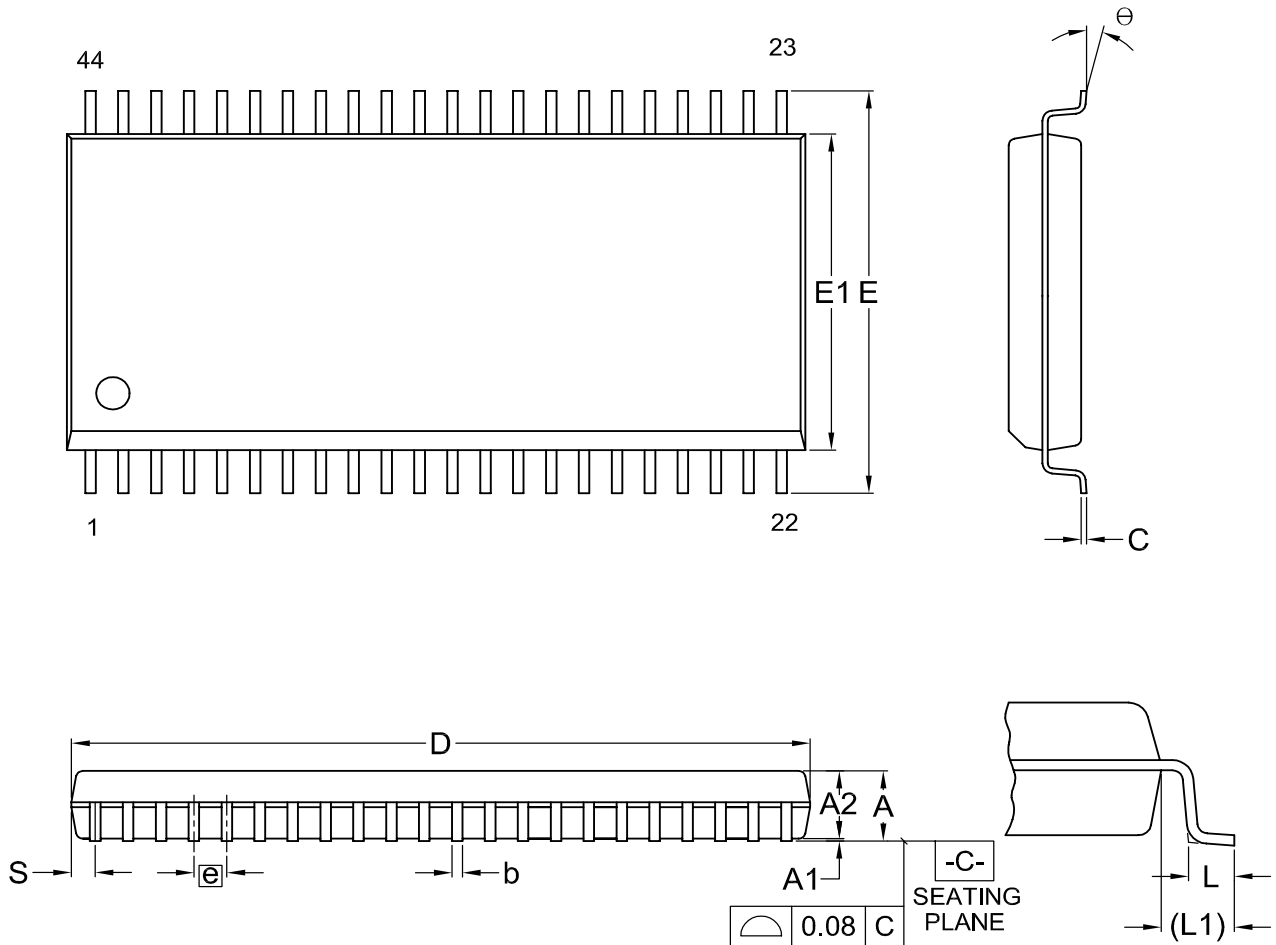
1. Sampled, not 100% tested.
2. Test conditions TA=25°C, f=1.0MHz

**DATA RETENTION**

Parameter	Test Conditions	Min	Unit
Minimum Pattern Data Retention Time	150	10	Years
	125	20	Years

**ORDERING INFORMATION****PLASTIC PACKAGE**

<b>PART NO.</b>	<b>ACCESS TIME (ns)</b>	<b>Temperature Range</b>	<b>Package type</b>
MX26L6420MC-90	90	Commercial	44 pin SOP
MX26L6420MC-10	100	Commercial	44 pin SOP
MX26L6420MC-12	120	Commercial	44 pin SOP
MX26L6420TC-90	90	Commercial	48 pin TSOP (Normal Type)
MX26L6420TC-10	100	Commercial	48 pin TSOP (Normal Type)
MX26L6420TC-12	120	Commercial	48 pin TSOP (Normal Type)

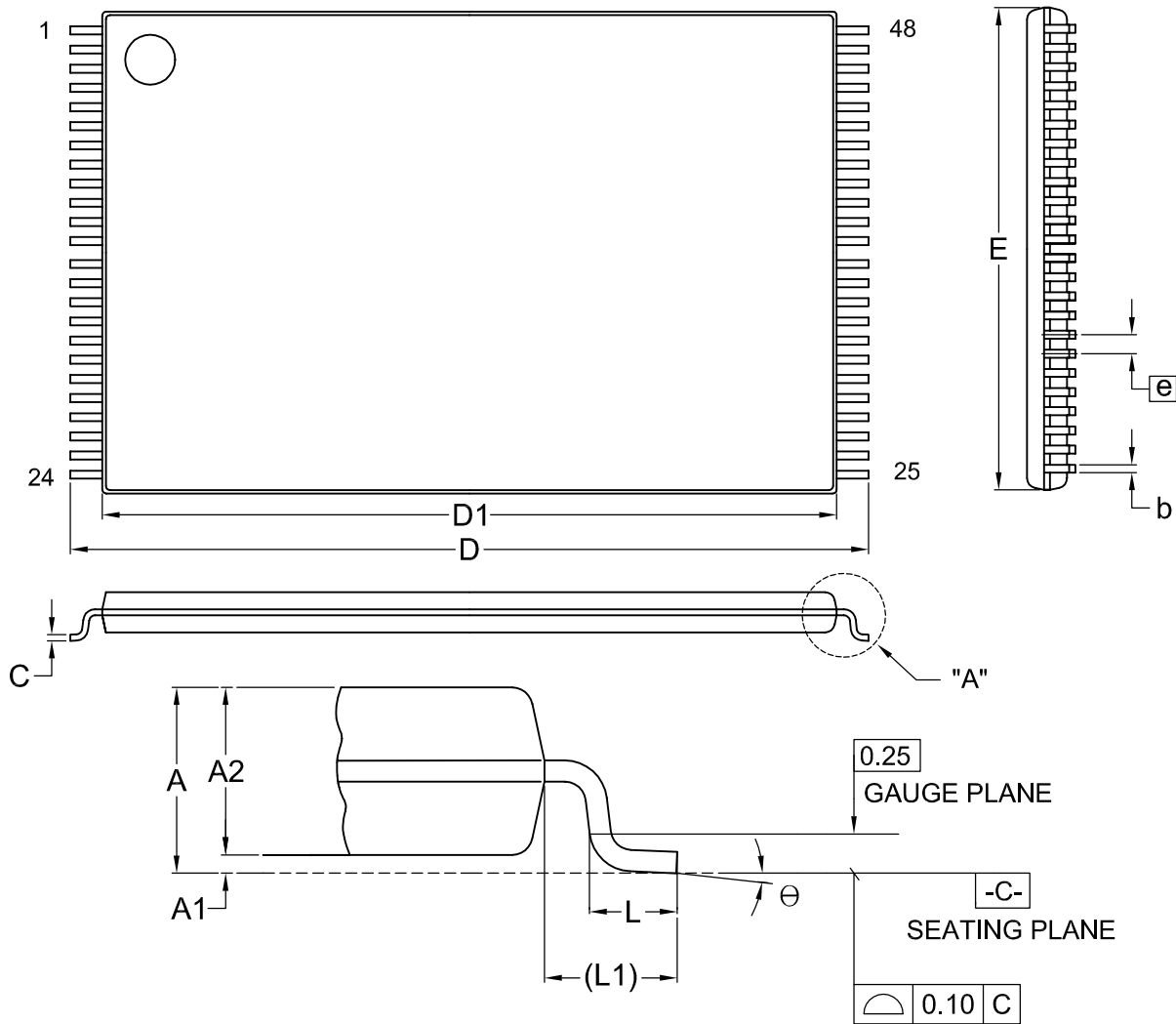
**PACKAGE INFORMATION**
**Title: Package Outline for SOP 44L (500MIL)**


Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL		A	A1	A2	b	C	D	E	E1	e	L	L1	S	$\theta$
UNIT														
mm	Min.	---	0.10	2.59	0.36	0.15	28.37	15.83	12.47		0.56	1.51	0.78	0
	Nom.	---	0.15	2.69	0.41	0.20	28.50	16.03	12.60	1.27	0.76	1.71	0.91	5
	Max.	3.00	0.20	2.80	0.51	0.25	28.63	16.23	12.73		0.96	1.91	1.04	10
Inch	Min.	---	0.004	0.102	0.014	0.006	1.117	0.623	0.491		0.022	0.059	0.031	0
	Nom.	---	0.006	0.106	0.016	0.008	1.122	0.631	0.496	0.050	0.030	0.067	0.036	5
	Max.	0.118	0.008	0.110	0.020	0.010	1.127	0.639	0.501		0.038	0.075	0.041	10

DWG.NO.	REVISION	REFERENCE			ISSUE DATE
		JEDEC	EIAJ		
6110-1405	5	MO-175			09-24-'02



**Title: Package Outline for TSOP(I) 48L (12X20mm)NORMAL FORM**

DETAIL "A"

Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL		A	A1	A2	b	C	D	D1	E	e	L	L1	θ
UNIT													
mm	Min.	---	0.05	0.95	0.17	0.10	19.80	18.30	11.90		0.50	0.70	0
	Nom.	---	0.10	1.00	0.20	0.13	20.00	18.40	12.00	0.50	0.60	0.80	5
	Max.	1.20	0.15	1.05	0.27	0.21	20.20	18.50	12.10		0.70	0.90	8
Inch	Min.	---	0.002	0.037	0.007	0.004	0.780	0.720	0.469		0.020	0.028	0
	Nom.	---	0.004	0.039	0.008	0.005	0.787	0.724	0.472	0.020	0.024	0.031	5
	Max.	0.047	0.006	0.041	0.011	0.008	0.795	0.728	0.476		0.028	0.035	8

DWG.NO.	REVISION	REFERENCE			ISSUE DATE
		JEDEC	EIAJ		
6110-1607	6	MO-142			09-24-'02

**REVISION HISTORY**

<b>Revision No.</b>	<b>Description</b>	<b>Page</b>	<b>Date</b>
1.0	1. Removed Advanced Information from title	P1	JUL/01/2003
1.1	1. Revised Latch-up characteristics	P32	JUL/16/2003
	2. Corrected typing errors	P2,5,9,14,33	
1.2	1. Removed secured silicon sector function	P1,5,7~9,25,26	OCT/30/2003
	2. Revised latch-up characteristics	P30	
1.3	1. Added ACC into High-V pin definition	P14	JAN/07/2004
	2. Loosed A9 input load current from 35uA to 80uA	P15	
	3. Corrected VHH voltage from 8.5V~9.5V to 11.5V~12.5V	P22	
	4. Loosed erase and programming performance	P30	
	5. Recovered latch-up characteristics from VCC+1.0V to 2VCCmax	P30	



**MX26L6420**

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