

TYPES SN54AS2620, SN54AS2623, SN74AS2620, SN74AS2623 OCTAL BUS TRANSCEIVERS/MOS DRIVER

DECEMBER 1983

- Bidirectional Octal Bus Transceivers For Driving MOS Devices
- I/O Ports Have 25 Ohm Series Resistors So No External Resistors Are Required
- Local Bus-Latch Capability
- Choice of True or Inverting Logic
- Dependable Texas Instruments Quality and Reliability

description

These octal bus transceivers are designed to drive the capacitive input characteristics of MOS devices and allow asynchronous two-way communication between data buses. The control function implementation allows for maximum flexibility in timing.

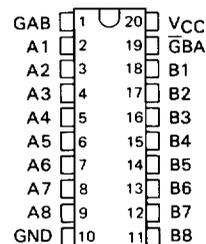
These devices allow data transmission from A bus to the B bus or from the B bus to the A bus depending upon the logic levels at the enable inputs ($\bar{G}BA$ and GAB).

The enable inputs can be used to disable the device so that the buses are effectively isolated.

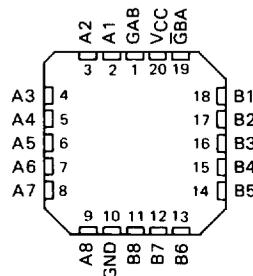
The dual-enable configuration gives the 'AS2620 or 'AS2623 the capability to store data by simultaneous enabling of $\bar{G}BA$ and GAB . Each output reinforces its input in this transceiver configuration. Thus, when both control inputs are enabled and all other data sources to the two sets of bus lines are at high impedance, both sets of bus lines (16 in all) will remain at their last states. The 8-bit codes appearing on the two sets of buses will be identical for the 'AS2623 or complementary for the 'AS2620.

The SN54AS2620 and SN54AS2623 are characterized for operation over the full military temperature range of -55°C to 125°C . The SN74AS2620 and SN74AS2623 are characterized for operation from 0°C to 70°C .

SN54AS' . . . J PACKAGE
SN74AS' . . . N PACKAGE
(TOP VIEW)



SN54AS' . . . FH PACKAGE
SN74AS' . . . FN PACKAGE
(TOP VIEW)



FUNCTION TABLE

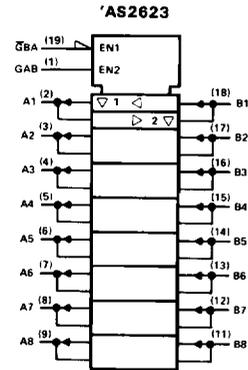
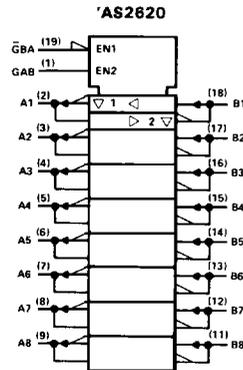
ENABLE INPUTS		OPERATION	
$\bar{G}BA$	GAB	'AS2620	'AS2623
L	L	\bar{B} data to A bus	B data to A bus
H	H	\bar{A} data to B bus	A data to B bus
H	L	Isolation	Isolation
L	H	\bar{B} data to A bus, \bar{A} data to B bus	B data to A bus, A data to B bus

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ALS AND AS CIRCUITS

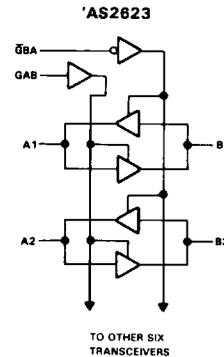
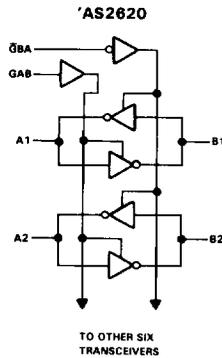
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logic symbols



Pin numbers shown are for J and N packages.

logic diagrams (positive logic)



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TYPES SN54AS2620, SN54AS2623, SN74AS2620, SN74AS2623
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AS2620 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V,}$ $C_L = 50 \text{ pF,}$ $R_1 = 500 \Omega,$ $R_2 = 500 \Omega,$ $T_A = \text{MIN to MAX}$				UNIT
			SN54AS2620		SN74AS2620		
			MIN	MAX	MIN	MAX	
t_{PLH}	A	B	1	9.5	1	8	ns
t_{PHL}			1	7.5	1	6.5	
t_{PLH}	B	A	1	9.5	1	8	ns
t_{PHL}			1	7.5	1	6.5	
t_{PZH}	$\bar{G}BA$	A	1	11	1	10	ns
t_{PZL}			1	12	1	11	
t_{PHZ}	$\bar{G}BA$	A	1	7.5	1	6	ns
t_{PLZ}			1	15	1	12	
t_{PZH}	GAB	B	1	9	1	8	ns
t_{PZL}			1	9	1	8	
t_{PHZ}	GAB	B	1	12	1	11	ns
t_{PLZ}			1	12	1	11	

AS2623 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V,}$ $C_L = 50 \text{ pF,}$ $R_1 = 500 \Omega,$ $R_2 = 500 \Omega,$ $T_A = \text{MIN to MAX}$				UNIT
			SN54AS2623		SN74AS2623		
			MIN	MAX	MIN	MAX	
t_{PLH}	A	B	1	9.5	1	8.5	ns
t_{PHL}			1	8.5	1	7.5	
t_{PLH}	B	A	1	10	1	9	ns
t_{PHL}			1	9	1	7.5	
t_{PZH}	$\bar{G}BA$	A	1	12.5	1	11	ns
t_{PZL}			1	12	1	11	
t_{PHZ}	$\bar{G}BA$	A	1	8.5	1	7.5	ns
t_{PLZ}			1	13	1	12	
t_{PZH}	GAB	B	1	13	1	12	ns
t_{PZL}			1	13.5	1	12	
t_{PHZ}	GAB	B	1	7.5	1	7	ns
t_{PLZ}			1	14.5	1	12.5	

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

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