FEATURES

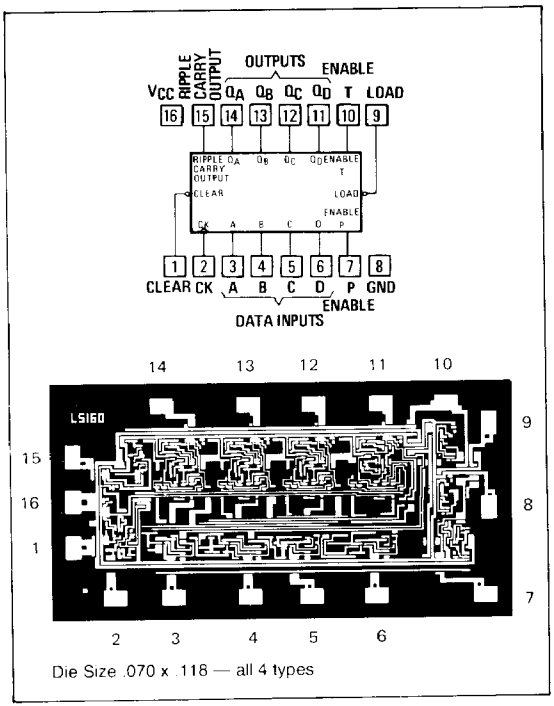
- 4-bit synchronous counters
- Synchronously programmable
- Internal look-ahead counting
- Carry output for n-bit cascading
- Synchronous or asynchronous clear
- Advanced low-power Schottky technology
- 100% reliability assurance testing in compliance with MIL-STD-883
- Higher speed compared to 9LS/54LS and 9LS/74LS
- 8mA sink current over full military temperature range
- 50mV improved V_{OL} compared to 9LS/74LS
- 440μA source current

DESCRIPTION

The 25LS160, 25LS161, 25LS162 and 25LS163 synchronous, presettable counts have internal look-ahead carry and ripple carry output for high-speed counting applications. The 25LS160 and 25LS162 are decade counters and the 25LS161 and 25LS163 are 4-bit binary counters. Counting or loading occurs on the positive transition of the clock pulse. A LOW level on the load input causes the data on the A, B, C and D inputs to be shifted to the appropriate Q outputs on the next positive clock transition.

The 25LS160 and 25LS161 feature an asynchronous clear. A LOW level at the clear input sets the Q outputs LOW regardless of the other inputs. The 25LS162 and 25LS163 have a synchronous clear. A LOW level at the clear input sets the Q outputs LOW after the next positive clock transition regardless of the enable inputs.

PIN-OUT DIAGRAM



Die Size .070 x .118 — all 4 types

Both count-enable inputs P and T must be HIGH to count. Count enable T is included in the ripple carry output gate for cascading connection.

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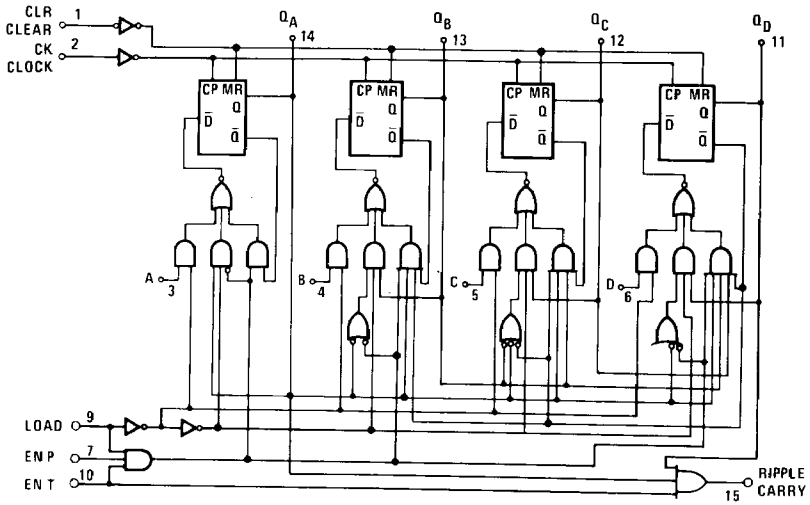
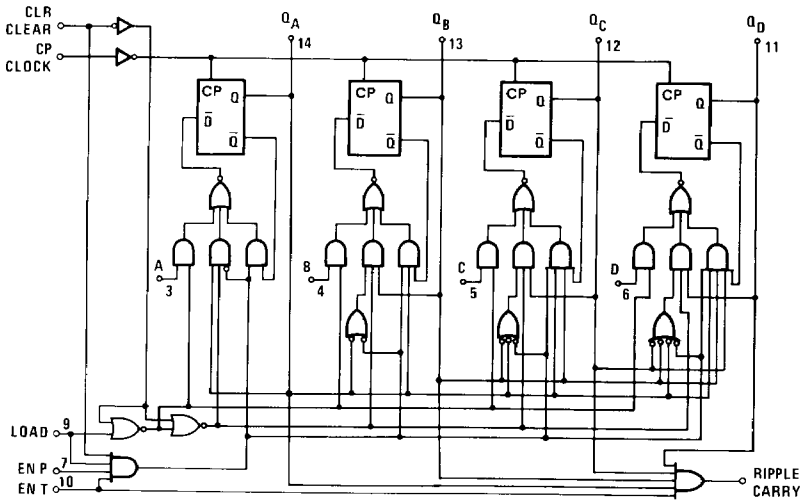
LOGIC DIAGRAMS

25LS160
Synchronous Decade Counter



25LS162 synchronous decade counters are similar; however, the clear is synchronous as shown for the 25LS163 binary counters.

25LS163 SYNCHRONOUS
BINARY COUNTER



25LS161 synchronous binary counters are similar; however, the clear is asynchronous as shown for the 25LS160 decade counters.

Recommended Operating Conditions

	Military			Commercial			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-440			-440	μA
Low-level output current, I_{OL}	4		8	4		8	mA
Operating free-air temperature, T_A	-5.5		125	0		70	°C

Electrical Characteristics Over Recommended Free-Air Temperature Range (Unless Otherwise Noted)

Parameter		Test Conditions*		Military			Commercial			Unit
				Min	Typ**	Max	Min	Typ**	Max	
V_{IH}				2			2			V
V_{IL}						0.7			0.8	V
V_I		V_{CC}=MIN, I_I=-18mA				-1.5			-1.5	V
V_{OH}		V_{CC}=MIN, V_{IH}=2V, V_{IL}=V_{IL}max, I_{OH}=-440μA		2.5	3.4		2.7	3.4		V
V_{OL}		V_{CC}=MIN, V_{IH}=2V, V_{IL}=V_{IL}max,	I_{OL}=4mA		0.25	0.40		0.25	0.40	V
			I_{OL}=8mA		0.35	0.45		0.35	0.45	
I_I	Data or enable P	V_{CC}=MAX, V_I=7V				0.1			0.1	mA
	Load, clock, or enable T					0.2			0.2	
	Clear (LS160,161)					0.1			0.1	
	Clear (LS162,163)					0.2			0.2	
I_{IH}	Data or enable P	V_{CC}=MAX, V_I=2.7V				20			20	μA
	Load, clock, or enable T					40			40	
	Clear (LS160,161)					20			20	
	Clear (LS162,163)					40			40	
I_{IL}	Data or enable P	V_{CC}=MAX, V_I=0.4V				-0.4			-0.4	mA
	Load, clock, or enable T					-0.8			-0.8	
	Clear (LS160,161)					-0.4			-0.4	
	Clear (LS162,163)					-0.8			-0.8	
I_{OS}†		V_{CC}=MAX		-15		-85	-15		-85	mA
I_{CCH}		V_{CC}=MAX, See Note 1			18	31		18	31	mA
I_{CCL}		V_{CC}=MAX, See Note 2			19	32		19	32	mA

*For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
**All typical values are at V_{CC} = 5V, T_A = 25°C.
†Not more than one output should be shorted at a time.

NOTES:
1. I_{CCH} is measured with the load input high, then again with the load input low, with all other inputs high and all outputs open.
2. I_{CCL} is measured with the clock input high, then again with the clock input low, with all other inputs low and all outputs open.

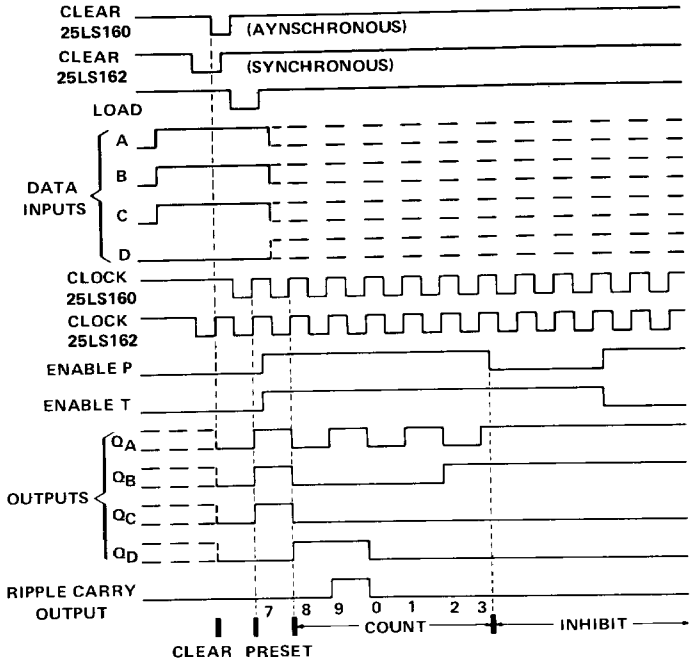
Switching Characteristics, V_{CC} = 5V, T_A = + 25°C

Parameters	From (Inputs)	To (Outputs)	+25°C Min	+25°C Typ	+25°C Max	Unit
Test Conditions: C_L = 15pF, R_L = 2kΩ (see Fig. A on page 2-174)						
t_{PLH}	Clock	Carry		25	35	ns
t_{PHL}				20	35	
t_{PLH}	Clock (Load Input High)	Q		10	18	ns
t_{PHL}				15	20	
t_{PLH}	Clock (Load Input Low)	Q		10	18	ns
t_{PHL}				14	20	
t_{PLH}	Enable T	Carry		15	20	ns
t_{PHL}				9	14	
t_{PHL}	Clear (Note 1)	Q		14	28	ns
t_{pw}	Pulse Width	Clock	25			ns
		Clear	20			
t_s	Set up time	Data A,B,C,D	20			ns
		ENABLE P	20			
		Load, Enable T	20			
		Clear (Note 2)	20			
t_h	Hold time	Any input	3			ns
f_{max}	Maximum Frequency		30	40		MHz

NOTES:

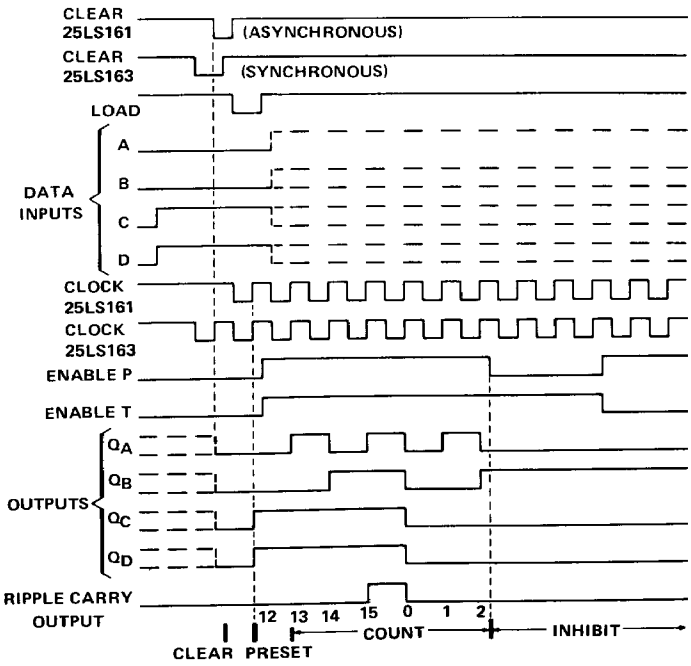
1. Measured from clear input on 25LS160 and 25LS161. Measured from clock input on 25LS162 and 25LS163.
2. Applies to 25LS162 and 25LS163 only.

TYPICAL CLEAR, PRESET, COUNT, AND INHIBIT SEQUENCES



25LS160, 25LS162

Illustrated below is the following sequence:
1. Clear outputs to zero
2. Preset to BCD seven
3. Count to eight, nine, zero, one, two, and three
4. Inhibit



25LS161, 25LS163

Illustrated below is the following sequence:
1. Clear outputs to zero
2. Preset to binary twelve
3. Count to thirteen; fourteen fifteen, zero, one, and two
4. Inhibit

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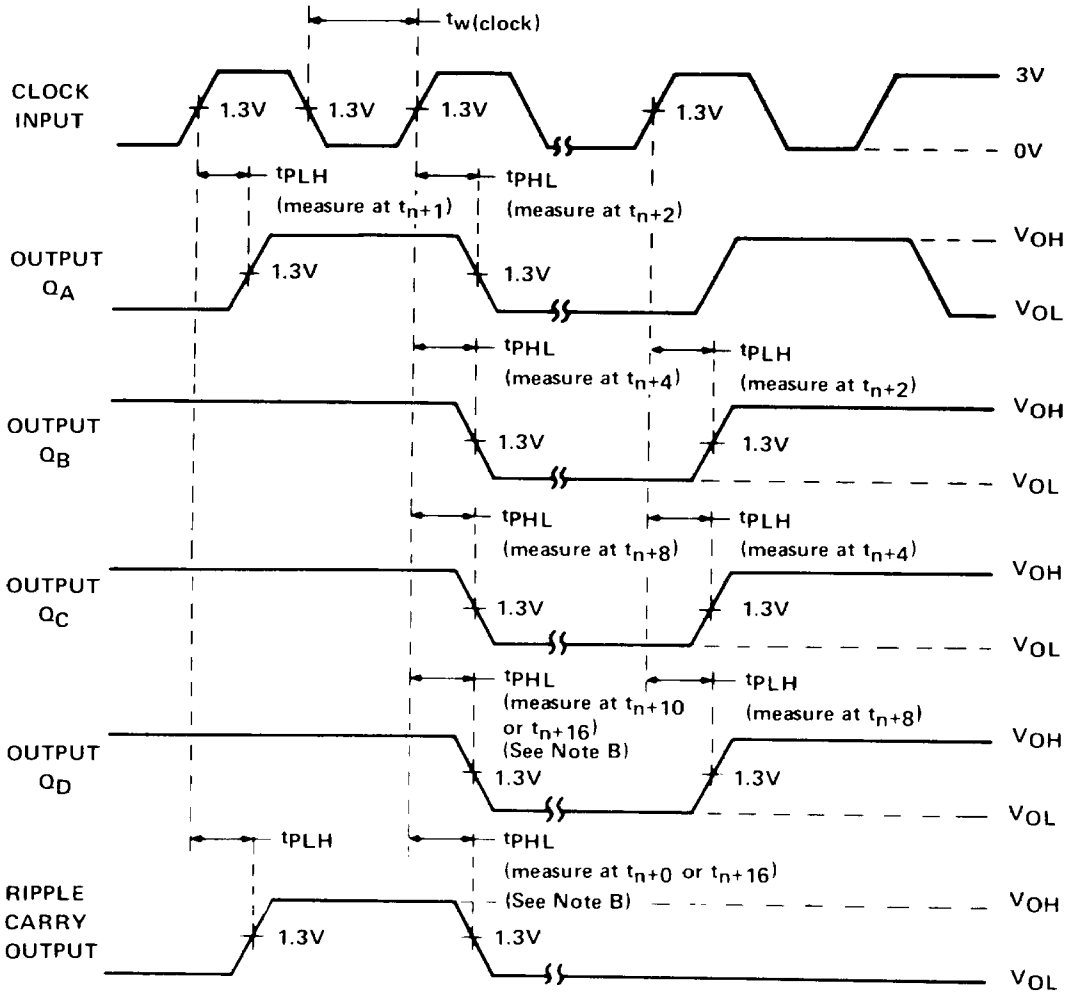
FIGURE 1

PARAMETER MEASUREMENT INFORMATION



VOLTAGE WAVEFORMS

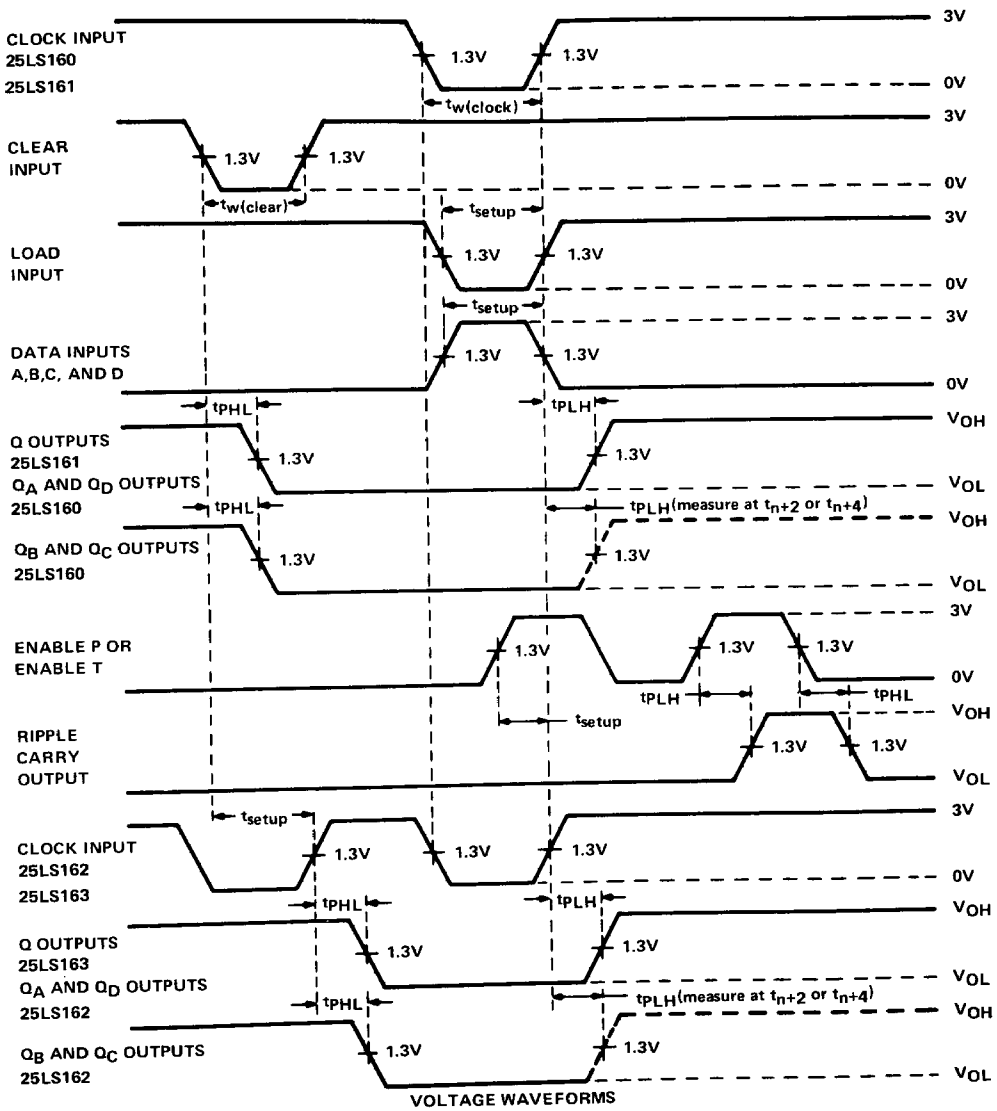
NOTES:

A. The input pulses are supplied by a generator having the following characteristics: PRR ≤ MHz, duty cycle ≤ 50%, $Z_{out} \approx 50\Omega$: $t_r \leq 15$ ns, $t_f \leq 6$ ns. Vary PRR to measure f_{max}.

B. Outputs Q_d and carry are tested at t_{n+10} 25LS162, and at t_n+16 for 25LS 163 where t_n is the bit time when all outputs are low.

FIGURE 2

PARAMETER MEASUREMENT INFORMATION



VOLTAGE WAVEFORMS

NOTES:

A. The input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, $Z_{out} \approx 50\ \Omega$; $t_r \leq 15$ ns, $t_f \leq 6$ ns.

B. Enable P and enable T setup times are measured at $t_n = 0$.

TYPICAL APPLICATION DATA

N-BIT SYNCHRONOUS COUNTERS

This application demonstrates how the look-ahead carry circuit can be used to implement a high-speed n-bit counter. The 25LS160 or 25LS162 will count in BCD and the 25LS163 will count in binary. Virtually any count mode (modulo-N, N_1-to N_2, N_1-to-maximum) can be used with this fast look-ahead circuit.