

SN54HC563, SN74HC563 OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

SCLS145B – DECEMBER 1982 – REVISED MAY 1997

- High-Current 3-State Outputs Drive Bus Lines Directly or up to 15 LSTTL Loads
- Bus-Structured Pinout
- Package Options Include Plastic Small-Outline (DW) and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs

description

These 8-bit transparent D-type latches feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

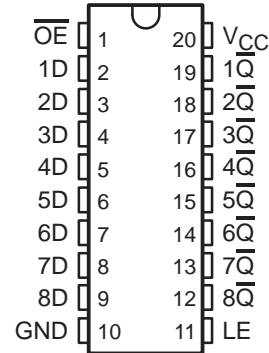
While the latch-enable (LE) input is high, the \bar{Q} outputs follow the complements of the data (D) inputs. When LE is taken low, the outputs are latched at the inverses of the levels set up at the D inputs.

A buffered output-enable (\overline{OE}) input places the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased high logic level provide the capability to drive bus lines without interface or pullup components.

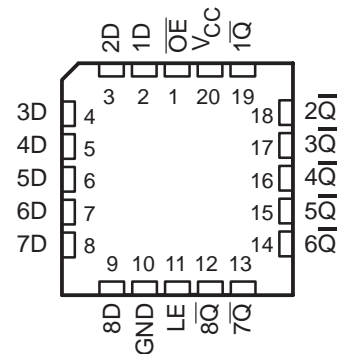
\overline{OE} does not affect internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN54HC563 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74HC563 is characterized for operation from -40°C to 85°C .

SN54HC563 . . . J OR W PACKAGE
SN74HC563 . . . DW OR N PACKAGE
(TOP VIEW)



SN54HC563 . . . FK PACKAGE
(TOP VIEW)



FUNCTION TABLE
(each latch)

INPUTS			OUTPUT
\overline{OE}	LE	D	\bar{Q}
L	H	H	L
L	H	L	H
L	L	X	\bar{Q}_0
H	X	X	Z



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
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recommended operating conditions

		SN54HC563			SN74HC563			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage	2	5	6	2	5	6	V
V _{IH}	High-level input voltage	V _{CC} = 2 V	1.5		1.5		V	
		V _{CC} = 4.5 V	3.15		3.15			
		V _{CC} = 6 V	4.2		4.2			
V _{IL}	Low-level input voltage	V _{CC} = 2 V	0	0.5	0	0.5	V	
		V _{CC} = 4.5 V	0	1.35	0	1.35		
		V _{CC} = 6 V	0	1.8	0	1.8		
V _I	Input voltage	0	V _{CC}		0	V _{CC}		V
V _O	Output voltage	0	V _{CC}		0	V _{CC}		V
t _t	Input transition (rise and fall) time	V _{CC} = 2 V	0	1000	0	1000	ns	
		V _{CC} = 4.5 V	0	500	0	500		
		V _{CC} = 6 V	0	400	0	400		
T _A	Operating free-air temperature	-55		125	-40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V _{CC}	T _A = 25°C			SN54HC563		SN74HC563		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	V _I = V _{IH} or V _{IL}	I _{OH} = -20 μA	2 V	1.9	1.998		1.9		1.9	V	
			4.5 V	4.4	4.499		4.4		4.4		
			6 V	5.9	5.999		5.9		5.9		
		I _{OH} = -6 mA	4.5 V	3.98	4.3		3.7		3.84		
		I _{OH} = -7.8 mA	6 V	5.48	5.8		5.2		5.34		
V _{OL}	V _I = V _{IH} or V _{IL}	I _{OL} = 20 μA	2 V		0.002	0.1		0.1		V	
			4.5 V		0.001	0.1		0.1			0.1
			6 V		0.001	0.1		0.1			0.1
		I _{OL} = 6 mA	4.5 V		0.17	0.26		0.4			0.33
		I _{OL} = 7.8 mA	6 V		0.15	0.26		0.4			0.33
I _I	V _I = V _{CC} or 0	6 V		±0.1	±100		±1000		±1000	nA	
I _{OZ}	V _O = V _{CC} or 0	6 V		±0.01	±0.5		±10		±5	μA	
I _{CC}	V _I = V _{CC} or 0, I _O = 0	6 V			8		160		80	μA	
C _i		2 V to 6 V		3	10		10		10	pF	



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timing requirements over recommended operating free-air temperature range (unless otherwise noted)

	V_{CC}	$T_A = 25^\circ\text{C}$		SN54HC563		SN74HC563		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_w Pulse duration, LE high	2 V	80	120	100				ns
	4.5 V	16	24	20				
	6 V	14	20	17				
t_{su} Setup time, data before LE↓	2 V	50	75	63				ns
	4.5 V	10	15	13				
	6 V	9	13	11				
t_h Hold time, data after LE↓	2 V	5	5	5				ns
	4.5 V	5	5	5				
	6 V	5	5	5				

switching characteristics over recommended operating free-air temperature range, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	$T_A = 25^\circ\text{C}$			SN54HC563		SN74HC563		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	D	\bar{Q}	2 V	77	175	265	220			ns	
			4.5 V	26	35	53	44				
			6 V	23	30	45	37				
	LE	Any \bar{Q}	2 V	90	175	265	220				
			4.5 V	27	35	53	44				
			6 V	23	30	45	37				
t_{en}	\overline{OE}	Any \bar{Q}	2 V	70	150	225	190			ns	
			4.5 V	24	30	45	38				
			6 V	21	26	38	32				
t_{dis}	\overline{OE}	Any \bar{Q}	2 V	47	150	225	190			ns	
			4.5 V	23	30	45	38				
			6 V	21	26	38	32				
t_t		Any \bar{Q}	2 V	28	60	90	75			ns	
			4.5 V	8	12	18	15				
			6 V	6	10	15	13				



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switching characteristics over recommended operating free-air temperature range, $C_L = 150 \text{ pF}$
(unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	$T_A = 25^\circ\text{C}$			SN54HC563		SN74HC563		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	D	\bar{Q}	2 V	95	200	300	250	ns			
			4.5 V	33	40	60	50				
			6 V	29	34	51	43				
	LE	Any \bar{Q}	2 V	103	225	335	285				
			4.5 V	33	45	67	57				
			6 V	29	38	57	48				
t_{en}	\overline{OE}	Any \bar{Q}	2 V	85	200	300	250	ns			
			4.5 V	29	40	60	50				
			6 V	26	34	51	43				
t_t		Any \bar{Q}	2 V	60	210	315	265	ns			
			4.5 V	17	42	63	53				
			6 V	14	36	53	45				

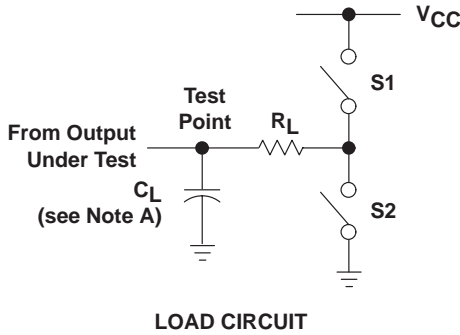
operating characteristics, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
C_{pd} Power dissipation capacitance per latch	No load	50	pF

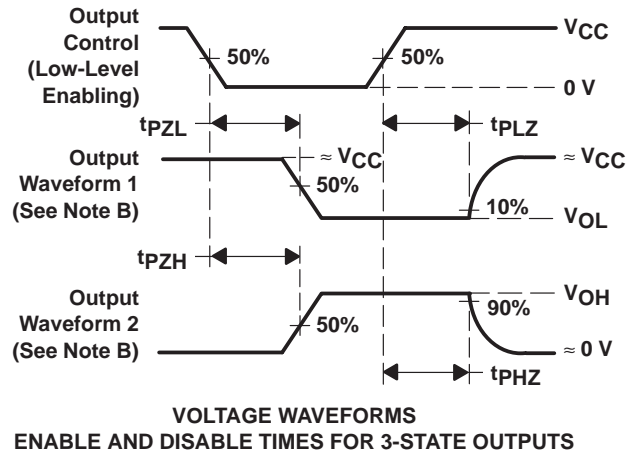
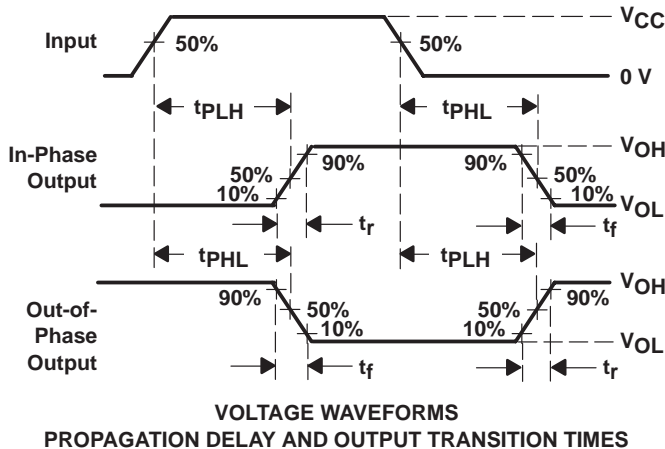
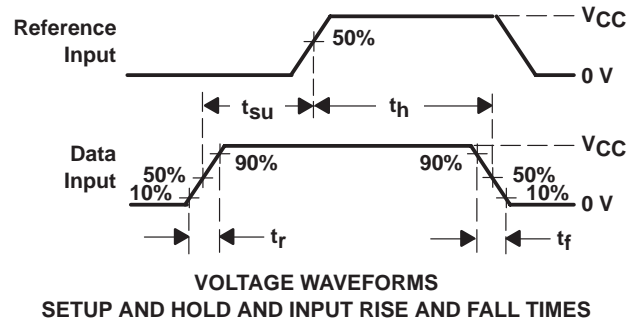
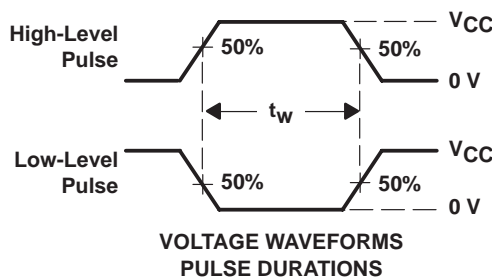
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PARAMETER MEASUREMENT INFORMATION



PARAMETER	R_L	C_L	S1	S2
t_{en}	1 k Ω	50 pF or 150 pF	Open	Closed
			Closed	Open
t_{dis}	1 k Ω	50 pF	Open	Closed
			Closed	Open
t_{pd} or t_t	—	50 pF or 150 pF	Open	Open



- NOTES: A. C_L includes probe and test-fixture capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1$ MHz, $Z_O = 50 \Omega$, $t_r = 6$ ns, $t_f = 6$ ns.
 D. The outputs are measured one at a time with one input transition per measurement.
 E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 F. t_{PZL} and t_{PZH} are the same as t_{en} .
 G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

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