LS190 Synchronous BCD Decade Up/Down Counter

LS191 Synchronous 4-Bit Binary Up/Down Counter

FEATURES

- Single up/down count mode control line
- Asynchronous parallel load
- Count enable, parallel load control inputs
- Cascadable

DESCRIPTION

The LS190 and LS191 are synchronous, reversible up/down counters having a complexity of 58 equivalent gates. The LS191 is a 4-bit binary counter and the LS190 is a BCD counter. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple clock) counters.

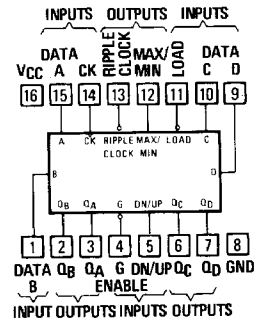
The outputs of the four master-slave flip-flops are triggered on a low-to-high-level transition of the clock input if the enable input is low. A high at the enable input inhibits counting. Level changes at the enable and down/up inputs should be made only when the clock input is high. The direction of the count is determined by the level of the down/up input. When low, the counter counts up and when high, it counts down.

These counters are fully programmable; that is, the outputs may be preset to either level by placing a low on the load input and entering the desired data at the data inputs. The output will change to agree with the data inputs independently of the level of the clock input. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

The clock, down/up, and load inputs are buffered to lower the drive requirement which significantly reduces the number of clock drivers, etc., required for long parallel words.

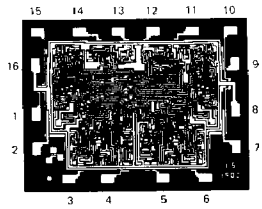
Two outputs have been made available to perform the cascading function: ripple clock and maximum/minimum count. The latter output produces a high-level output pulse with a duration approximately equal to one complete cycle of the clock when the counter overflows or underflows. The ripple clock output produces a low-level output pulse equal in width to the low-level portion of the clock input when an overflow or underflow condition exists. The counters can be easily cascaded by feeding the ripple clock output to the enable input of the succeeding counter if parallel clocking is used, or to the clock input if parallel enabling is used. The maximum/minimum count output can be used to accomplish look-ahead for high-speed operation.

PIN-OUT DIAGRAM

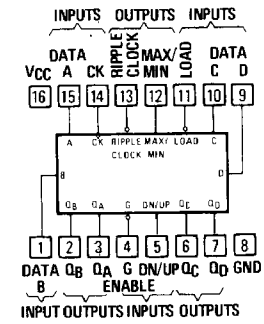


LOW INPUT TO LOAD SETS Q_A = A, Q_B = B, Q_C = C, Q_D = D

LS190

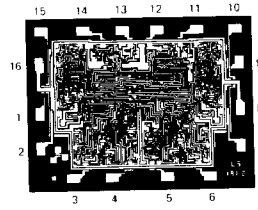


Die Size .100 x .077



LOW INPUT TO LOAD SETS Q_A = A, Q_B = B, Q_C = C, Q_D = D

LS191



Die Size .100 x .077

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Recommended Operating Conditions

	9LS/54LS			9LS/74LS			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-400			-400	μA
Low-level output current, I_{OL}			4			8	mA
Input clock frequency, f_{clock}	0		20	0		20	MHz
Width of clock input pulse, $t_{w(clock)}$	25			25			ns
Width of load input pulse, $t_{w(load)}$	35			35			ns
Data setup time, t_{setup} (see Figures 1 and 2)	20			20			ns
Enable to clock setup time, t_{setup}	20			20			ns
Data hold time, t_{hold}	0			0			ns
Operating free-air temperature, T_A	-55		125	0		70	°C

Electrical Characteristics Over Recommended Free-Air Temperature Range (Unless Otherwise Noted)

Parameter		Test Conditions*		9LS/54LS			9LS/74LS			Unit
				Min	Typ**	Max	Min	Typ**	Max	
V_{IH}				2			2			V
V_{IL}						0.7			0.8	V
V_I		V_{CC}=MIN, I_I=-18mA				-1.5			-1.5	V
V_{OH}		V_{CC}=MIN, V_{IH}=2V, V_{IL}=V_{IL}max, I_{OH}=-400μA		2.5	3.4		2.7	3.4		V
V_{OL}		V_{CC}=MIN, V_{IH}=2V, V_{IL}=V_{IL}max	I_{OL}=4mA		0.25	0.40		0.25	0.40	V
			I_{OL}=8mA					0.35	0.5	
I_I	Enable	V_{CC}=MAX, V_I=7V				0.3			0.3	mA
	Others					0.1			0.1	
I_{IH}	Enable	V_{CC}=MAX, V_I=2.7V				60			60	μA
	Others					20			20	
I_{IL}	Enable	V_{CC}=MAX, V_I=0.4V				-1.2			-1.2	mA
	Others					-0.4			-0.4	
I_{OS}†		V_{CC}=MAX		-15		-100	-15		-100	mA
I_{CC}††		V_{CC}=MAX			20	35		20	35	mA

*For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
**All typical values are at V_{CC} = 5V, T_A = 25°C.
†Not more than one output should be shorted at a time.
††I_{CC} is measured with all inputs grounded and all outputs open.

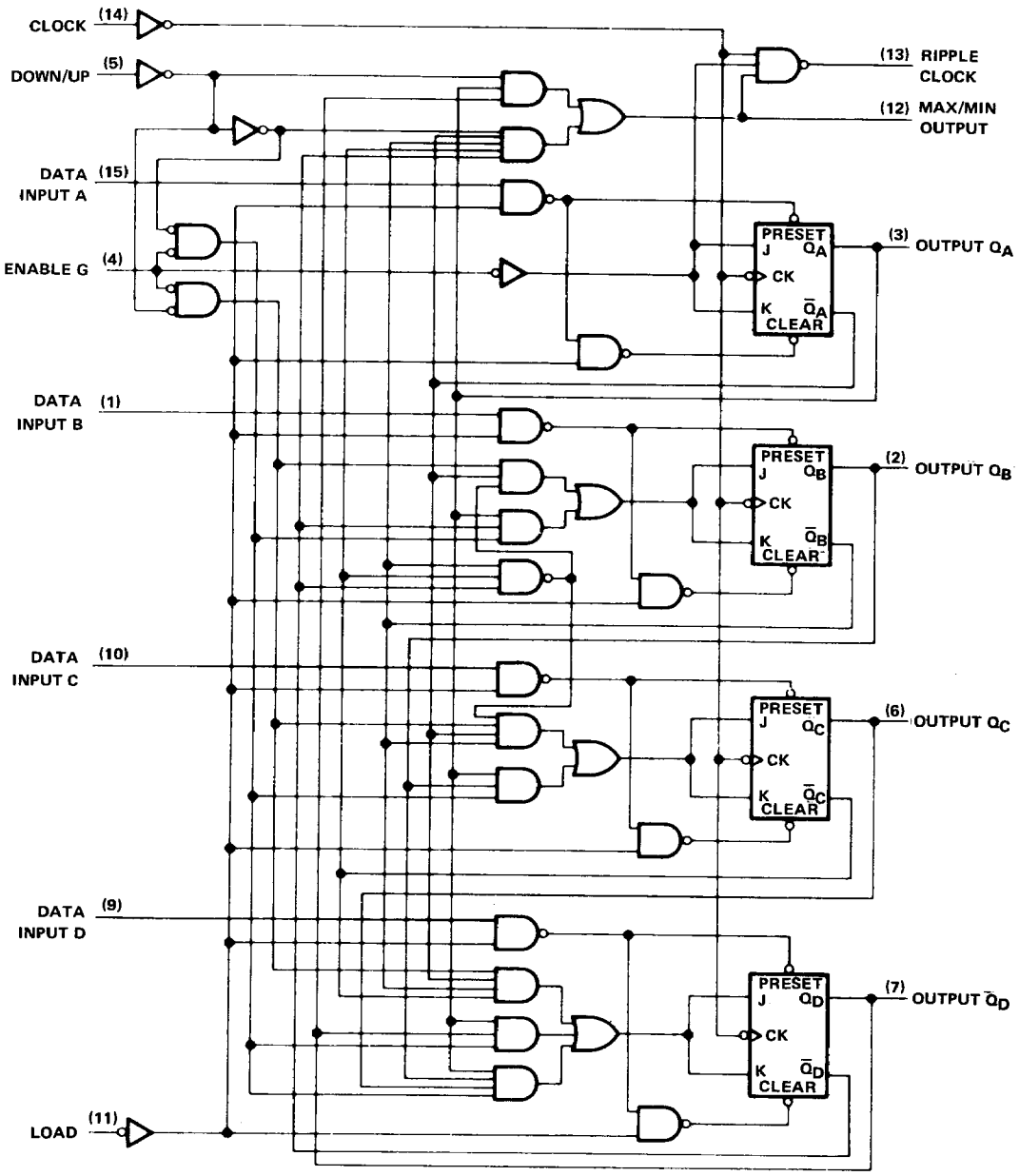
Switching Characteristics, V_{CC} = 5V Over Recommended Free-Air Temperature Range

Parameter	From (Input)	To (Output)	−55°C			+25°C			+125°C			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Test Conditions: C_L = 15pF, R_L = 2kΩ (See Fig. 1 thru 7 on pages 2-115 and 2-116 and Fig. A on page 2-174)												
f_{max}						20	25					MHz
t_{PLH}	Load	Q_A,Q_B,Q_C,Q_D		25	37		22	33		25	37	ns
t_{PHL}				36	54		33	50		36	54	
t_{PLH}	Data A,B,C,D	Q_A,Q_B,Q_C,Q_D		17	26		14	22		17	26	ns
t_{PHL}				38	56		35	50		38	56	
t_{PLH}	Clock	Ripple Clock		16	24		13	20		16	24	ns
t_{PHL}				19	28		16	24		19	28	
t_{PLH}	Clock	Q_A,Q_B,Q_C,Q_D		19	28		16	24		19	28	ns
t_{PHL}				27	40		24	36		27	40	
t_{PLH}	Clock	Max/Min		31	46		28	42		31	46	ns
t_{PHL}				40	56		37	52		40	56	
t_{PLH}	Down/Up	Ripple Clock		33	49		30	45		33	49	ns
t_{PHL}				33	49		30	45		33	49	
t_{PLH}	Down/Up	Max/Min		24	37		21	33		24	37	ns
t_{PHL}				25	38		22	33		25	38	
t_{PLH}	Enable	Ripple Clock		24	37		21	33		24	37	ns
t_{PHL}				25	38		22	33		25	38	
Test Conditions: C_L = 50pF, R_L = 2kΩ (See Fig. 1 thru 7 on pages 2-115 and 2-116 and Fig. A on page 2-174)												
t_{PLH}	Load			28	42		25	37		28	42	ns
t_{PHL}				39	59		36	54		39	59	
t_{PLH}	Data A,B,C,D	Q_A,Q_B,Q_C,Q_D		20	31		17	26		20	31	ns
t_{PHL}				41	61		38	54		41	61	
t_{PLH}	Clock	Ripple Clock		19	29		16	24		19	29	ns
t_{PHL}				22	33		19	28		22	33	
t_{PLH}	Clock	Q_A,Q_B,Q_C,Q_D		22	33		19	28		22	33	ns
t_{PHL}				30	45		27	40		30	45	
t_{PLH}	Clock	Max/Min		34	51		31	46		34	51	ns
t_{PHL}				43	61		40	56		43	61	
t_{PLH}	Down/Up	Ripple Clock		36	54		33	49		36	54	ns
t_{PHL}				36	54		33	49		36	54	
t_{PLH}	Down/Up	Max/Min		27	42		24	37		27	42	ns
t_{PHL}				28	43		25	37		28	43	
t_{PLH}	Enable	Ripple Clock		27	42		24	37		27	42	ns
t_{PHL}				28	43		25	37		28	33	

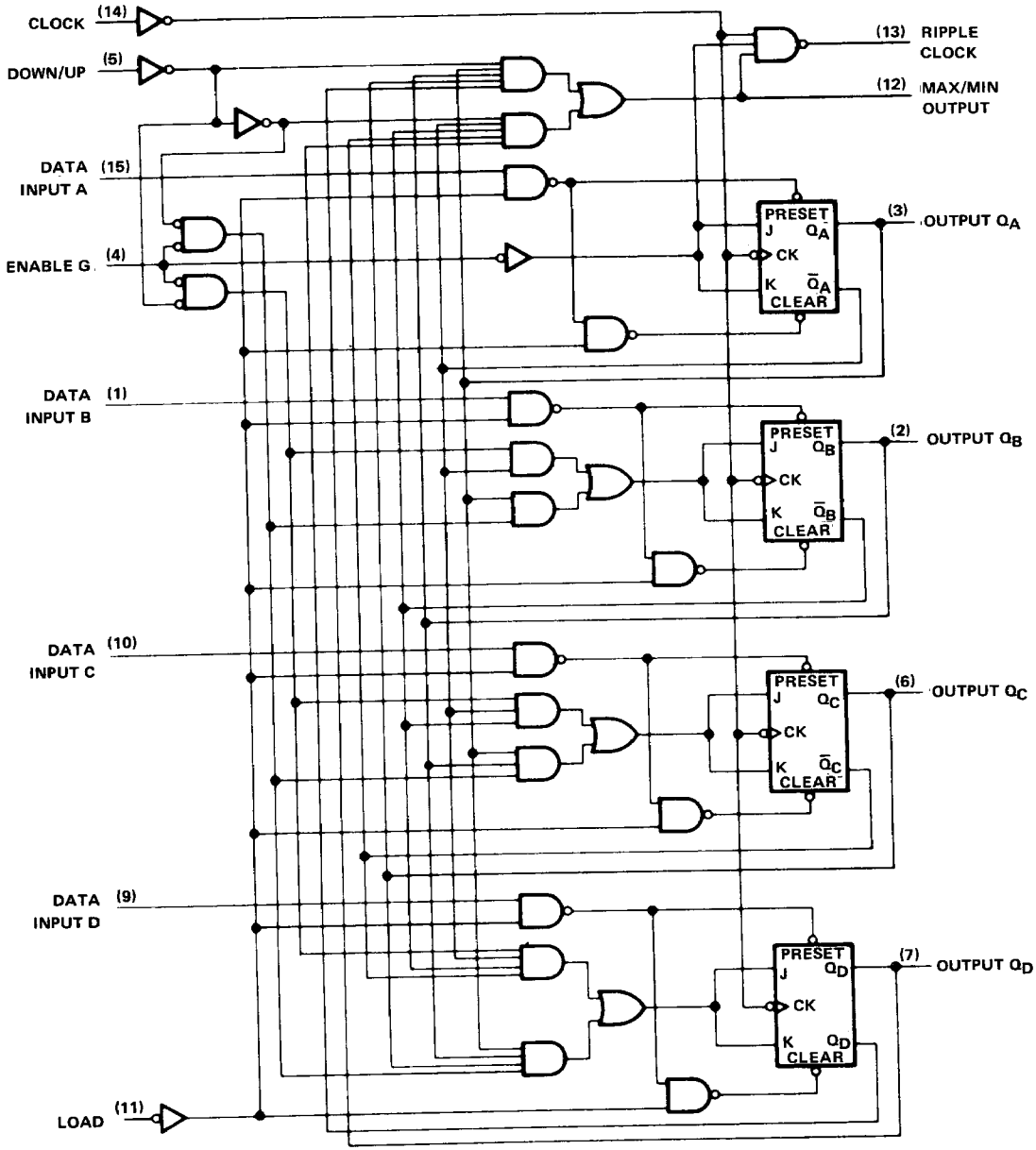
Note: AC specification shown under −55°C and +125°C are for 9LS devices only.
All 50pF specifications are for 9LS only.

LOGIC DIAGRAM

LS190



LOGIC DIAGRAM
LS191



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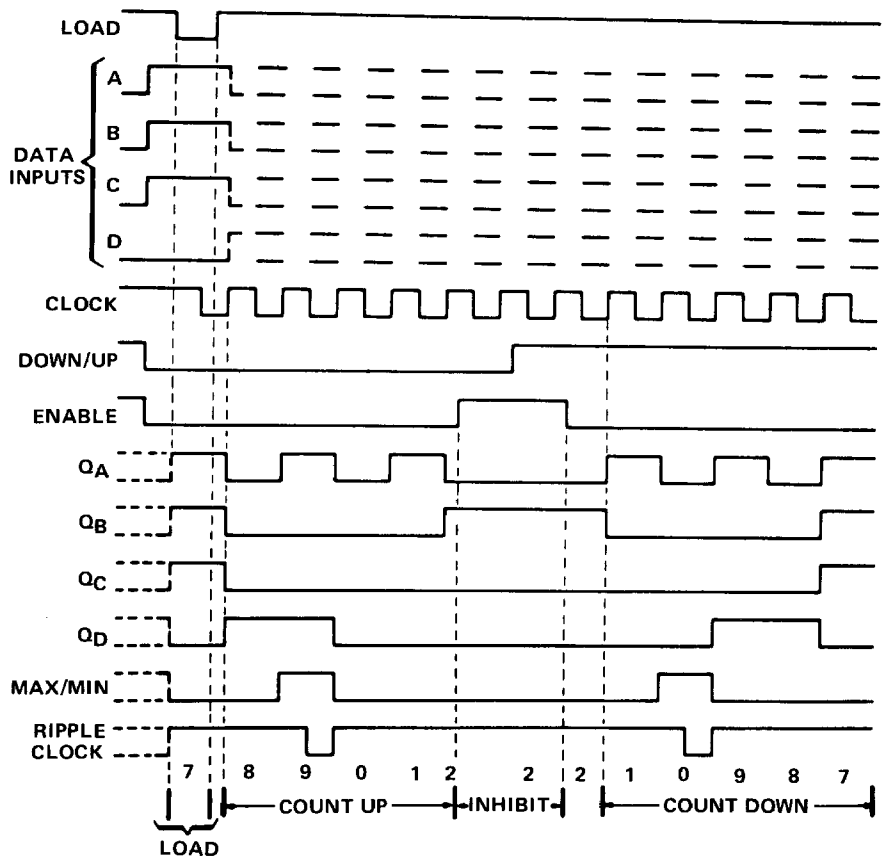
LS190 TYPICAL LOAD, COUNT AND INHIBIT SEQUENCES

Illustrated below is the following sequence:

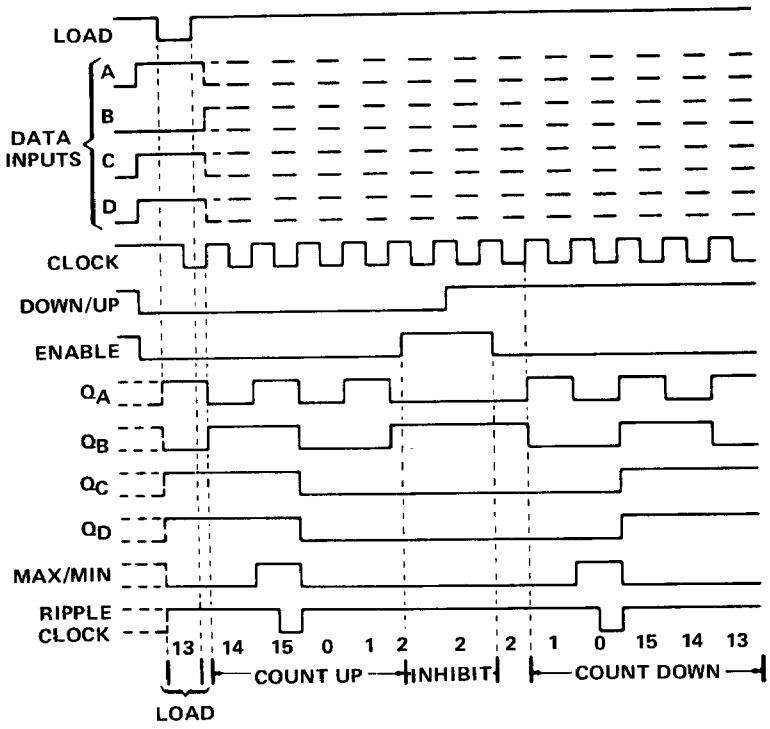
1. Load (preset) to BCD seven.
2. Count up to eight, nine (maximum), zero, one, and two.
3. Inhibit.
4. Count down to one, zero (minimum), nine, eight, and seven.



LS191 TYPICAL LOAD, COUNT AND INHIBIT SEQUENCES

Illustrated below is the following sequence:

1. Load (preset) to binary thirteen.
2. Count up to fourteen, fifteen (maximum), zero, one, and two.
3. Inhibit.
4. Count down to one, zero (minimum), fifteen, fourteen, and thirteen.



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PARAMETER MEASUREMENT INFORMATION

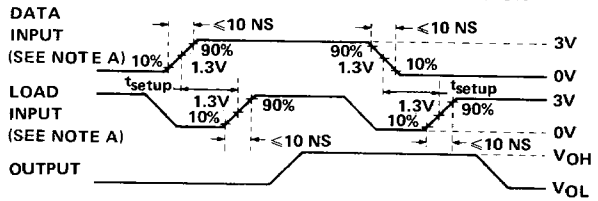


FIGURE 1—DATA SETUP TIME VOLTAGE WAVEFORMS

See waveform sequences in Figures 4 through 7 for propagation times from a specific input to a specific output. For simplification, pulse rise times, reference levels, etc., have not been shown in Figures 4 through 7.

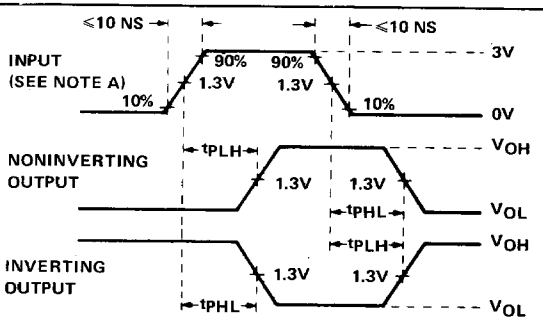
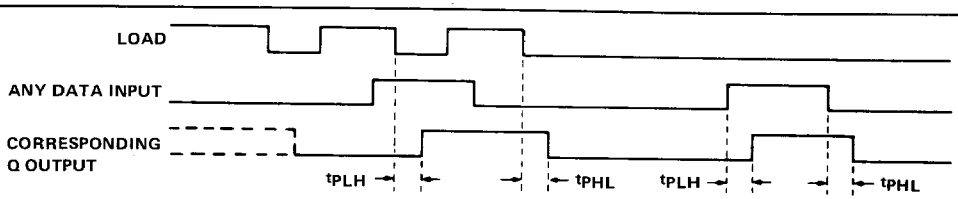


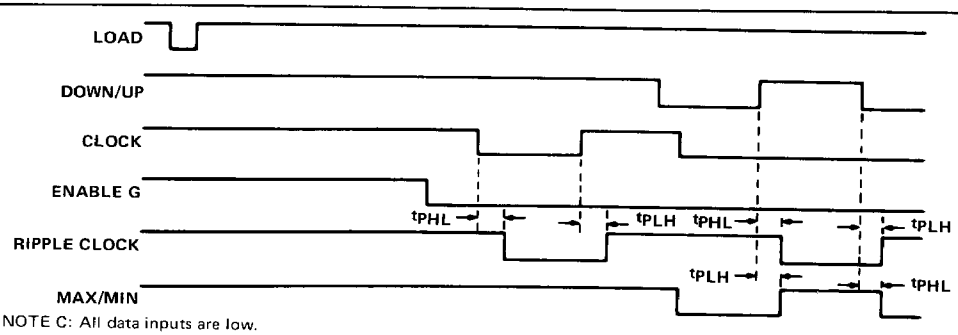
FIGURE 2– GENERAL VOLTAGE WAVEFORMS FOR PROPAGATION TIMES

NOTES:
A. The input pulses are supplied by generators having the following characteristics: $Z_{out} = 50\Omega$, duty cycle ≤ 50%, PRR ≤ 1MHz.



NOTE B: Conditions on other inputs are irrelevant.

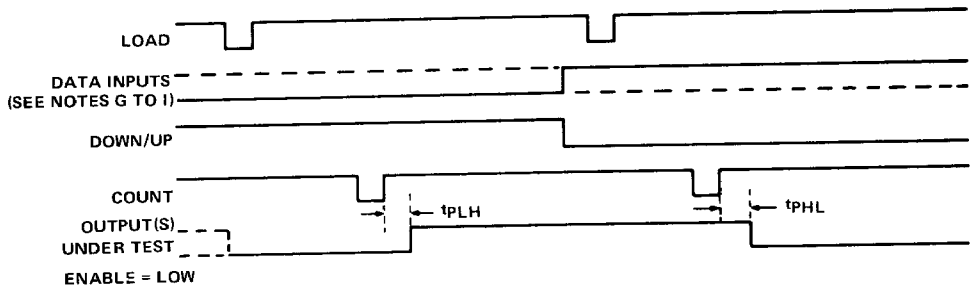
FIGURE 3—LOAD TO OUTPUT AND DATA TO OUTPUT



NOTE C: All data inputs are low.

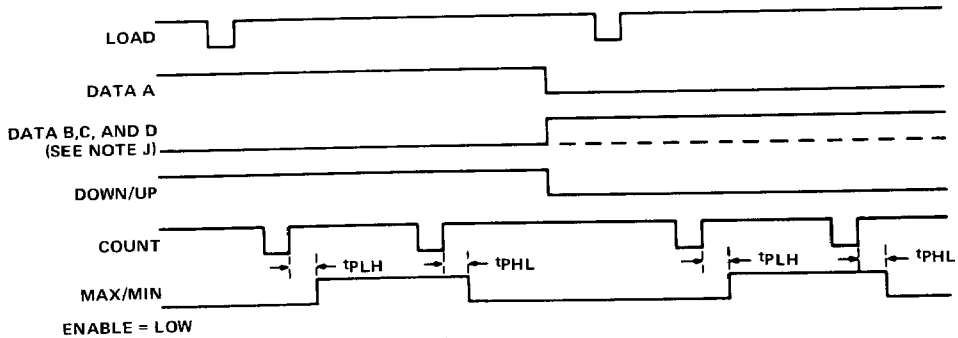
FIGURE 4—ENABLE TO RIPPLE CLOCK, CLOCK TO RIPPLE CLOCK, DOWN/UP TO MAX/MIN

PARAMETER MEASUREMENT INFORMATION (Continued)



F. to test Q_A, Q_B, and Q_C outputs of LS190: Data inputs A, B, and C are shown by the solid line. Data input D is shown by the dashed line.
G. To test Q_D output of LS190: Data inputs A and D are shown by the solid line. Data inputs B and C are held at the low logic level.
H. To test Q_A, Q_B, Q_C, and Q_D outputs of LS191: All four data inputs are shown by the solid line.

FIGURE 5–CLOCK TO OUTPUT



NOTE I:
Data inputs B and C are shown by the dashed line for the LS190 and the solid line for the LS191: Data input D is shown by the solid line for both devices.

FIGURE 6–CLOCK TO MAX/MIN