

To our customers,

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## Old Company Name in Catalogs and Other Documents

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Renesas Electronics website: <http://www.renesas.com>

April 1<sup>st</sup>, 2010  
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (<http://www.renesas.com>)

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# MOS FIELD EFFECT TRANSISTOR

## 2SJ325, 325-Z

### SWITCHING

### P-CHANNEL POWER MOS FET

#### DESCRIPTION

The 2SJ325 is P-channel MOS Field Effect Transistor designed for solenoid, motor and lamp driver.

#### FEATURES

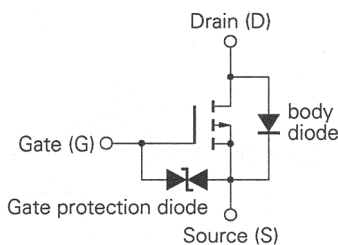
- Low On-state Resistance  
 $R_{DS(on)} = 0.08 \Omega$  TYP. ( $V_{GS} = -10 V, I_D = -2.0 A$ )  
 $R_{DS(on)} = 0.15 \Omega$  TYP. ( $V_{GS} = -4 V, I_D = -1.6 A$ )
- Low  $C_{iss}$ :  $C_{iss} = 800 pF$  TYP.
- Built-in G-S Gate Protection Diode

#### ABSOLUTE MAXIMUM RATINGS ( $T_A = 25^\circ C$ )

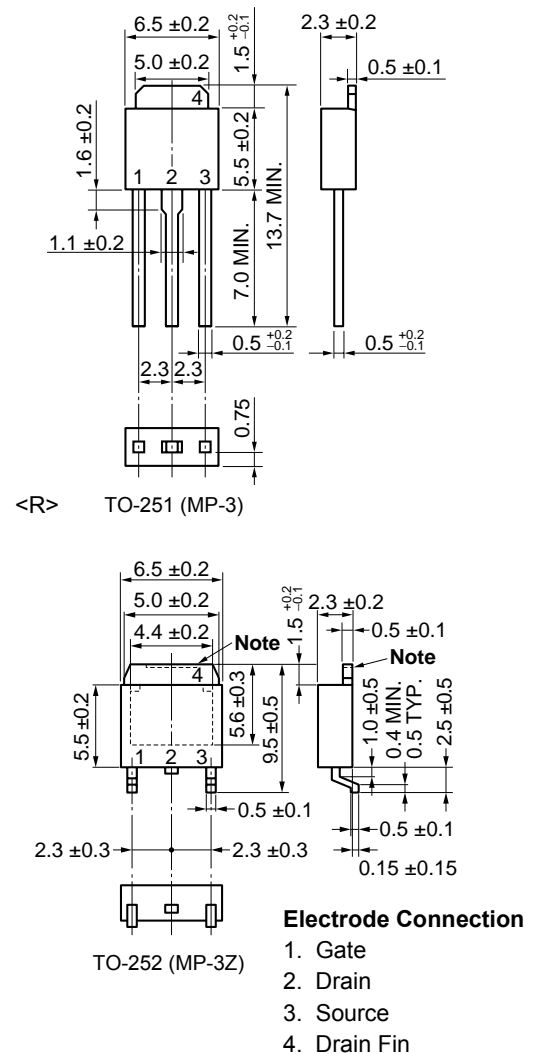
Drain to Source Voltage	$V_{DSS}$	-30	V
Gate to Source Voltage (AC)	$V_{GSS(AC)}$	$\pm 20$	V
Gate to Source Voltage (DC)	$V_{GSS(DC)}$	-20, +10	V
Drain Current (DC)	$I_{D(DC)}$	$\mp 4.0$	A
Drain Current (pulse) <sup>Note</sup>	$I_{D(pulse)}$	$\mp 16$	A
Total Power Dissipation ( $T_C = 25^\circ C$ )	$P_{T1}$	20	W
Total Power Dissipation ( $T_A = 25^\circ C$ )	$P_{T2}$	1.0	W
Channel Temperature	$T_{ch}$	150	$^\circ C$
Storage Temperature	$T_{stg}$	-55 to +150	$^\circ C$

**Note**  $PW \leq 10 \mu s$ , Duty Cycle  $\leq 1\%$

#### EQUIVALENT CIRCUIT



#### PACKAGE DRAWINGS (Unit: mm)



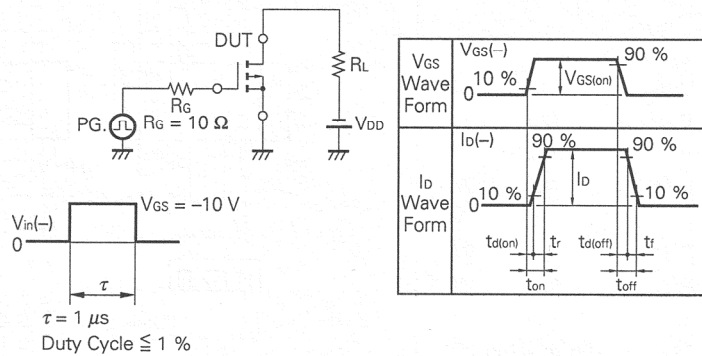
**Note** The depth of notch at the top of the fin is from 0 to 0.2 mm.

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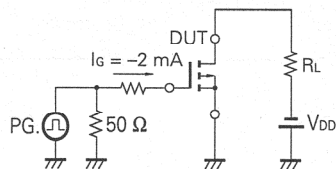
**ELECTRICAL CHARACTERISTICS (T<sub>a</sub> = 25 °C)**

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Drain to Source On-state Resistance	R <sub>DS(on)</sub>		0.08	0.11	Ω	V <sub>GS</sub> = -10 V, I <sub>D</sub> = -2.0 A
Drain to Source On-state Resistance	R <sub>DS(on)</sub>		0.15	0.24	Ω	V <sub>GS</sub> = -4 V, I <sub>D</sub> = -1.6 A
Gate to Source Cutoff Voltage	V <sub>GS(off)</sub>	-1.0	-1.5	-2.0	V	V <sub>DS</sub> = -10 V, I <sub>D</sub> = -1 mA
Forward Transfer Admittance	y <sub>fs</sub>	3.0	4.2		S	V <sub>DS</sub> = -10 V, I <sub>D</sub> = -2.0 A
Drain Leakage Current	I <sub>DSS</sub>			-10	μA	V <sub>DS</sub> = -30 V, V <sub>GS</sub> = 0
Gate to Source Leakage Current	I <sub>GSS</sub>			±10	μA	V <sub>GS</sub> = ±16 V, V <sub>DS</sub> = 0
Input Capacitance	C <sub>iss</sub>		800		pF	V <sub>DS</sub> = -10 V V <sub>GS</sub> = 0 f = 1 MHz
Output Capacitance	C <sub>oss</sub>		600		pF	
Reverse Transfer Capacitance	C <sub>rs</sub>		250		pF	
Turn-On Delay Time	t <sub>d(on)</sub>		15		ns	V <sub>GS(on)</sub> = -10 V V <sub>DD</sub> = -15 V I <sub>D</sub> = -2.0 A, R <sub>G</sub> = 10 Ω R <sub>L</sub> = 7.5 Ω
Rise Time	t <sub>r</sub>		65		ns	
Turn-Off Delay Time	t <sub>d(off)</sub>		85		ns	
Fall Time	t <sub>f</sub>		60		ns	
Total Gate Charge	Q <sub>G</sub>		28		nC	V <sub>GS</sub> = -10 V I <sub>D</sub> = -4.0 A V <sub>DD</sub> = -24 V
Gate to Source Charge	Q <sub>GS</sub>		3		nC	
Gate to Drain Charge	Q <sub>GD</sub>		11		nC	
Body Diode Forward Voltage	V <sub>F</sub>		0.9		V	I <sub>F</sub> = 4.0 A, V <sub>GS</sub> = 0
Reverse Recovery Time	t <sub>rr</sub>		65		ns	I <sub>F</sub> = 4.0 A, V <sub>GS</sub> = 0
Reverse Recovery Charge	Q <sub>rr</sub>		60		nC	di/dt = 50 A/μs

**Test Circuit 1: Switching Time**

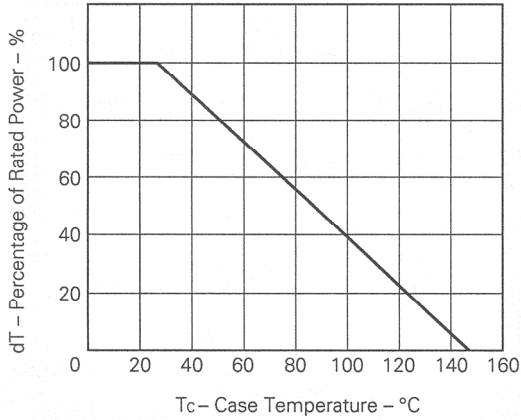


**Test Circuit 2: Gate Charge**

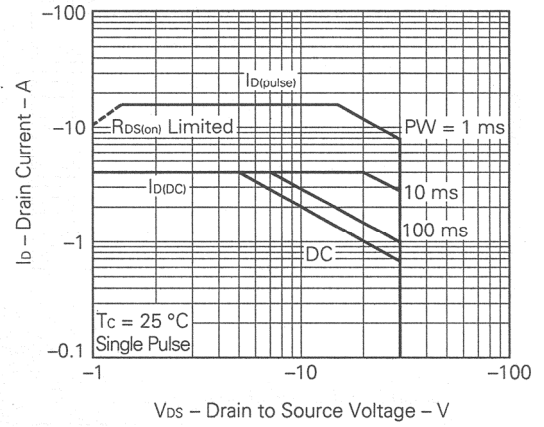


TYPICAL CHARACTERISTICS (T<sub>a</sub> = 25 °C)

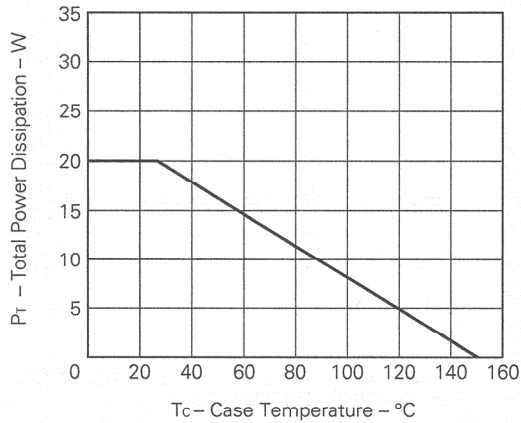
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



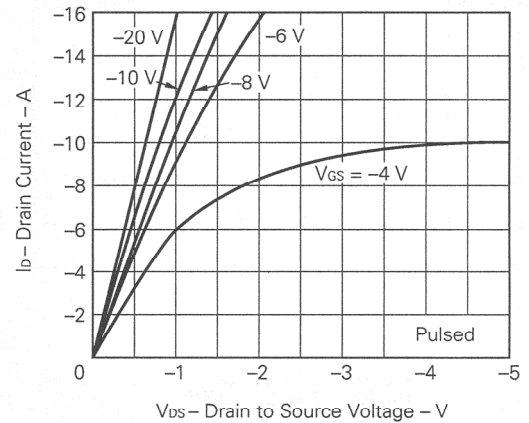
FORWARD BIAS SAFE OPERATING AREA



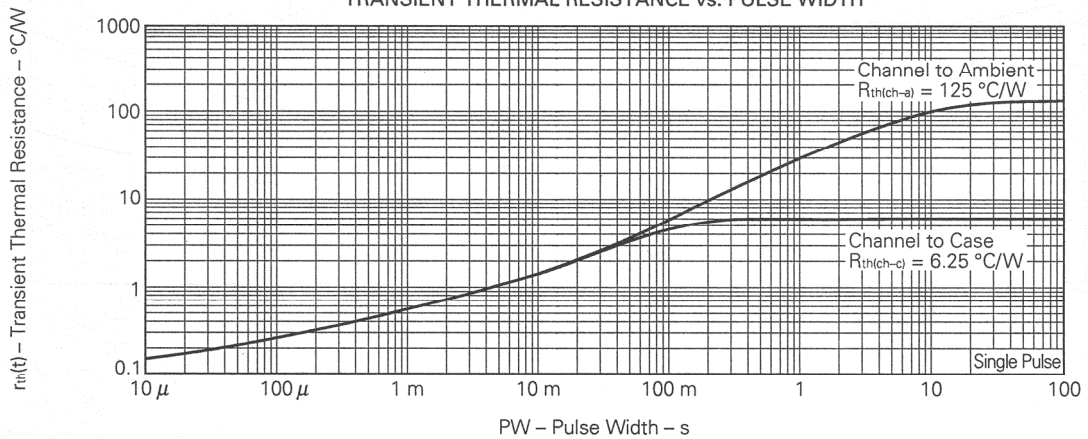
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE

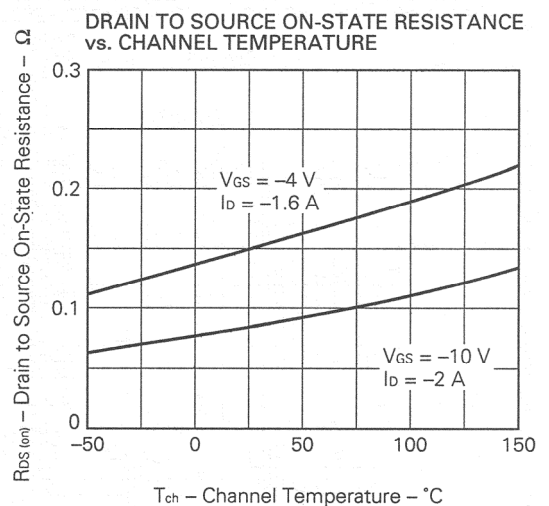
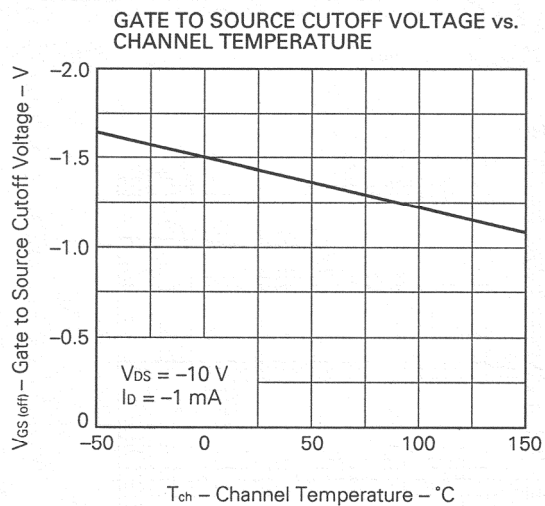
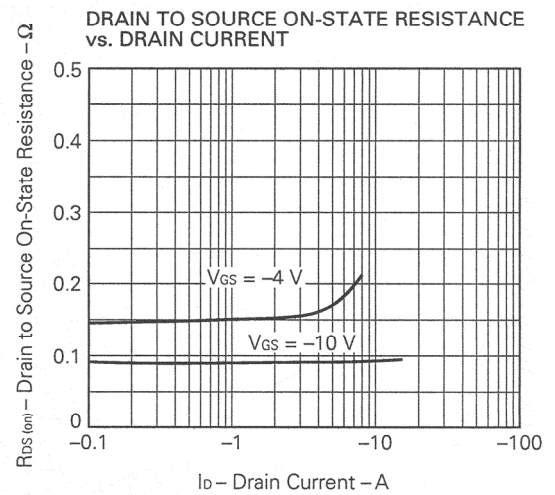
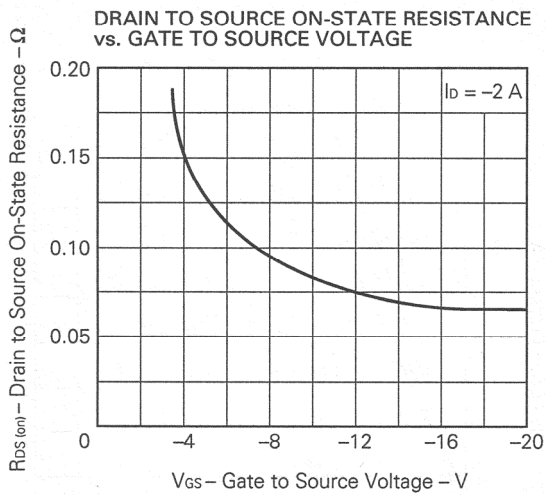
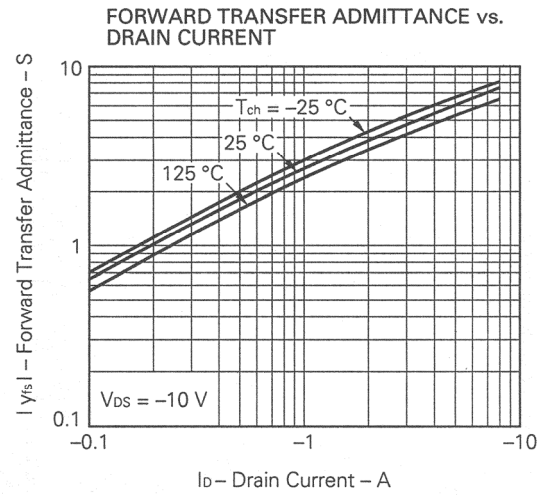
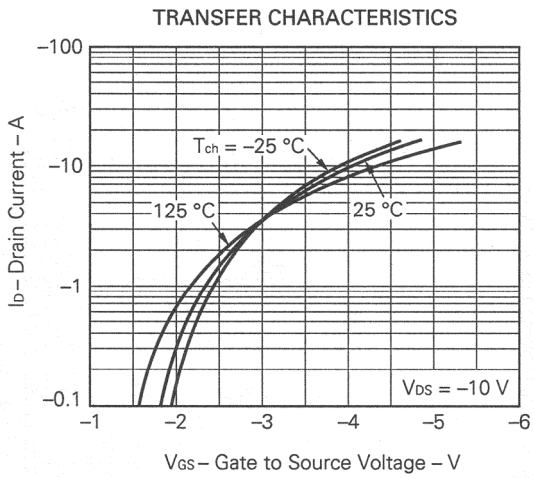


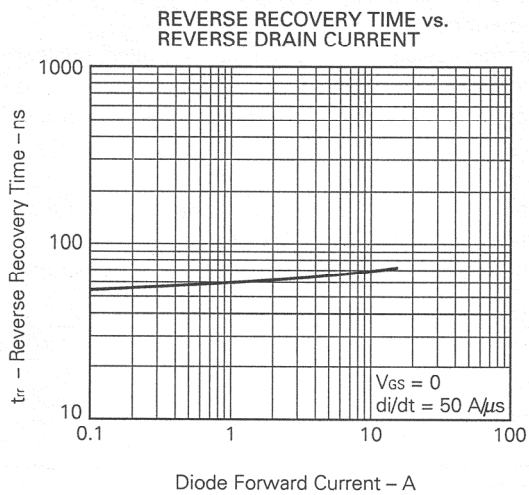
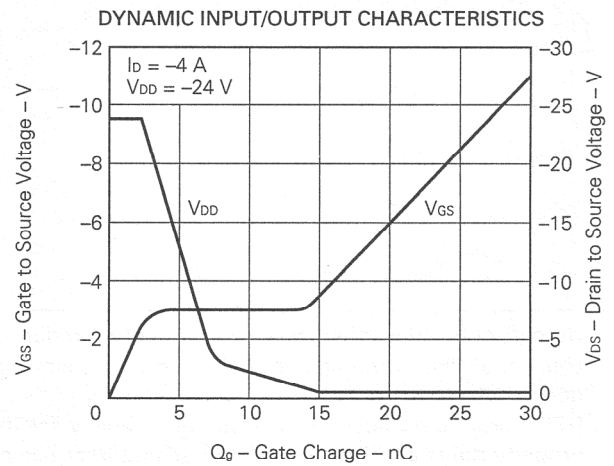
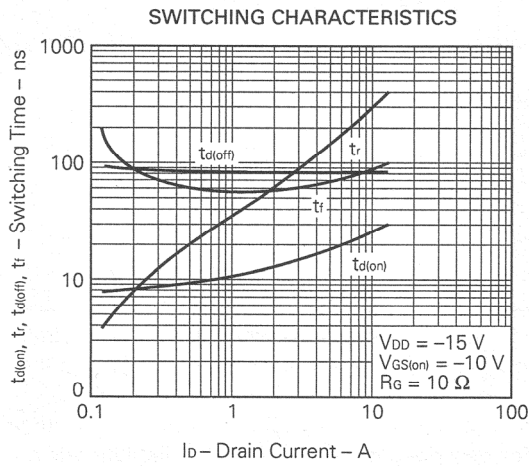
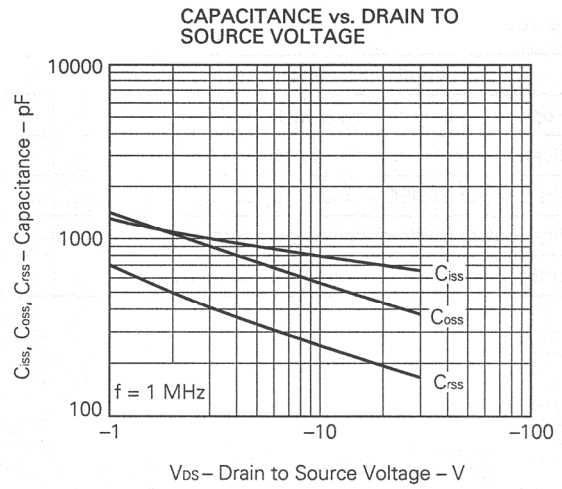
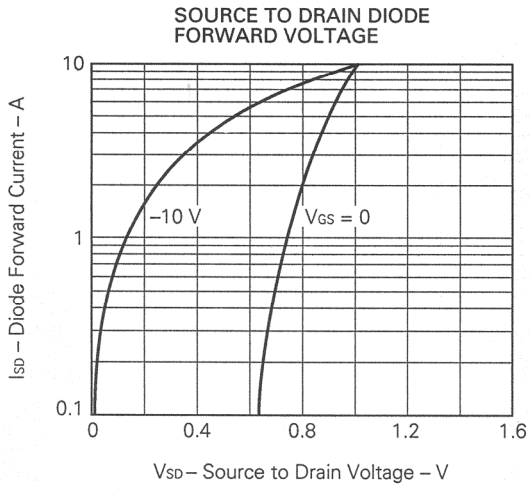
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH







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