



UC1823 UC2823 UC3823

High Speed PWM Controller

FEATURES

- Compatible with Voltage or Current-Mode Topologies
- Practical Operation @ Switching Frequencies to 1.0MHz
- 50ns Propagation Delay to Output
- High Current Totem Pole Output (1.5A peak)
- Wide Bandwidth Error Amplifier
- Fully Latched Logic with Double Pulse Suppression
- Pulse-by-Pulse Current Limiting
- Soft Start/Max. Duty Cycle Control
- Under-Voltage Lockout with Hysteresis
- Low Start Up Current (1.1mA)
- Trimmed Bandgap Reference (5.1V ±1%)

DESCRIPTION

The UC1823 family of PWM control ICs is optimized for high frequency switched mode power supply applications. Particular care was given to minimizing propagation delays through the comparators and logic circuitry while maximizing bandwidth and slew rate of the error amplifier. This controller is designed for use in either current-mode or voltage-mode systems with the capability for input voltage feed-forward.

Protection circuitry includes a current limit comparator, a TTL compatible shutdown port, and a soft start pin which will double as a maximum duty cycle clamp. The logic is fully latched to provide jitter free operation and prohibit multiple pulses at the output. An under-voltage lockout section with 800mV of hysteresis assures low start up current. During under-voltage lockout, the output is high impedance. The current limit reference (pin 11) is a DC input voltage to the current limit comparator. Consult specifications for details.

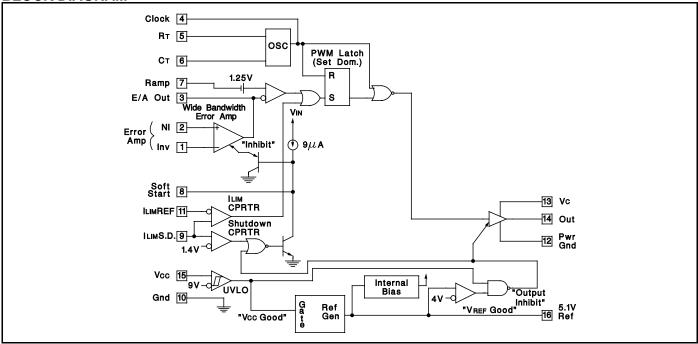
These devices feature a totem pole output designed to source and sink high peak currents from capacitive loads, such as the gate of a power MOSFET. The on state is defined as a high level.

ABSOLUTE MAXIMUM RATINGS

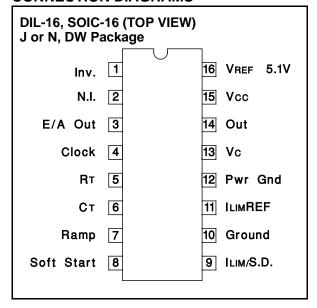
Supply Voltage (Pins 15, 13)	V
Output Current, Source or Sink (Pin14)	
DC	Α
Pulse (0.5μs)	Α
Analog Inputs (Pins 1, 2, 7, 8, 9, 11)0.3V to +6'	V
Clock Output Current (Pin 4)	Α
Error Amplifier Output Current (Pin 3) 5m/	Α
Soft Start Sink Current (Pin 8)	Α

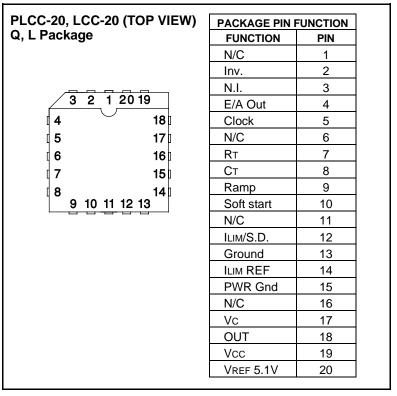
Consult Packaging Section of Databook for thermal limitations and considerations of packages.

BLOCK DIAGRAM



CONNECTION DIAGRAMS





ELECTRICAL CHARACTERISTICS: Unless otherwise noted, these specifications apply for RT = 3.65k, CT = 100 1 nF, Vcc = 15V, $0^{\circ}C < T_A < +70^{\circ}C$ for the UC3823, $-25^{\circ}C < T_A < +85^{\circ}C$ for the UC2823, and $-55^{\circ}C < T_A < +125^{\circ}C$ for the UC1823, $T_A = T_J$.

PARAMETER	TEST CONDITIONS		UC1823 UC2823			UC3823		
		MIN	TYP	MAX	MIN	TYP	MAX	
Reference Section								
Output Voltage	T _J = 25°C, lo = 1mA	5.05	5.10	5.15	5.00	5.10	5.20	V
Line Regulation	10 < Vcc < 30V		2	20		2	20	mV
Load Regulation	1 < lo < 10mA		5	20		5	20	mV
Temperature Stability*	TMIN < TA < TMAX		0.2	0.4		0.2	0.4	mV/°C
Total Output Variation*	Line, Load, Temp.	5.00		5.20	4.95		5.25	
Output Noise Voltage*	10Hz < f < 10kHz		50			50		μV
Long Term Stability*	T _J = 125°C, 1000 hrs.		5	25		5	25	mV
Short Circuit Current	VREF=0V	-15	-50	-100	-15	-50	-100	mA
Oscillator Section								
Initial Accuracy*	TJ=25°C	360	400	440	360	400	440	kHz
Voltage Stability*	10 < Vcc < 30V		0.2	2		0.2	2	%
Temperature Stability*	TMIN <ta <="" td="" tmax<=""><td></td><td>5</td><td></td><td></td><td>5</td><td></td><td>%</td></ta>		5			5		%
Total Variation*	Line, Temp.	340		460	340		460	kHz
Clock Out High		3.9	4.5		3.9	4.5		V
Clock Out Low			2.3	2.9		2.3	2.9	V
Ramp Peak*		2.6	2.8	3.0	2.6	2.8	3.0	V
Ramp Valley*		0.7	1.0	1.25	0.7	1.0	1.25	V
Ramp Valley to Peak*		1.6	1.8	2.0	1.6	1.8	2.0	V

^{*} These parameters are guaranteed by design but not 100% tested in production.

ELECTRICAL CHARACTERISTICS: Unless otherwise noted, these specifications apply for RT = 3.65k, CT = 1nF, Vcc = 15V, $0^{\circ}C$ < TA < $+70^{\circ}C$ for the UC3823, $-25^{\circ}C$ < TA < $+85^{\circ}C$ for the UC2823, and $-55^{\circ}C$ < TA < $+125^{\circ}C$ for the UC1823, TA = TJ.

PARAMETER	TEST CONDITIONS	UC1823 UC2823			UC3823			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Error Amplifier Section						_		
Input Offset Voltage				10			15	mV
Input Bias Current			0.6	3		0.6	3	μΑ
Input Offset Current			0.1	1		0.1	1	μΑ
Open Loop Gain	1 < Vo < 4V	60	95		60	95		dB
CMRR	1.5 < VCM < 5.5V	75	95		75	95		dB
PSRR	10 < Vcc < 30V	85	110		85	110		dB
Output Sink Current	VPIN 3 =1V	1	2.5		1	2.5		mA
Output Source Current	VPIN 3 = 4V	-0.5	-1.3		-0.5	-1.3		mA
Output High Voltage	IPIN 3 = -0.5mA	4.0	4.7	5.0	4.0	4.7	5.0	V
Output Low Voltage	IPIN 3 = 1mA	0	0.5	1.0	0	0.5	1.0	V
Unity Gain Bandwidth*		3	5.5		3	5.5		MHz
Slew Rate*		6	12		6	12		V/μS
PWM Comparator Section								
Pin 7 Bias Current	VPIN 7 = 0V		-1	-5		-1	-5	μΑ
Duty Cycle Range		0		80	0		85	%
Pin 3 Zero D.C. Threshold	VPIN 7 = 0V	1.1	1.25		1.1	1.25		V
Delay to Output*			50	80		50	80	ns
Soft-Start Section								
Charge Current	V _{PIN 8} = 0.5V	3	9	20	3	9	20	μΑ
Discharge Current	VPIN 8 = 1V	1			1			mA
Current Limit/Shutdown Section	1							
Pin 9 Bias Current	0 < VPIN 9 < 4V			±10			±10	μΑ
Current Limit Offset	VPIN 11 = 1.1V			15			15	mV
Current Limit Common Mode Range (VPIN 11)		1.0		1.25	1.0		1.25	V
Shutdown Threshold		1.25	1.40	1.55	1.25	1.40	1.55	V
Delay to Output*			50	80		50	80	ns
Output Section								
Output Low Level	IOUT = 20mA		0.25	0.40		0.25	0.40	V
	IOUT = 200mA		1.2	2.2		1.2	2.2	V
Output High Level	IOUT = -20mA	13.0	13.5		13.0	13.5		V
	IOUT = -200mA	12.0	13.0		12.0	13.0		V
Collector Leakage	Vc = 30V		100	500		100	500	μΑ
Rise/Fall Time*	CL = 1nF		30	60		30	60	ns
Under-Voltage Lockout Section								
Start Threshold		8.8	9.2	9.6	8.8	9.2	9.6	V
UVLO Hysteresis		0.4	0.8	1.2	0.4	0.8	1.2	V
Supply Current								
Start Up Current	Vcc = 8V		1.1	2.5		1.1	2.5	mA
Icc	VPIN 1, VPIN 7, VPIN 9 = 0V, VPIN 2 = 1V		22	33		22	33	mA

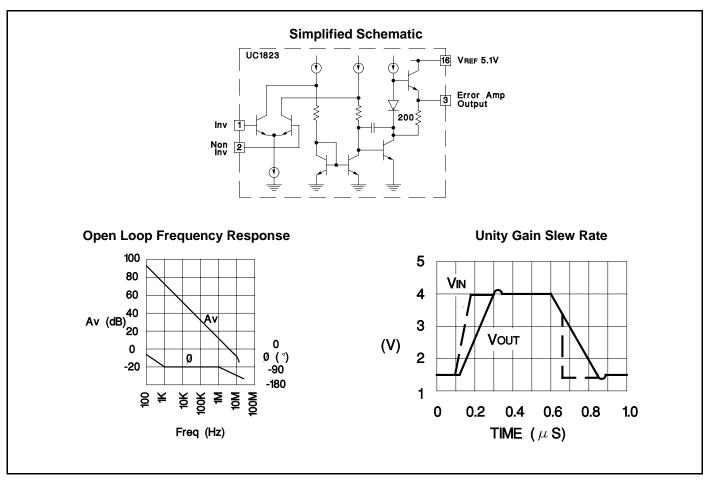
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UC1823 PRINTED CIRCUIT BOARD LAYOUT CONSIDERATIONS

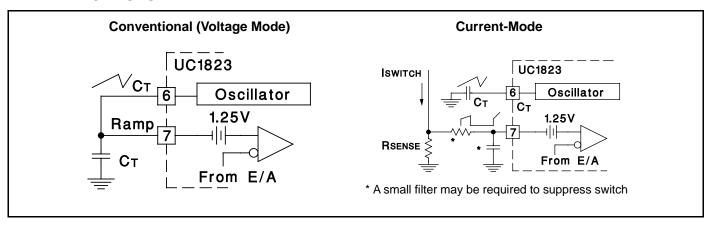
High speed circuits demand careful attention to layout and component placement. To assure proper performance of the UC1823, follow these rules. 1) Use a ground plane. 2) Damp or clamp parasitic inductive kick energy from the gate of driven MOSFET. Don't allow the output pins to ring below ground. A series gate resistor or a shunt 1 Amp Schottky diode at the output pin will serve

this purpose. 3) Bypass Vcc, Vc, and VREF. Use $0.1\mu F$ monolithic ceramic capacitors with low equivalent series inductance. Allow less than 1 cm of total lead length for each capacitor between the bypassed pin and the ground plane. 4) Treat the timing capacitor, CT, like a bypass capacitor.

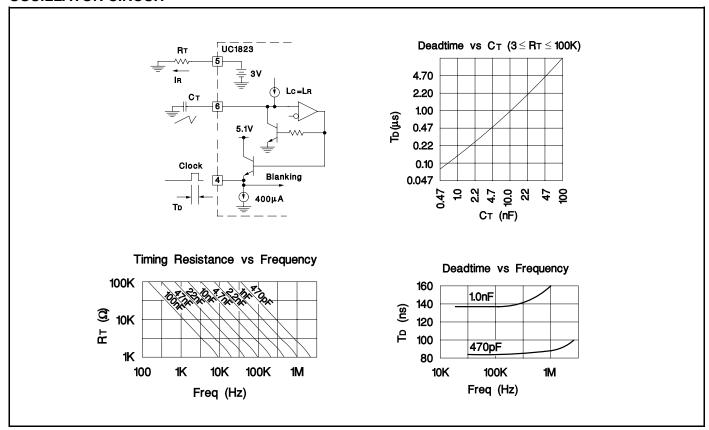
ERROR AMPLIFIER CIRCUIT



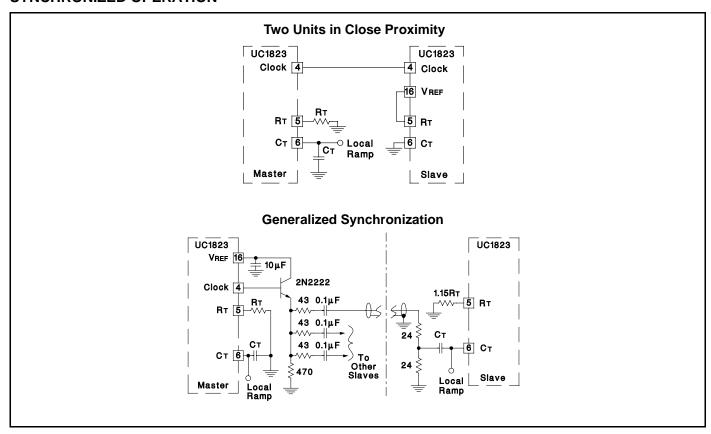
PWM APPLICATIONS



OSCILLATOR CIRCUIT

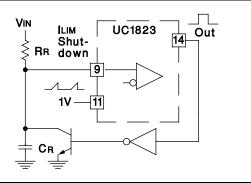


SYNCHRONIZED OPERATION

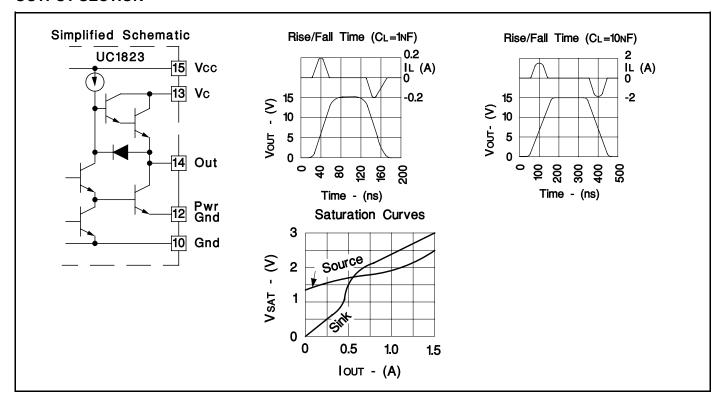


CONSTANT VOLT-SECOND CLAMP CIRCUIT

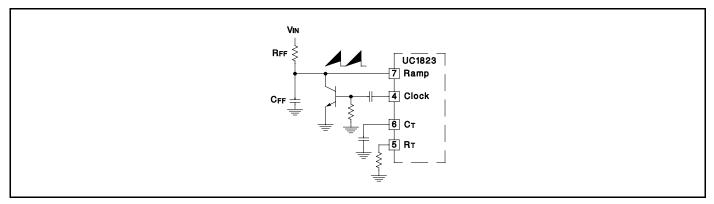
The circuit shown here will achieve a constant volt-second product clamp over varying input voltages. The ramp generator components, RT and CR are chosen so that the ramp at Pin 9 crosses the 1V threshold at the same time the desired maximum volt-second product is reached. The delay through the inverter must be such that the ramp capacitor can be completely discharged during the minimum deadtime.



OUTPUT SECTION



FEED FORWARD TECHNIQUE FOR OFF-LINE VOLTAGE MODE APPLICATION



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UC1823, High Speed PWM Controller

Device Status: Active

- > Description
- > Features
- > Datasheets
- > Pricing/Samples/Availability
- > Application Notes
- > Applications

Parameter Name	UC1823
Shutdown	Yes
Output Type	Single, Totem Pole
Output Current (mA)	1500
Frequency (max) (kHz)	1000
Pulse - by - Pulse Isense	Yes
Reference Voltage (V)	5.1
Vref tol (%)	1
Startup Current (uA)	1100
Duty Cycle (max) (%)	100
Operating Supply Current (mA)	22
Operating Supply (max) (V)	30
Operating Supply (min) (V)	8.4
PWM Outputs (#)	1
Error Amplifier GBW (mHz)	5.5

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To view the following documents, Acrobat Reader 3.x is required.

To download a document to your hard drive, right-click on the link and choose 'Save'.

Price/unit

Datasheets

Full datasheet in Acrobat PDF: <u>slus219.pdf</u> (409 KB)

Pricing/Samples/Availability

Orderable <u>Device</u>	<u>Package</u>	<u>Pins</u>	<u>Temp</u> (°C)	<u>Status</u>	USD (100- 999)	Pack Qty	<u>DSCC</u> <u>Number</u>	<u>Availability /</u> <u>Samples</u>
5962- 89905012A	<u>L</u>	20	-55 TO 125	ACTIVE	50.74	1		Check stock or order
5962- 8990501EA	<u>J</u>	16	-55 TO 125	ACTIVE	27.92	1		Check stock or order
UC1823J	<u>J</u>	16	-55 TO 125	ACTIVE	13.51	1		Check stock or order
UC1823J883B	<u>J</u>	16	-55 TO 125	ACTIVE	27.92	1		Check stock or order
UC1823L	<u>L</u>	20	-55 TO 125	ACTIVE	30.91	1		Check stock or order
UC1823L883B	<u>L</u>	20	-55 TO 125	ACTIVE	50.74	1	5962- 89905012A	Check stock or order

Application Reports

• <u>U-131 Simple Switchmode Lead-Acid Battery Charger</u> (SLUA055 - Updated: 09/05/1999)

Table Data Updated on: 9/13/2000

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