High-Speed CMOS 2K x 9, 4K x 9 FIFO Buffer Memories

QS7203
QS7204

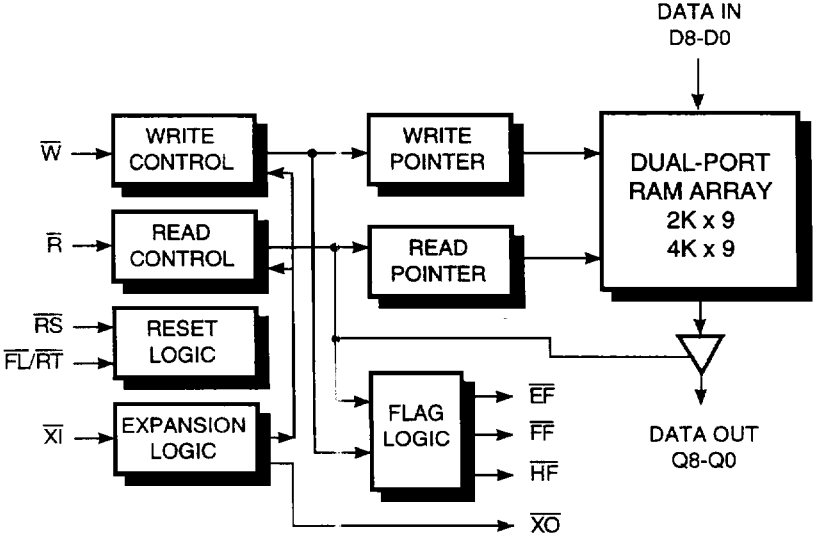
FEATURES

- 10 ns flag and data access times
- Fully Asynchronous Read and Write
- Zero fall-through time
- Expandable in depth with no speed loss
- TTL input and output level compatible
- Retransmit capability
- Dual-Port RAM based cell technology
- Available in PDIP, SOJ, PLCC
- Low Power with industry standard pinouts

DESCRIPTION

The QS7203 and QS7204 are 2K x 9 and 4K x 9 FIFOs, respectively. These FIFOs use a dual-port RAM based architecture and have independent read and write pointers. This allows high-speed and zero fall-through time. The read and write pointers are incremented on the rising edges of the Read and Write lines. The flag circuitry is based on a patented high-speed design, giving precise half-full, full, and empty conditions. These flags also prevent the FIFO from being written into when full or being read from when empty. These FIFOs are easily cascadable to any depth and expandable to any width without any speed penalty. Retransmit resets the read pointer to memory location zero, and is useful for data communications, digital filtering, and video line doubling applications.

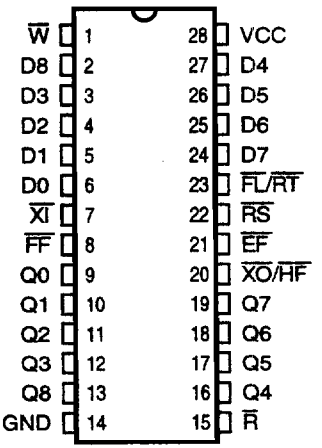
FUNCTIONAL BLOCK DIAGRAM



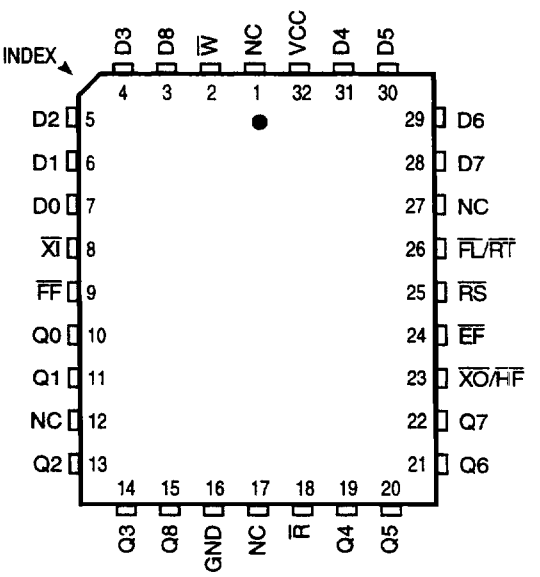
Note: $\overline{XO}$ and $\overline{HF}$ share the same pin so the half-full flag is available only in standalone, not depth expansion mode.

PINOUTS (All Pins Top View)

PDIP, SOIC, SOJ



PLCC



PIN DESCRIPTIONS

Name	I/O	Description
Di	I	Data Inputs
Qi	O	Data Outputs
$\overline{R}$	I	Read Clock
$\overline{W}$	I	Write Clock
$\overline{EF}$	O	Empty Flag
$\overline{FF}$	O	Full Flag
$\overline{RS}$	I	Reset
$\overline{FL/RT}$	I	First Load/Retransmit
$\overline{XI}$	I	Expansion Clock In
$\overline{XO/HF}$	O	Expansion Clock Out/ Half Full Flag

FUNCTION TABLES

RESET AND RETRANSMIT FUNCTION TABLE

Mode	INPUTS $\overline{RS}$	$\overline{FL}/\overline{RT}$	$\overline{XI}$	INTERNAL STATUS Read Pointer	Write Pointer	OUTPUTS $\overline{EF}$	$\overline{FF}$	$\overline{HF}$
Reset	L	X	L	Location Zero	Location Zero	L	H	H
Retransmit	H	L	L	Location Zero	Unchanged	(3)	(3)	(3)
Read/Write	H	H	L	Increment(1)	Increment(2)	(4)	(4)	(4)

Notes:
1. The Read Pointer will increment if the FIFO is not empty.
2. The Write flag will increment if the FIFO is not full.
3. The flags will change after the retransmit operation and will correspond to the read pointer being at location zero.
4. The flags will reflect the relative locations of the read and write pointers.

RESET AND FIRST LOAD FUNCTION TABLE

Mode	INPUTS $\overline{RS}$	$\overline{FL}/\overline{RT}$	$\overline{XI}$	INTERNAL STATUS Read Pointer	Write Pointer	OUTPUTS $\overline{EF}$	$\overline{FF}$	$\overline{HF}$
Reset	L	L	(1)	Location Zero	Location Zero	L	H	H
Retransmit	L	H	(1)	Location Zero	LOCATION ZERO	(3)	(3)	(3)
Read/Write	H	(2)	(1)	Increment(1)	Increment(2)	(4)	(4)	(4)

Notes:
1. The Expansion In ($\overline{XI}$) is connected to the Expansion Out ($\overline{XO}$) of the previous device.
2. The device with $\overline{FL}$ tied low will receive the first N writes and first N reads, where N is the FIFO size. On the Nth write, the $\overline{XO}$ pulse is sent to the next device to indicate that it will receive the (N+1)th write. Similarly on the Nth read another $\overline{XO}$ pulse is sent to the next device to indicate that it will output the (N+1) th read.
3. The read and write pointers will be activated according to whether the FIFO received an $\overline{XO}$ pulse, or whether they were the first device in the daisy chain. The flags will reflect the empty or full conditions for the individual FIFOs. To create the composite Full and Empty flags, an OR-ing of the individual flags is required.
4. The flags will reflect the relative locations of the read and write pointers.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage to Gound	–0.5 to +7.0V
DC Output Voltage V_{OUT}	–0.5 to Vcc + 0.5V
DC Input Voltage V_{IN}	–0.5 to Vcc + 0.5V
AC Input Voltage (Pulse Width ≤ 20ns)	–3.0V
DC Input Diode Current with V_{IN} < 0	–20 mA
DC Output Current with V_{IN} > Vcc	20 mA
DC Output Diode Current with V_{OUT} < 0	–50 mA
DC Output Current with V_{OUT} > Vcc	50 mA
DC Output Current Max. Sink Current/Pin	+70 mA
DC Output Current Max. Source Current/Pin	–30 mA
Total DC Ground Current	(NxI_{OL} + MxΔI_{CC}) mA
Total DC Vcc Power Supply Current	(NxI_{OH} + MxΔI_{CC}) mA
(N = Number of Outputs, M = Number of Inputs)	
T_{STG} StorageTemperature	–65°C to +165°C

Note: Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to this device resulting in functional or reliability type failures.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Commercial V_{CC} = 5V ± 10%, T_A = 0°C to +70°C

Symbol	Parameter	Test Conditions	Min	Max	Units
V_{IH}	Input HIGH Voltage	Logic HIGH for All Inputs	2.0	6.0	V
V_{IL}	Input LOW Voltage	Logic LOW for All Inputs	—	0.8	V
V_{OH}	Output HIGH Voltage	I_{OH} = –2 mA, V_{CC} = 4.5V	2.4	—	V
V_{OL}	Output LOW Voltage	I_{OL} = 8 mA, V_{CC} = 4.5V	—	0.4	V
$\lvert I_{OZ} \rvert$	Output Leakage	V_{CC} = 5.5V, V_{OUT} = V_{CC} or 0V	—	10	µA
$\lvert I_{IL} \rvert$	Input Leakage	V_{CC} = 5.5V, GND < V_{IN} < V_{CC}	—	1	µA

CAPACITANCE

T_A = 25°C, f = 1.0 MHz

Name	Description	Conditions	Typ	Max	Units
C_{IN}	Input Capacitance	V_{IN} = 0V	5	8	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	5	8	pF

Note: Capacitance is guaranteed but not tested.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Com	Units
I_{CC1}[1]	Operating Current V_{CC} = Max., Outputs Open	100	mA
I_{CC2}	Standby Current $\overline{R}$ = $\overline{W}$ = $\overline{RS}$ = $\overline{FL}/\overline{RT}$ = V_{IH}	15	mA
I_{SB}	Power Down Current All Inputs at V_{HC} or V_{IC} $\overline{R}$ = $\overline{W}$ = $\overline{RS}$ = $\overline{FL}/\overline{RT}$ = V_{HC}	5	mA

Note:
1. I_{CC} is tested at 30 MHz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Commercial Vcc = 5V ± 10%, T_A = 0°C to +70°C

READ CYCLE TIMING

Sym.	Parameter	-10	-12	-15	-20	-25	-35	-50	-80	Unit	Type
t_{RF}	Read Frequency, MHz[2]	45.5	43.5	40	33	28	22	15	10	MHz	Min
t_{RC}	Read Cycle Time	22	23	25	30	35	45	65	100	ns	Min
t_A	Read Access Time	10	12	15	20	25	35	50	80	ns	Max
t_{RR}	Read Recovery Time	7	8	10	10	10	10	15	20	ns	Min
t_{RPW}	Read Pulse Width[1]	15	15	15	20	25	35	50	80		
t_{RLZ}	$\overline{R}$ Data Bus Low-Z[2]	3	3	3	3	3	3	3	3		
t_{WLZ}	$\overline{W}$ Data Bus Low-Z[2,3]	3	3	3	3	3	3	3	3		
t_{DV}	$\overline{R}$ HIGH to Data Hold Time	5	5	5	5	5	5	5	5		
t_{RHZ}	$\overline{R}$ to Data High-Z[2]	10	12	14	18	18	20	30	35		

WRITE CYCLE TIMING

Sym.	Parameter	-10	-12	-15	-20	-25	-35	-50	-80	Unit	Type
t_{WF}	Write Frequency, MHz[2]	45.5	43.5	40	33	28	22	15	10	ns	Min
t_{WC}	Write Cycle Time	22	23	25	30	35	45	65	100		
t_{WPW}	Write Pulse Width[1]	15	15	15	20	25	35	50	80		
t_{WR}	Write Recovery Time	7	8	10	10	10	10	15	20		
t_{DS}	Write Data Setup Time	8	8	9	12	15	18	30	40		
t_{DH}	Write Data Hold Time	0	0	0	0	0	0	0	0		

RESET AND TRANSMIT CYCLE TIMING

Sym.	Parameter	-10	-12	-15	-20	-25	-35	-50	-80	Unit	Type
t_{RSC}	Reset Cycle Time	17	20	25	30	35	45	65	100	ns	Min
t_{RS}	Reset Pulse Width[1]	10	12	15	20	25	35	50	80		
t_{RSS}	Reset Setup Time	10-	12	15	20	25	35	50	80		
t_{RSR}	Reset Recovery Time	7	8	10	10	10	10	15	20		
t_{RTC}	Retransmit Cycle Time	19	20	25	30	35	45	65	100		
t_{RT}	Retransmit Pulse Width[1]	12	12	15	20	25	35	50	80		
t_{RTS}	Retransmit Setup Time	10	12	15	20	25	35	50	80		
t_{RTR}	Retransmit Recovery Time	7	8	10	10	10	10	15	20		

Notes: These timings are measured as defined ir AC Test Conditions.

1. Pulse widths less than the specified minimum value may upset the internal pointers and are not allowed.
2. These values are guaranteed by design and not tested
3. This applies to the read data flow-through mode only.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Commercial Vcc = 5V ± 10%, T_A = 0°C to +70°C

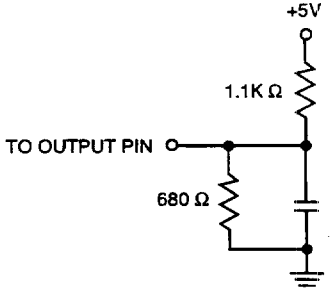
FLAG TIMING

Sym.	Parameter	-10	-12	-15	-20	-25	-35	-50	-80	Unit	Type
t_{REF}	Read Low to $\overline{EF}$ Low	10	12	15	20	25	30	45	60	ns	Max
t_{RFF}	Read High to $\overline{FF}$ High	13	14	15	20	25	30	45	60		
t_{RHF}	Read High to $\overline{HF}$ High	16	17	19	20	25	30	45	60		
t_{RPE}	Read Pulse After $\overline{EF}$ High	10	12	15	20	25	30	50	80	ns	Min
t_{WEF}	Write Low to $\overline{EF}$ Low	10	12	15	20	25	30	45	60	ns	Max
t_{WFF}	Write High to $\overline{FF}$ High	13	14	15	20	25	30	45	60		
t_{WHF}	Write High to $\overline{HF}$ High	16	17	19	20	25	30	45	60		
t_{WPE}	Write Pulse After $\overline{EF}$ High	10	12	15	20	25	30	50	80	ns	Min
t_{EFL}	Reset Low to $\overline{EF}$ Low	10	12	15	20	25	30	45	60	ns	Max
t_{FFH}	Reset High to $\overline{FF}$ High	13	14	15	20	25	30	45	60		
t_{HFH}	Reset High to $\overline{HF}$ High	16	17	19	20	25	30	45	60		

EXPANSION TIMING

Sym.	Parameter	-10	-12	-15	-20	-25	-35	-50	-80	Unit	Type
t_{XOL}	Read/Write to $\overline{XO}$ Low	12	12	15	20	25	35	50	80	ns	Min
t_{XOH}	Read/Write to $\overline{XO}$ High	12	12	15	20	25	35	50	80		
t_{XI}	$\overline{XI}$ Pulse Width	10	12	15	20	25	35	50	80		
t_{XIR}	$\overline{XI}$ Recovery Time	7	8	10	10	10	10	10	10		
t_{XIS}	$\overline{XI}$ Setup Time	7	8	10	15	15	15	15	15		

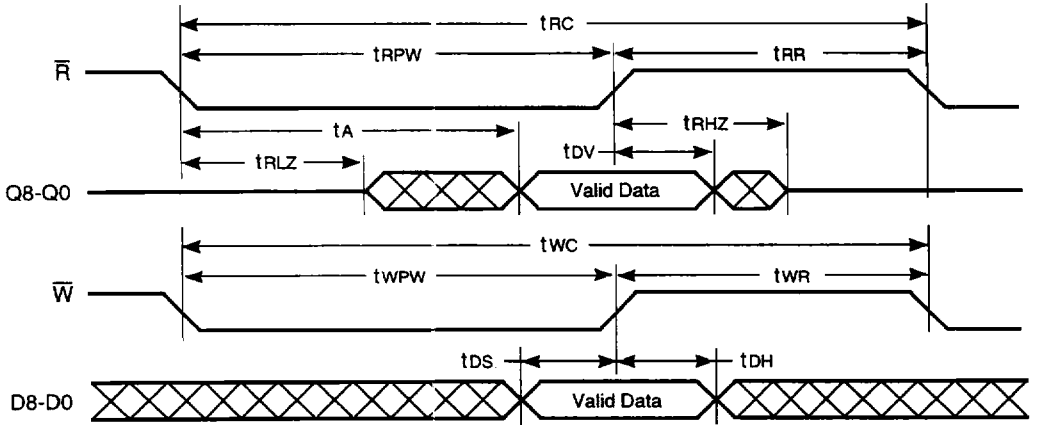
AC TEST CONDITIONS



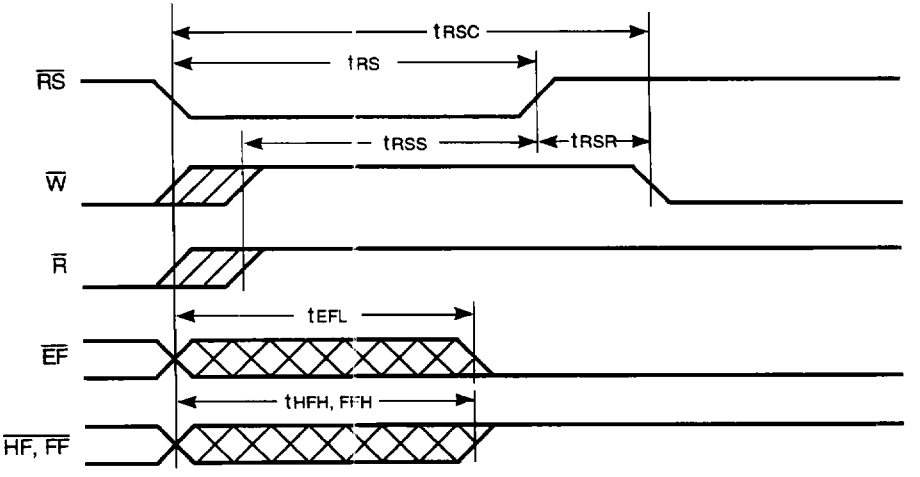
Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3 ns
Input Timing References Levels	1.5V
Output Reference Levels	1.5V

TIMING DIAGRAMS

ASYNCHRONOUS READ AND WRITE OPERATIONS

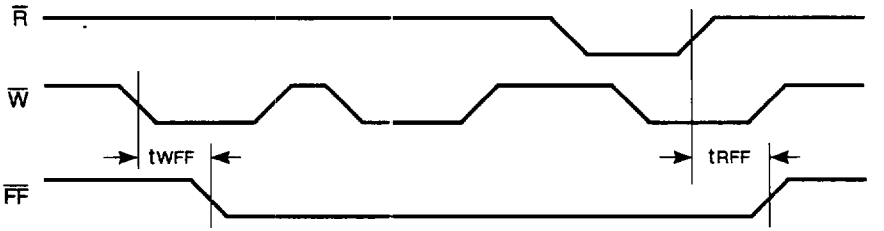


RESET TIMING

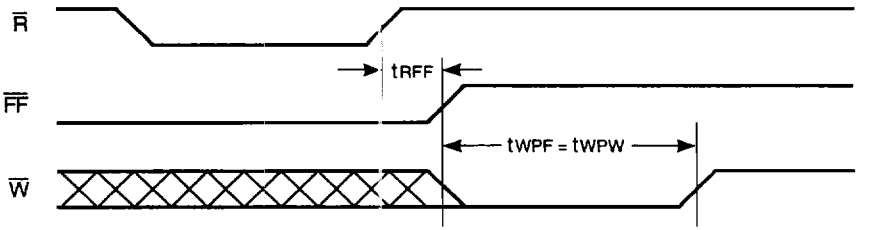


Notes:
1. Read and Write have to be at a HIGH level around the rising edge of Reset. The flags may change during reset but are valid at tRSC.

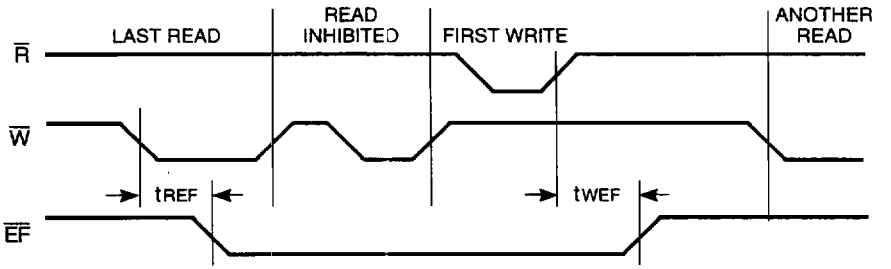
FULL FLAG BEHAVIOR FROM LAST WRITE TO FIRST READ



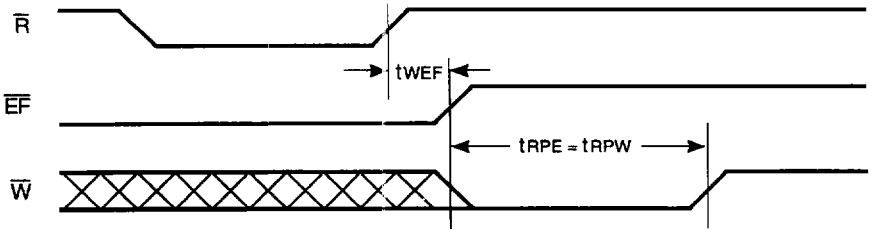
FULL FLAG AND REQUIRED WRITE PULSE AT FULL CONDITION



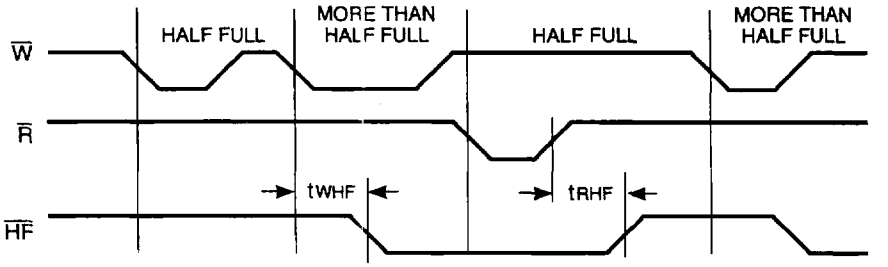
EMPTY FLAG BEHAVIOR FROM LAST READ TO FIRST WRITE



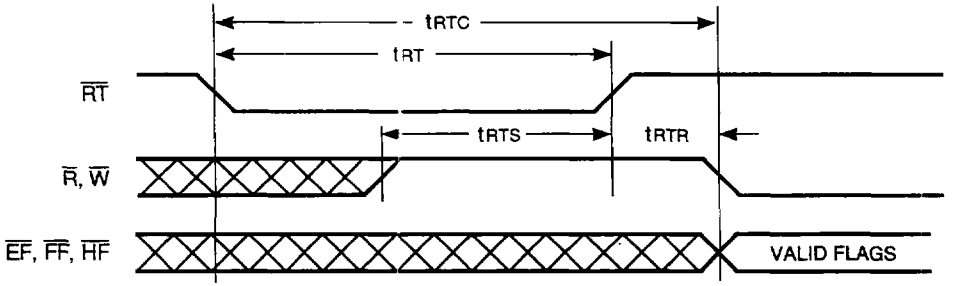
EMPTY FLAG AND REQUIRED WRITE PULSE AT EMPTY CONDITION



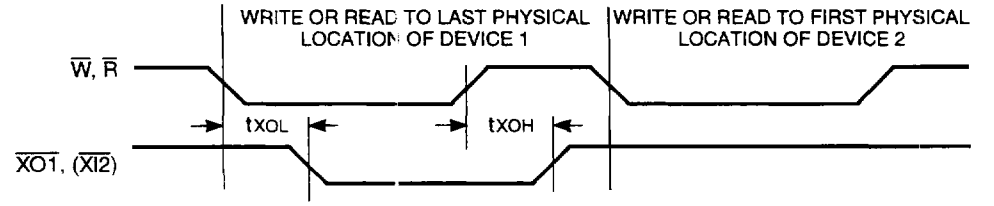
HALF FULL FLAG TIMING



RETRANSMIT FUNCTION TIMING

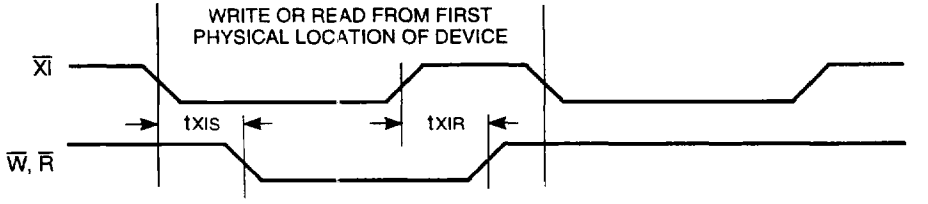


EXPANSION OUT TIMING

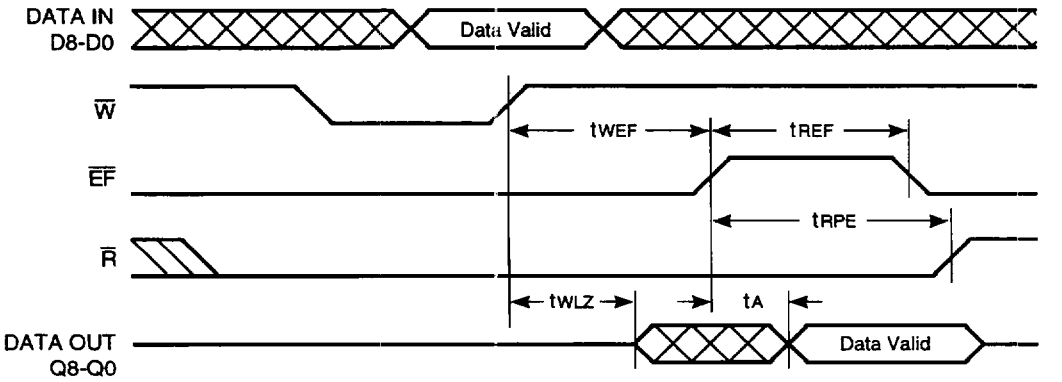


Note:
1. The Expansion Out of Device 1 is connected to the Expansion In of Device 2.

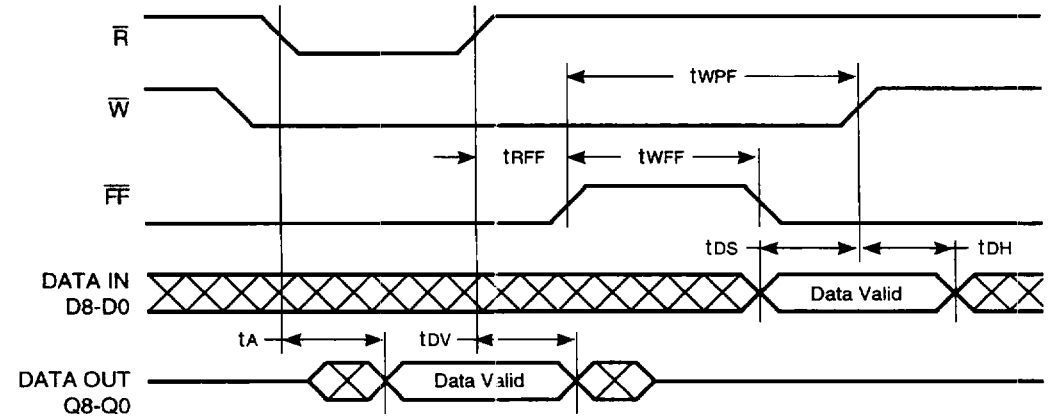
EXPANSION IN TIMING



READ DATA FLOW-THROUGH MODE



WRITE DATA FLOW-THROUGH MODE



OPERATIONAL DESCRIPTION AND APPLICATION INFORMATION

The QS7203 and QS7204 are 1Kx9 and 2Kx9 FIFOs respectively. These FIFOs use a dual-port RAM based architecture and have independent read and write pointers. This allows high speed and zero fall-through time. The Write line causes data to be written into the FIFO. The Read line causes data to be read from the FIFO. The Read line also activates the three-state outputs to present the read data. The read and write pointers are incremented on the rising edges of the Read and Write lines. The flag circuitry is based on a reliable sequential design giving precise half full, full, and empty conditions. These flags also prevent the FIFO from being written into when full or being read from when empty. Depth expansion pins are provided which allow these FIFOs to be expanded in depth without speed penalty. Retransmit capability is provided. Activating the Retransmit pin resets the read pointer to zero, and is useful for data communications and digital filtering applications.

SIGNAL DESCRIPTION

DATA INPUTS

D8-D0
The Data In lines D8 to D0 provide data to be written into the FIFO. Note: unused inputs must be tied to Vcc or Gnd.

CONTROL INPUTS

Reset ($\overline{RS}$)
The Reset input resets the Read and Write pointers and the flags to zero. The FIFO must be reset at power-up to insure proper operation of the pointers and flags. This is done by asserting the Reset line to a LOW state, which causes the FIFO flags to be set to empty. This causes the Empty flag is asserted and the Full and Half Full flags to be deasserted. Read and Write lines must be HIGH for t_{RSS} before and t_{RSR} after the rising edge of the Reset signal for a valid reset operation.

Write ($\overline{W}$)
The Write line caused data to be written into the FIFO. A write cycle is initiated by the falling edge of the Write signal. A write will occur if the full flag was not asserted, indicative of at least one empty location in the FIFO. Data is stored in the FIFO on the rising edge of the Write signal using the data setup and hold times specified. Data is stored in a sequential manner in the FIFO, and the read and write operations can be asynchronous. The falling edge of the Write signal asserts the Half full and Full flags when the next word after half full is written and when the last word has been written, respectively. The rising edge of the Write line deasserts the Empty flag when the first write is performed after an empty or reset condition. When the Full flag is asserted, subsequent writes are blocked. The user can apply a write pulse after the full condition is deasserted.

Read ($\overline{R}$)
The Read signal causes data to be read from the FIFO. A read cycle is initiated by the falling edge of the Read signal. A read is performed if the Empty flag is not asserted, indicative of at least one word being present in the FIFO. The data is accessed in a First-In-First-Out basis asynchronous to the Write operations. After the Read control is deasserted the data outputs go from a valid state into high-impedance. The outputs remain in high-impedance until the next read cycle. When all the data is read on the last read cycle, the Empty Flag is asserted, and will inhibit any subsequent reads. The outputs will be in high-impedance for subsequent read operation until a write occurs that deasserts the Empty Flag, allowing a read cycle to begin. The outputs may also be in high impedance when the FIFOs are cascaded in depth. In this case, only the active FIFO asserts data , and the other FIFOs data outputs are in high-impedance. The falling edge of the read signal will set the Empty Flag during the read of the last word in the FIFO. The rising edge of the Read signal will deassert the Half Full and the Full Flags when the FIFO has reached half full and when the FIFO was full, respectively.

First Load/ Retransmit ($\overline{FL}/\overline{RT}$)
This is a dual purpose input. In the depth expansion mode, this pin indicates the first FIFO device that will be loaded or read from after a reset operation. In the standalone or width expansion mode (when the the expansion input is grounded) this pin initiates the a retransmit function.

Retransmit resets the read pointer to zero. The Read and Write signals must be HIGH before and after the rising edge of the retransmit pulse. The retransmit feature is useful when the same data needs to be read again without rewriting it into the FIFO. Pulsing retransmit pin will cause the read pointer to be reset to zero and the previously read data can be read again. The flags will change according to the relative location of the pointers after the retransmit pulse.

Expansion In ($\overline{XI}$)
This is a dual purpose pin. When it is grounded then it indicates that the FIFO is a standalone device. When it is not grounded, it indicates that the FIFO is in the depth expansion mode. In the depth expansion mode this pin is connected to the $\overline{XO}$ pin of the previous device.

DATA OUTPUTS

Data Outputs Q8-Q0
The 9-bit data output bus, Q8-Q0 receives the read data from the FIFO. It is active whenever the Read signal is low. It is in a high impedance state when the Read signal is high. It is also in high impedance when the FIFO Empty Flag is active (i.e., when the FIFO is empty).

CONTROL OUTPUTS

Full Flag ($\overline{FF}$)
The Full Flag indicates that the FIFO is full. The Full Flag is asserted when there is only one empty location in the FIFO and a falling edge of the Write signal initiates the last write operation. The rising edge of the Read signal deasserts the flag, as at least one location has become available.

Empty Flag ($\overline{EF}$)
The Empty Flag indicates the FIFO is empty. It is asserted when there is only one word in the FIFO, and a falling edge of the Read signal initiates the last read operation. The rising edge of the Write signal deasserts the flag, as one word is now present in the FIFO.

Expansion Out/Half Full Flag ($\overline{XO}/\overline{HF}$)
This is a dual purpose flag. In the single device mode, the Expansion In is grounded and the Half Full Flag output is present on this pin. Whenever the FIFO is more than half full the flag remains asserted . When the FIFO is exactly half full and the next falling edge of the Write signal asserts the flag. The rising edge of read that causes the FIFO to be half full, will deassert the Half Full Flag. It will remain asserted until the FIFO is half full or less than half full. The name given to the flag is half full, but it is asserted on the one plus the half full condition.

In the depth expansion mode, the Expansion Out is connected to the Expansion In of the next device. This causes the next device to perform write or read operations.

OPERATING MODES

SINGLE DEVICE MODE

A FIFO is in standalone mode when the Expansion In control is grounded. In this mode the Half Full Flag is available on the shared $\overline{XO/HF}$ line. Figure 1 shows the standalone mode and this applies to FIFO width expansion, as shown in Figure 2.

DEPTH EXPANSION MODE

A FIFO is in the depth expansion mode when the Expansion In control is not grounded but tied to the Expansion Out pin of the previous FIFO. Using the depth expansion mode, the QS7203/04 can be easily cascaded to create FIFOs of larger depth. The devices are cascaded as shown in Figure 3. In the depth expansion mode, the device that receives the first word of data has its First Load input grounded. The other devices have their First Load inputs in the high state. Two 4-input OR gates are required to create the composite Full and Empty Flags for the FIFO array. In using the depth expansion mode, care must be taken to keep the traces short between the Expansion In of one device to the Expansion Out of the next device to minimize crosstalk noise.

FLOW-THROUGH MODES

Flow-through modes refer to the internal operation of the FIFO in empty and full conditions. Flow-through modes allow data to flow directly through the FIFO from input to output under the appropriate empty and full conditions.

Two types of flow-through modes, a Read flow-through and a Write flow-through, are supported by the FIFO. In the Read flow-through, mode the FIFO is empty and the read side is waiting for data from a write. Read flow-through is represented by an empty FIFO that has its Read line held low, and a write occurs. This rising edge of the Write would deassert the Empty Flag and cause valid data to appear on the outputs after a certain time delay of $t_{WEF} + t_A$. The Read line being low would cause the data to be read and also assert the Empty Flag once again. The user must raise the Read line in order to increment the read pointer.

In the Write flow-through mode, the FIFO is full and the write side is waiting for a word location to be made available by a read. A Write flow-through operation permits the writing of a single word of data immediately after reading one word of of data from a full FIFO. This is similar to the Read flow-through case, and the Write line must toggled to increment the write pointer.

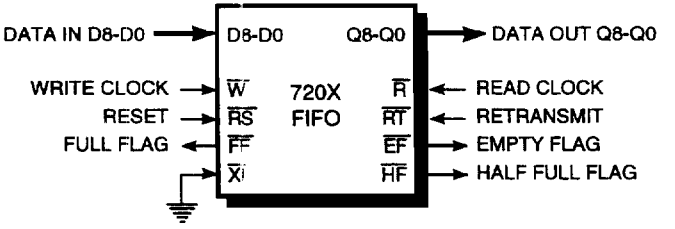


Figure 1. The FIFO in Standalone Mode.

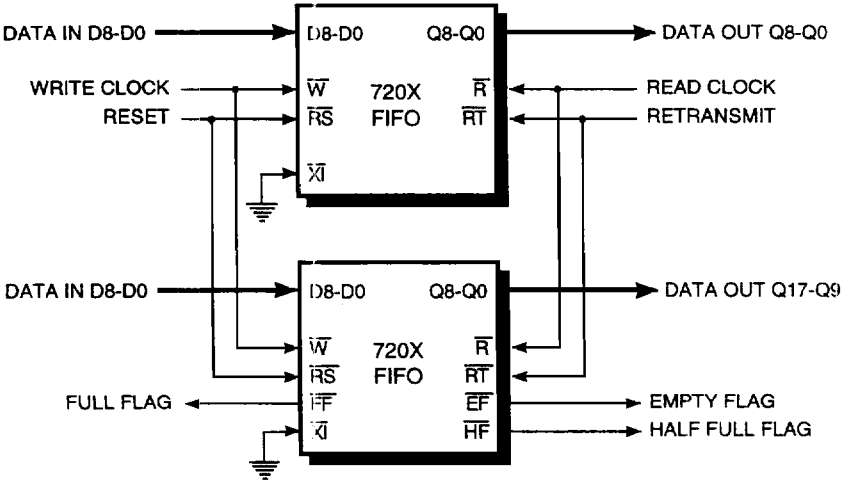
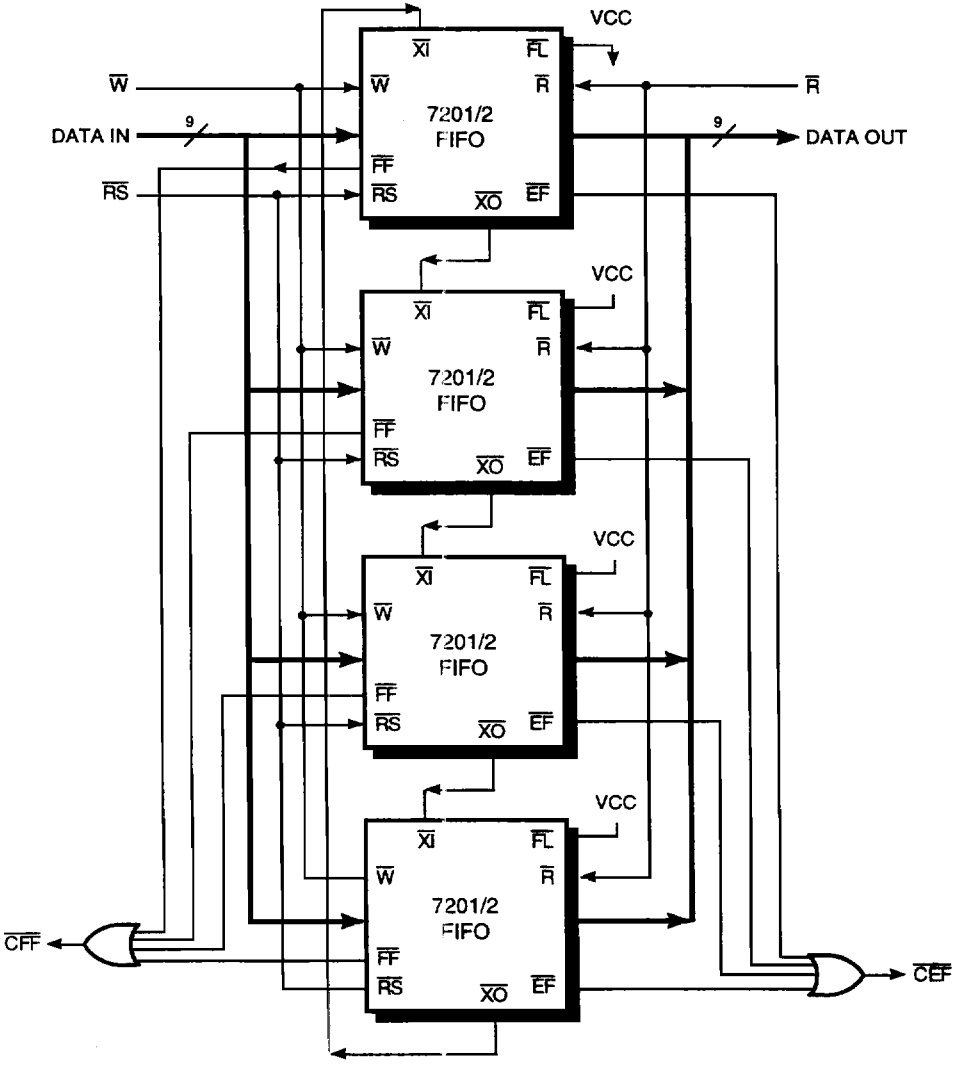


Figure 2. A 18-bit Wide FIFO Using 2 FIFOs



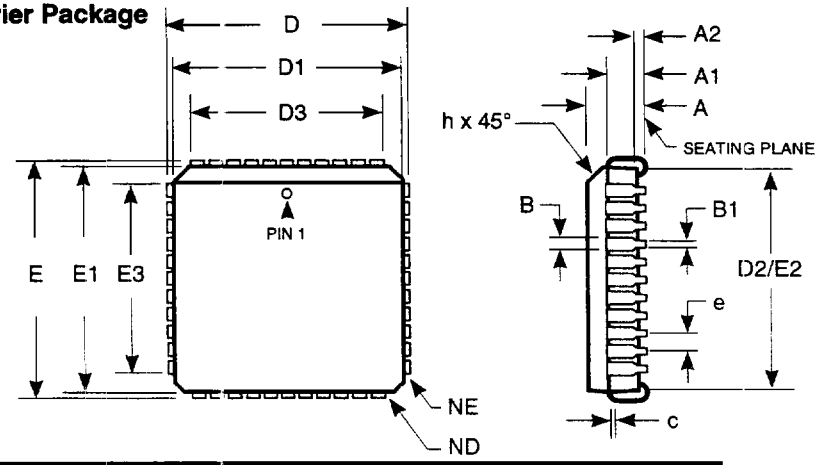
Note: The composite Empty and Full Flags require the OR-ing of the individual Empty and Full Flags, respectively

Figure 3. Building a 4N-deep FIFO Using Four N-deep FIFOs

PLCC (Package Code J/JR)

Leaded Chip Carrier Package

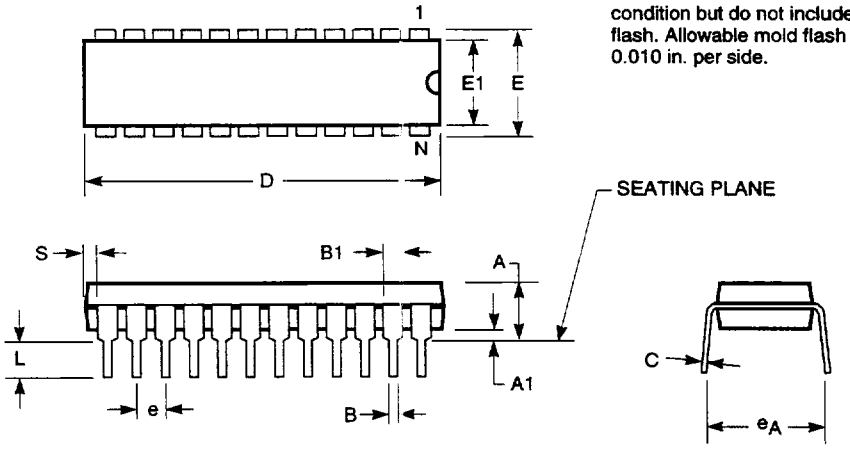
Notes:
1. Refer to applicable symbol list.
2. All dimensions are in inches.
3. N is the number of lead positions.
4. Dimensions D1 and E1 are to be measured at maximum material condition but do not include mold flash. Allowable mold flash is 0.010 in. per side.
5. Lead coplanarity is 0.004 in. maximum.



JEDEC#	MO-047 AB		MO-052 AE		MO-047 AD					
DWG#	PL28A		PL32A		PL52A		PL68A		PL84A	
Symbol	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.
A	0.165	0.180	0.115	0.135	0.165	0.180	0.165	0.180	0.165	0.180
A1	0.090	0.120	0.070	0.090	0.090	0.120	0.090	0.120	0.090	0.120
A2	0.015	0.035	0.015	0.035	0.015	0.035	0.015	0.035	0.015	0.035
B	0.026	0.032	0.026	0.032	0.026	0.032	0.026	0.032	0.026	0.032
B1	0.014	0.019	0.014	0.019	0.014	0.019	0.014	0.019	0.014	0.019
C	0.009	0.012	0.009	0.012	0.009	0.012	0.009	0.012	0.009	0.012
D	0.485	0.495	0.485	0.495	0.785	0.795	0.985	0.995	1.185	1.195
D1	0.450	0.456	0.448	0.452	0.750	0.756	0.950	0.956	1.150	1.156
D2	0.390	0.430	0.390	0.430	0.690	0.730	0.890	0.930	1.090	1.130
D3	0.300 REF		0.300 REF		0.600 REF		0.800 REF		1.000 REF	
E	0.485	0.495	0.585	0.595	0.785	0.795	0.985	0.995	1.185	1.195
E1	0.450	0.456	0.548	0.552	0.750	0.756	0.950	0.956	1.150	1.156
E2	0.390	0.430	0.490	0.530	0.690	0.730	0.890	0.930	1.090	1.130
E3	0.300 REF		0.400 REF		0.600 REF		0.800 REF		1.000 REF	
e	0.044	0.056	0.044	0.056	0.044	0.056	0.044	0.056	0.044	0.056
h	0.042	0.048	0.042	0.048	0.042	0.048	0.044	0.056	0.044	0.056
ND	7		7		13		17		21	
NE	7		9		13		17		21	

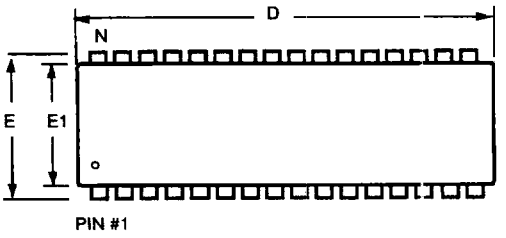
300-MIL PDIP - Package Code P
Plastic Dual In-line Package

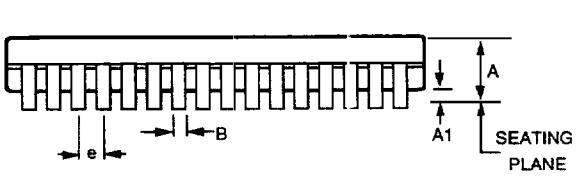
Notes:
1. Refer to applicable symbol list.
2. All dimensions are in inches.
3. N is the number of lead positions.
4. Dimensions D and E1 are to be measured at maximum material condition but do not include mold flash. Allowable mold flash is 0.010 in. per side.

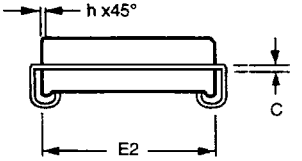


JEDEC#	MS-001AC		MS001AA		MS-001AE		N/A		MS-001AF		MO-095AH	
DWG#	PD14A		PD16A		PD20A		PT22B		PT24A		PT28A	
Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
A	0.130	0.170	0.130	0.170	0.130	0.170	0.130	0.170	0.130	0.170	0.130	0.180
A1	0.015	0.040	0.015	0.040	0.015	0.040	0.015	0.040	0.015	0.040	0.015	0.040
B	0.016	0.020	0.016	0.020	0.016	0.020	0.016	0.020	0.016	0.020	0.016	0.020
B1	0.045	0.070	0.045	0.070	0.045	0.070	0.045	0.070	0.045	0.070	0.045	0.060
C	0.009	0.012	0.009	0.012	0.009	0.012	0.009	0.012	0.009	0.012	0.009	0.012
D	0.745	0.765	0.745	0.765	1.020	1.040	1.020	1.040	1.150	1.260	1.345	1.385
E	0.300	0.325	0.300	0.325	0.300	0.325	0.300	0.325	0.300	0.325	0.300	0.325
E1	0.240	0.270	0.240	0.270	0.240	0.270	0.240	0.270	0.250	0.280	0.275	0.295
e	0.090	0.110	0.090	0.110	0.090	0.110	0.090	0.110	0.090	0.110	0.090	0.110
e_A	0.310	0.380	0.310	0.380	0.310	0.380	0.310	0.380	0.310	0.380	0.310	0.380
L	0.120	0.140	0.120	0.140	0.120	0.140	0.120	0.140	0.120	0.140	0.120	0.140
S	0.070	0.080	0.020	0.035	0.060	0.070	0.010	0.020	0.025	0.080	0.020	0.040
N	14		16		20		22		24		28	

300-MIL SOJ - Package Code V







JEDEC#	MO-088AD		MO-088AE		MO-088AF	
DWG#	PJ20A		PJ24A		PJ28A	
Symbol	Min	Max	Min	Max	Min	Max
A	0.120	0.140	0.120	0.140	0.120	0.140
A1	0.025	0.045	0.025	0.045	0.025	0.045
B	0.014	0.019	0.014	0.019	0.014	0.019
C	0.009	0.012	0.009	0.012	0.009	0.012
D	0.502	0.512	0.602	0.612	0.701	0.711
E	0.336	0.347	0.336	0.347	0.336	0.347
E1	0.292	0.299	0.292	0.299	0.292	0.299
E2	0.262	0.272	0.262	0.272	0.262	0.272
e	0.044	0.056	0.044	0.056	0.044	0.056
h	0.010	0.016	0.010	0.016	0.010	0.016
N	20		24		28	

Notes:
1. Refer to applicable symbol list.
2. All dimensions are in inches.
3. N is the maximum number of lead positions.
4. Dimensions D1 and E1 are to be measured at maximum material condition but do not include mold flash. Allowable mold flash is 0.006 in. per side.
5. Lead coplanarity is 0.004 in. maximum.

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