## Document Title

**256Kx36 & 256Kx32 & 512Kx18-Bit Pipelined N*t*RAM™**

## Revision History

| Rev. No. | History | Draft Date | Remark |
|---|---|---|---|
| 0.0 | 1. Initial document. | May. 18. 2001 | Preliminary |
| 0.1 | 1. Add x32 org part and industrial temperature part | Aug. 11. 2001 | Preliminary |
| 0.2 | 1. change scan order(1) form 4T to 6T at 119BGA(x18) | Aug. 28. 2001 | Preliminary |
| 1.0 | 1. Final spec release<br>2. Change $I_{SB1}$ form 80mA to 100mA<br>3. Change $I_{SB2}$ form 40mA to 60mA | Nov. 16. 2001 | Final |

## 8Mb NtRAM(Flow Through / Pipelined) Ordering Information

| Org. | Part Number | Mode | VDD | Speed<br>FT ; Access Time(ns)<br>Pipelined ; Cycle Time(MHz) | PKG | Temp |
|---|---|---|---|---|---|---|
| 512Kx18 | K7M801825B-Q(H)C(I)65/75/85 | FlowThrough | 3.3 | 6.5/7.5/8.5 ns | Q:<br>100TQFP<br><br>H:<br>119BGA | C:<br>Commercial<br>Temperature<br>Range<br>I:<br>Industrial<br>Temperature<br>Range |
| | K7N801801B-Q(H)C(I)16/13 | Pipelined | 3.3 | 167/133 MHz | | |
| | K7N801809B-Q(H)C(I)25/22/20 | Pipelined | 3.3 | 250/225/200 MHz | | |
| | K7N801845B-Q(H)C(I)16/13 | Pipelined | 2.5 | 167/133 MHz | | |
| | K7N801849B-Q(H)C(I)25/22/20 | Pipelined | 2.5 | 250/225/200 MHz | | |
| 256Kx32 | K7M803225B-QC(I)65/75/85 | FlowThrough | 3.3 | 6.5/7.5/8.5 ns | | |
| | K7N803201B-QC(I)16/13 | Pipelined | 3.3 | 167/133 MHz | | |
| | K7N803209B-QC(I)25/22/20 | Pipelined | 3.3 | 250/225/200 MHz | | |
| | K7N803245B-QC(I)C16/13 | Pipelined | 2.5 | 167/133 MHz | | |
| | K7N803249B-QC(I)25/22/20 | Pipelined | 2.5 | 250/225/200 MHz | | |
| 256Kx36 | K7M803625B-Q(H)C(I)65/75/85 | FlowThrough | 3.3 | 6.5/7.5/8.5 ns | | |
| | K7N803601B-Q(H)C(I)16/13 | Pipelined | 3.3 | 167/133 MHz | | |
| | K7N803609B-Q(H)C(I)25/22/20 | Pipelined | 3.3 | 250/225/200 MHz | | |
| | K7N803645B-Q(H)C(I)16/13 | Pipelined | 2.5 | 167/133 MHz | | |
| | K7N803649B-Q(H)C(I)25/22/20 | Pipelined | 2.5 | 250/225/200 MHz | | |

# 256Kx36 & 512Kx18-Bit Pipelined N*t*RAM™

## FEATURES

- 2.5V ±5% Power Supply.
- Byte Writable Function.
- Enable clock and suspend operation.
- Single READ/WRITE control pin.
- Self-Timed Write Cycle.
- Three Chip Enable for simple depth expansion with no data contention .
- A interleaved burst or a linear burst mode.
- Asynchronous output enable control.
- Power Down mode.
- TTL-Level Three-State Outputs.
- 100-TQFP-1420A / 119BGA(7x17 Ball Grid Array Package).
- Operating in commeical and industrial temperature range.

## FAST ACCESS TIMES

| PARAMETER | Symbol | -25 | -22 | -20 | Unit |
|---|---|---|---|---|---|
| Cycle Time | tCYC | 4.0 | 4.4 | 5.0 | ns |
| Clock Access Time | tCD | 2.6 | 2.8 | 3.2 | ns |
| Output Enable Access Time | tOE | 2.6 | 2.8 | 3.2 | ns |

## GENERAL DESCRIPTION

The K7N803649B, K7N803249B and K7N801849B are 9,437,184 bits Synchronous Static SRAMs.

The N*t*RAM™, or No Turnaround Random Access Memory utilizes all the bandwidth in any combination of operating cycles. Address, data inputs, and all control signals except output enable and linear burst order are synchronized to input clock. Burst order control must be tied "High or Low".

Asynchronous inputs include the sleep mode enable(ZZ). Output Enable controls the outputs at any given time.

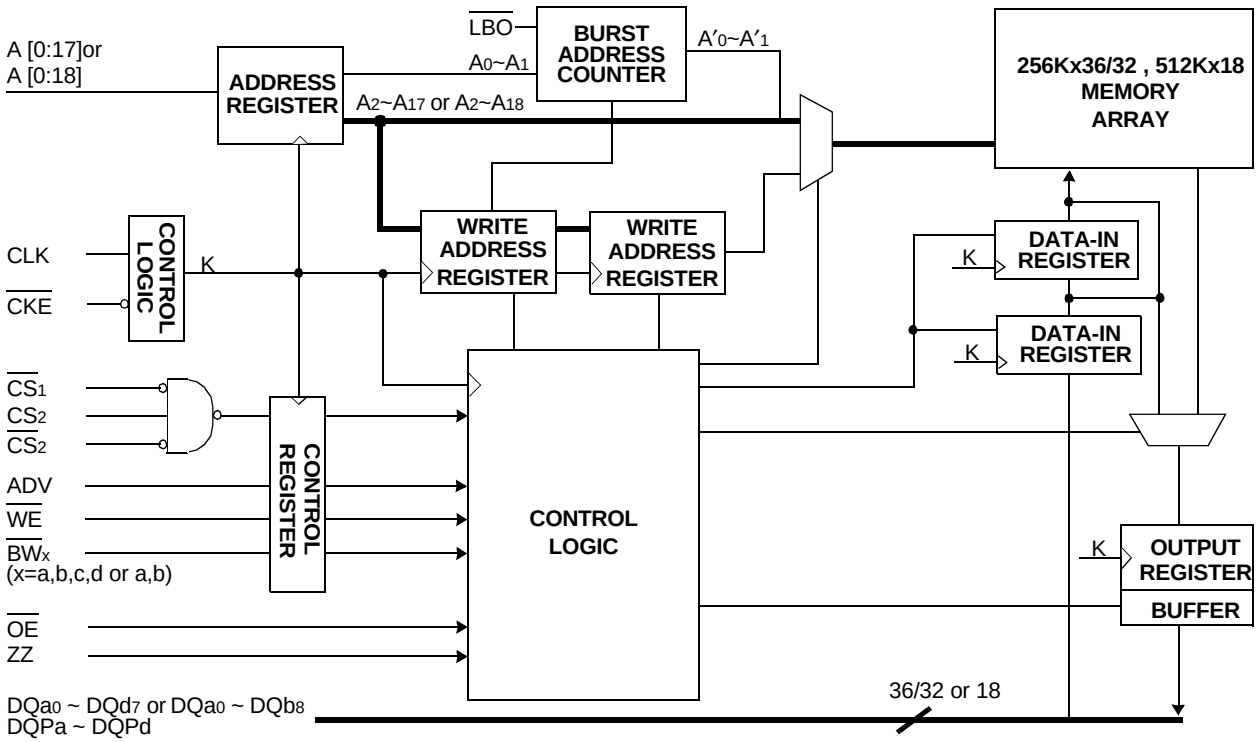
Write cycles are internally self-timed and initiated by the rising edge of the clock input. This feature eliminates complex off-chip write pulse generation and provides increased timing flexibility for incoming signals.

For read cycles, pipelined SRAM output data is temporarily stored by an edge triggered output register and then released to the output buffers at the next rising edge of clock.

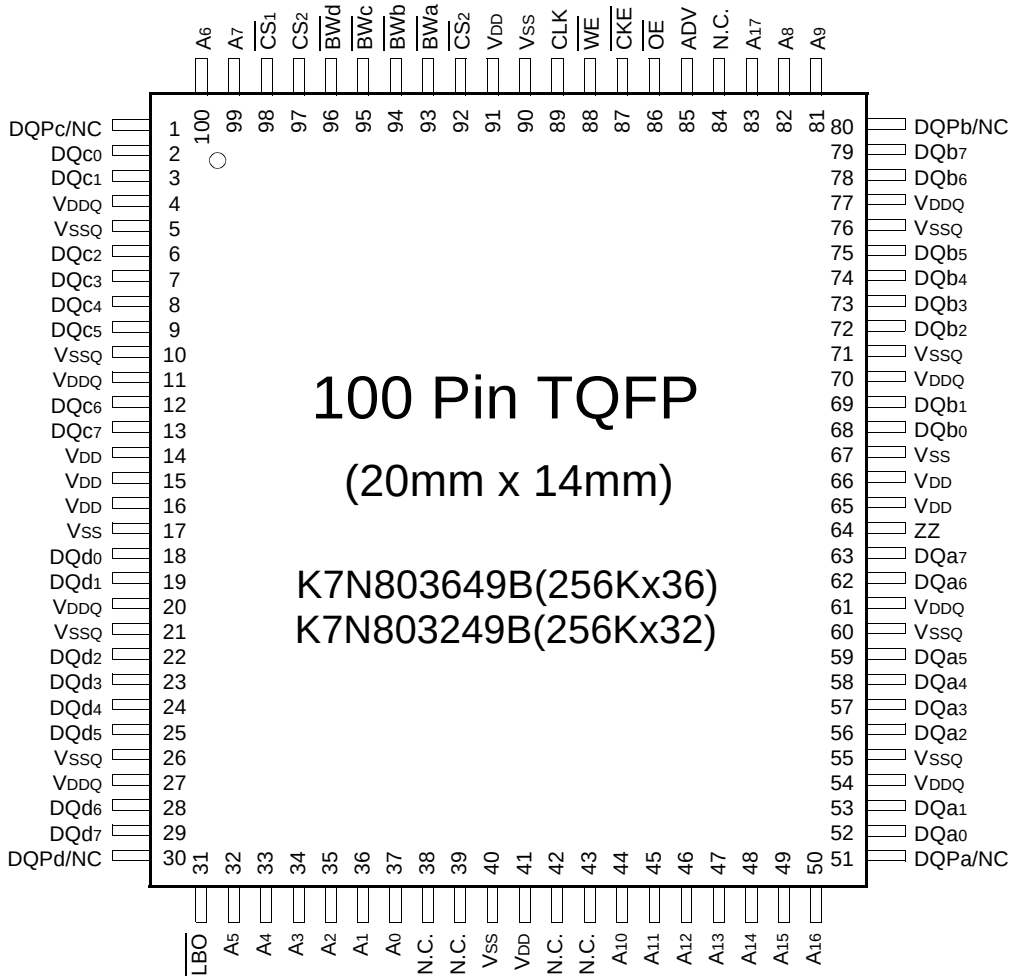
The K7N803649B, K7N803249B and K7N801849B are implemented with SAMSUNG′s high performance CMOS technology and is available in 100pin TQFP and 119BGA packages (100pin TQFP only for K7M803249B).

Multiple power and ground pins minimize ground bounce.

## LOGIC BLOCK DIAGRAM



## PIN CONFIGURATION(TOP VIEW)

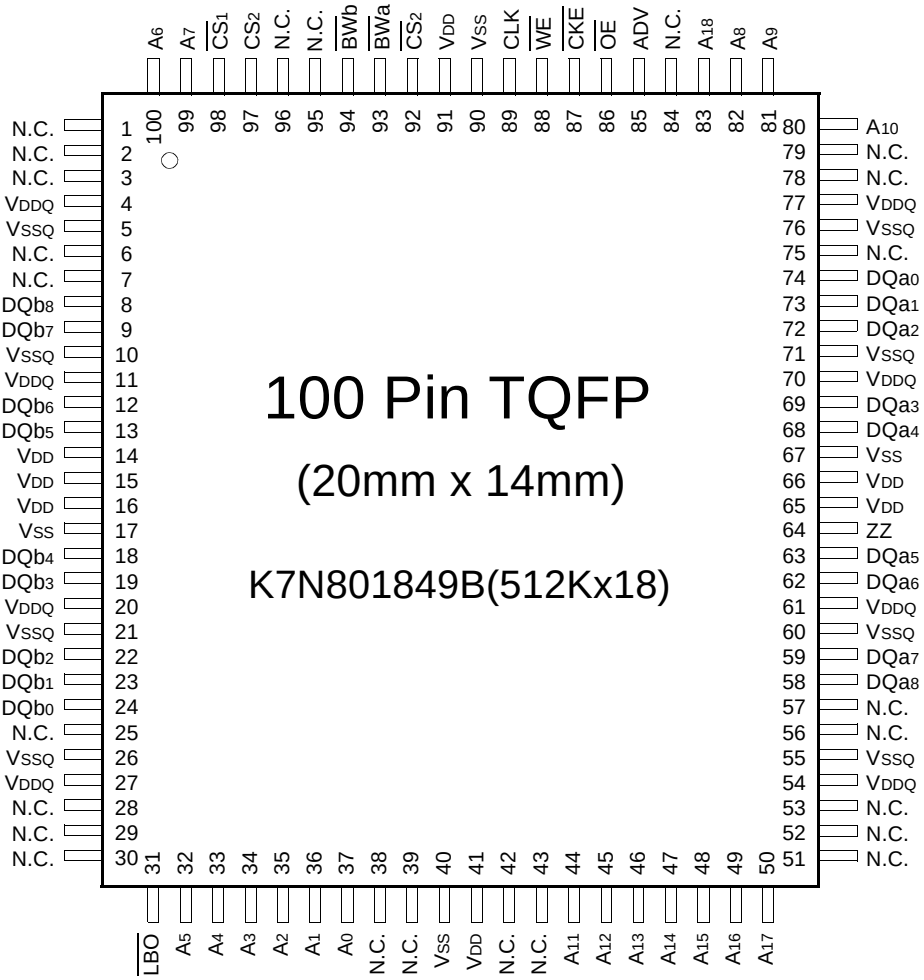



## PIN NAME

| SYMBOL | PIN NAME | TQFP PIN NO. | SYMBOL | PIN NAME | TQFP PIN NO. |
|---|---|---|---|---|---|
| $A_0$ - $A_{17}$ | Address Inputs | 32,33,34,35,36,37, 44,45,46,47,48,49, 50,81,82,83,99,100 | $V_{DD}$ | Power Supply(+2.5V) | 14,15,16,41,65,66,91 |
| | | | $V_{SS}$ | Ground | 17,40,67,90 |
| | | | N.C. | No Connect | 38,39,42,43,84 |
| $\overline{ADV}$ | Address Advance/Load | 85 | | | |
| $\overline{WE}$ | Read/Write Control Input | 88 | $DQa_0$~$a_7$ | Data Inputs/Outputs | 52,53,56,57,58,59,62,63 |
| $\overline{CLK}$ | Clock | 89 | $DQb_0$~$b_7$ | | 68,69,72,73,74,75,78,79 |
| $\overline{CKE}$ | Clock Enable | 87 | $DQc_0$~$c_7$ | | 2,3,6,7,8,9,12,13 |
| $\overline{CS_1}$ | Chip Select | 98 | $DQd_0$~$d_7$ | | 18,19,22,23,24,25,28,29 |
| $\overline{CS_2}$ | Chip Select | 97 | DQPa~Pd | | 51,80,1,30 |
| $\overline{CS_2}$ | Chip Select | 92 | /NC | | |
| $\overline{BWx}$ | Byte Write Inputs | 93,94,95,96 | | Output Power Supply | 4,11,20,27,54,61,70,77 |
| $\overline{OE}$ | Output Enable | 86 | $V_{DDQ}$ | (+2.5V) | |
| $\overline{ZZ}$ | Power Sleep Mode | 64 | | Output Ground | 5,10,21,26,55,60,71,76 |
| LBO | Burst Mode Control | 31 | $V_{SSQ}$ | | |

**Notes :** 1. The pin 84 is reserved for address bit for the 16Mb NtRAM.
2. $A_0$ and $A_1$ are the two least significant bits(LSB) of the address field and set the internal burst counter if burst is desired.
3. DQPa~DQPd are NC for K7M803249B

## PIN CONFIGURATION(TOP VIEW)




## PIN NAME

| SYMBOL | PIN NAME | TQFP PIN NO. | SYMBOL | PIN NAME | TQFP PIN NO. |
|---|---|---|---|---|---|
| A0 - A18 | Address Inputs | 32,33,34,35,36,37, 44,45,46,47,48,49,50, 80,81,82,83,99,100 | VDD | Power Supply(+2.5V) | 14,15,16,41,65,66,91 |
| | | | VSS | Ground | 17,40,67,90 |
| | | | N.C. | No Connect | 1,2,3,6,7,25,28,29,30, 38,39,42,43,51,52,53, 56,57,75,78,79,84,95,96 |
| ADV | Address Advance/Load | 85 | | | |
| WE | Read/Write Control Input | 88 | | | |
| CLK | Clock | 89 | | | |
| CKE | Clock Enable | 87 | DQa0~a8 | Data Inputs/Outputs | 58,59,62,63,68,69,72,73,74 |
| CS1 | Chip Select | 98 | DQb0~b8 | | 8,9,12,13,18,19,22,23,24 |
| CS2 | Chip Select | 97 | | | |
| CS2 | Chip Select | 92 | | | |
| BWx | Byte Write Inputs | 93,94 | VDDQ | Output Power Supply (+2.5V) | 4,11,20,27,54,61,70,77 |
| OE | Output Enable | 86 | | | |
| ZZ | Power Sleep Mode | 64 | VSSQ | Output Ground | 5,10,21,26,55,60,71,76 |
| LBO | Burst Mode Control | 31 | | | |

**Notes :** 1. The pin 84 is reserved for address bit for the 16Mb NtRAM.
2. A0 and A1 are the two least significant bits(LSB) of the address field and set the internal burst counter if burst is desired.

## 119BGA PACKAGE PIN CONFIGURATIONS(TOP VIEW)

**K7N803649B(256Kx36)**

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
|---|---|---|---|---|---|---|---|
| **A** | $V_{DDQ}$ | A | A | NC** | A | A | $V_{DDQ}$ |
| **B** | NC | $CS_2$ | A | ADV | A | $\overline{CS_2}$ | NC |
| **C** | NC | A | A | $V_{DD}$ | A | A | NC |
| **D** | DQc | DQPc | $V_{SS}$ | NC | $V_{SS}$ | DQPb | DQb |
| **E** | DQc | DQc | $V_{SS}$ | $\overline{CS_1}$ | $V_{SS}$ | DQb | DQb |
| **F** | $V_{DDQ}$ | DQc | $V_{SS}$ | $\overline{OE}$ | $V_{SS}$ | DQb | $V_{DDQ}$ |
| **G** | DQc | DQc | $\overline{BW}$c | A | $\overline{BW}$b | DQb | DQb |
| **H** | DQc | DQc | $V_{SS}$ | $\overline{WE}$ | $V_{SS}$ | DQb | DQb |
| **J** | $V_{DDQ}$ | $V_{DD}$ | NC | $V_{DD}$ | NC | $V_{DD}$ | $V_{DDQ}$ |
| **K** | DQd | DQd | $V_{SS}$ | CLK | $V_{SS}$ | DQa | DQa |
| **L** | DQd | DQd | $\overline{BW}$d | NC | $\overline{BW}$a | DQa | DQa |
| **M** | $V_{DDQ}$ | DQd | $V_{SS}$ | $\overline{CKE}$ | $V_{SS}$ | DQa | $V_{DDQ}$ |
| **N** | DQd | DQd | $V_{SS}$ | $A_1$* | $V_{SS}$ | DQa | DQa |
| **P** | DQd | DQPd | $V_{SS}$ | $A_0$* | $V_{SS}$ | DQPa | DQa |
| **R** | NC | A | $\overline{LBO}$ | $V_{DD}$ | NC | A | NC |
| **T** | NC | NC | A | A | A | NC | ZZ |
| **U** | $V_{DDQ}$ | TMS | TDI | TCK | TDO | NC | $V_{DDQ}$ |

**Note :** * $A_0$ and $A_1$ are the two least significant bits(LSB) of the address field and set the internal burst counter if burst is desired.

** Pin 4A is reserved for address expansion to 16Mb.

## PIN NAME

| SYMBOL | PIN NAME | SYMBOL | PIN NAME |
|---|---|---|---|
| A | Address Inputs | $V_{DD}$ | Power Supply |
| | | $V_{SS}$ | Ground |
| $A_0$,$A_1$ | Burst Address Inputs | | |
| $\overline{ADV}$ | Address Advance/Load | N.C. | No Connect |
| $\overline{WE}$ | Read/Write Control Input | | |
| $\overline{CLK}$ | Clock | DQa | Data Inputs/Outputs |
| $\overline{CKE}$ | Clock Enable | DQb | Data Inputs/Outputs |
| $\overline{CS_1}$ | Chip Select | DQc | Data Inputs/Outputs |
| $\overline{CS_2}$ | Chip Select | DQd | Data Inputs/Outputs |
| $\overline{CS_2}$ | Chip Select | DQPa~Pd | Data Inputs/Outputs |
| $\overline{BW}$x | Byte Write Inputs | | |
| (x=a,b,c,d) | | $V_{DDQ}$ | Output Power Supply |
| $\overline{OE}$ | Output Enable | | |
| $\overline{ZZ}$ | Power Sleep Mode | | |
| $\overline{LBO}$ | Burst Mode Control | | |
| TCK | JTAG Test Clock | | |
| TMS | JTAG Test Mode Select | | |
| TDI | JTAG Test Data Input | | |
| TDO | JTAG Test Data Output | | |

## 119BGA PACKAGE PIN CONFIGURATIONS(TOP VIEW)

**K7N801849B(512Kx18)**

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
|---|---|---|---|---|---|---|---|
| **A** | $V_{DDQ}$ | A | A | NC** | A | A | $V_{DDQ}$ |
| **B** | NC | $CS_2$ | A | ADV | A | $\overline{CS_2}$ | NC |
| **C** | NC | A | A | $V_{DD}$ | A | A | NC |
| **D** | DQb | NC | $V_{SS}$ | NC | $V_{SS}$ | DQPa | NC |
| **E** | NC | DQb | $V_{SS}$ | $\overline{CS_1}$ | $V_{SS}$ | NC | DQa |
| **F** | $V_{DDQ}$ | NC | $V_{SS}$ | $\overline{OE}$ | $V_{SS}$ | DQa | $V_{DDQ}$ |
| **G** | NC | DQb | $\overline{BW}$b | A | $V_{SS}$ | NC | DQa |
| **H** | DQb | NC | $V_{SS}$ | $\overline{WE}$ | $V_{SS}$ | DQa | NC |
| **J** | $V_{DDQ}$ | $V_{DD}$ | NC | $V_{DD}$ | NC | $V_{DD}$ | $V_{DDQ}$ |
| **K** | NC | DQb | $V_{SS}$ | CLK | $V_{SS}$ | NC | DQa |
| **L** | DQb | NC | $V_{SS}$ | NC | $\overline{BW}$a | DQa | NC |
| **M** | $V_{DDQ}$ | DQb | $V_{SS}$ | $\overline{CKE}$ | $V_{SS}$ | NC | $V_{DDQ}$ |
| **N** | DQb | NC | $V_{SS}$ | $A_1$* | $V_{SS}$ | DQa | NC |
| **P** | NC | DQPb | $V_{SS}$ | $A_0$* | $V_{SS}$ | NC | DQa |
| **R** | NC | A | $\overline{LBO}$ | $V_{DD}$ | NC | A | NC |
| **T** | NC | A | A | NC | A | A | ZZ |
| **U** | $V_{DDQ}$ | TMS | TDI | TCK | TDO | NC | $V_{DDQ}$ |

**Note :** * $A_0$ and $A_1$ are the two least significant bits(LSB) of the address field and set the internal burst counter if burst is desired.

** Pin 4A is reserved for address expansion to 16Mb.

## PIN NAME

| SYMBOL | PIN NAME | SYMBOL | PIN NAME |
|---|---|---|---|
| A | Address Inputs | $V_{DD}$ | Power Supply |
| | | $V_{SS}$ | Ground |
| $A_0$,$A_1$ | Burst Address Inputs | | |
| $\overline{ADV}$ | Address Advance/Load | N.C. | No Connect |
| $\overline{WE}$ | Read/Write Control Input | | |
| $\overline{CLK}$ | Clock | | |
| $\overline{CKE}$ | Clock Enable | DQa | Data Inputs/Outputs |
| $\overline{CS_1}$ | Chip Select | DQb | Data Inputs/Outputs |
| $CS_2$ | Chip Select | DQPa, Pb | Data Inputs/Outputs |
| $\overline{CS_2}$ | Chip Select | | |
| $\overline{BW}$x (x=a,b) | Byte Write Inputs | $V_{DDQ}$ | Output Power Supply |
| $\overline{OE}$ | Output Enable | | |
| $\overline{ZZ}$ | Power Sleep Mode | | |
| $\overline{LBO}$ | Burst Mode Control | | |
| TCK | JTAG Test Clock | | |
| TMS | JTAG Test Mode Select | | |
| TDI | JTAG Test Data Input | | |
| TDO | JTAG Test Data Output | | |

## FUNCTION DESCRIPTION

The K7N803649B, K7N803249B and K7N801849B are N*t*RAM™ designed to sustain 100% bus bandwidth by eliminating turnaround cycle when there is transition from Read to Write, or vice versa.
All inputs (with the exception of $\overline{OE}$, $\overline{LBO}$ and ZZ) are synchronized to rising clock edges.

All read, write and deselect cycles are initiated by the ADV input. Subsequent burst addresses can be internally generated by the burst advance pin (ADV). ADV should be driven to Low once the device has been deselected in order to load a new address for next operation.

Clock Enable($\overline{CKE}$) pin allows the operation of the chip to be suspended as long as necessary. When $\overline{CKE}$ is high, all synchronous inputs are ignored and the internal device registers will hold their previous values.

N*t*RAM™ latches external address and initiates a cycle, when $\overline{CKE}$, ADV are driven to low and all three chip enables($\overline{CS_1}$, $CS_2$, $\overline{CS_2}$) are active .
Output Enable($\overline{OE}$) can be used to disable the output at any given time.

Read operation is initiated when at the rising edge of the clock, the address presented to the address inputs are latched in the address register, $\overline{CKE}$ is driven low, all three chip enables($\overline{CS_1}$, $CS_2$, $\overline{CS_2}$) are active, the write enable input signals $\overline{WE}$ are driven high, and ADV driven low.The internal array is read between the first rising edge and the second rising edge of the clock and the data is latched in the output register. At the second clock edge the data is driven out of the SRAM. Also during read operation $\overline{OE}$ must be driven low for the device to drive out the requested data.

Write operation occurs when $\overline{WE}$ is driven low at the rising edge of the clock. $\overline{BW}$[d:a] can be used for byte write operation. The pipe-lined N*t*RAM™ uses a late-late write cycle to utilize 100% of the bandwidth.
At the first rising edge of the clock, $\overline{WE}$ and address are registered, and the data associated with that address is required two cycle later.

Subsequent addresses are generated by ADV High for the burst access as shown below. The starting point of the burst seguence is provided by the external address. The burst address counter wraps around to its initial state upon completion.
The burst sequence is determined by the state of the $\overline{LBO}$ pin. When this pin is low, linear burst sequence is selected.
And when this pin is high, Interleaved burst sequence is selected.

During normal operation, ZZ must be driven low. When ZZ is driven high, the SRAM will enter a Power Sleep Mode after 2 cycles. At this time, internal state of the SRAM is preserved. When ZZ returns to low, the SRAM normally operates after 2 cycles of wake up time.

## BURST SEQUENCE TABLE

**(Interleaved Burst, $\overline{LBO}$=High)**

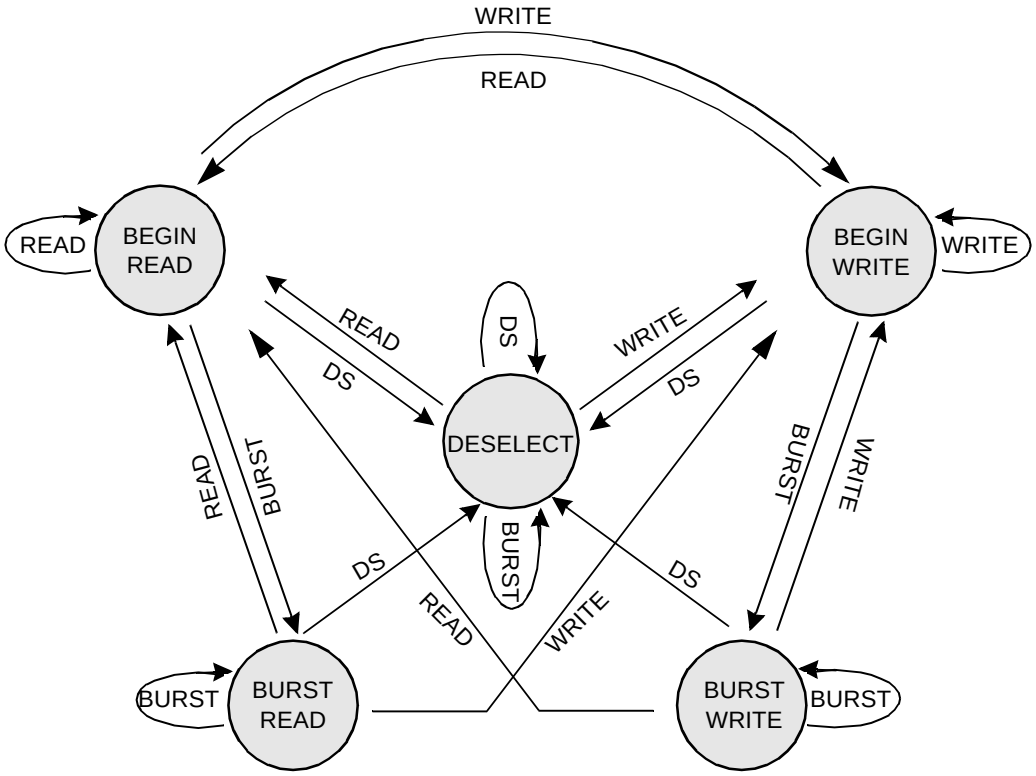
| $\overline{LBO}$ PIN | HIGH | Case 1 | | Case 2 | | Case 3 | | Case 4 | |
|---|---|---|---|---|---|---|---|---|---|
| | | $A_1$ | $A_0$ | $A_1$ | $A_0$ | $A_1$ | $A_0$ | $A_1$ | $A_0$ |
| First Address | | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 |
| ↓ | | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 0 |
| | | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 |
| Fourth Address | | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 0 |

**(Linear Burst, $\overline{LBO}$=Low)**

| $\overline{LBO}$ PIN | LOW | Case 1 | | Case 2 | | Case 3 | | Case 4 | |
|---|---|---|---|---|---|---|---|---|---|
| | | $A_1$ | $A_0$ | $A_1$ | $A_0$ | $A_1$ | $A_0$ | $A_1$ | $A_0$ |
| First Address | | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 |
| ↓ | | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 |
| | | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 |
| Fourth Address | | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 |

**Note :** 1. $\overline{LBO}$ pin must be tied to High or Low, and Floating State must not be allowed.

## STATE DIAGRAM FOR N*t*RAM™




| COMMAND | ACTION |
|---|---|
| DS | DESELECT |
| READ | BEGIN READ |
| WRITE | BEGIN WRITE |
| BURST | BEGIN READ<br>BEGIN WRITE<br>CONTINUE DESELECT |

**Notes :** 1. An IGNORE CLOCK EDGE cycle is not shown is the above diagram. This is because CKE HIGH only blocks the clock(CLK) input and does not change the state of the device.
2. States change on the rising edge of the clock(CLK)

## TRUTH TABLES

### SYNCHRONOUS TRUTH TABLE

| $\overline{CS_1}$ | $CS_2$ | $\overline{CS_2}$ | ADV | $\overline{WE}$ | $\overline{BWx}$ | $\overline{OE}$ | $\overline{CKE}$ | CLK | ADDRESS ACCESSED | OPERATION |
|---|---|---|---|---|---|---|---|---|---|---|
| H | X | X | L | X | X | X | L | ↑ | N/A | Not Selected |
| X | L | X | L | X | X | X | L | ↑ | N/A | Not Selected |
| X | X | H | L | X | X | X | L | ↑ | N/A | Not Selected |
| X | X | X | H | X | X | X | L | ↑ | N/A | Not Selected Continue |
| L | H | L | L | H | X | L | L | ↑ | External Address | Begin Burst Read Cycle |
| X | X | X | H | X | X | L | L | ↑ | Next Address | Continue Burst Read Cycle |
| L | H | L | L | H | X | H | L | ↑ | External Address | NOP/Dummy Read |
| X | X | X | H | X | X | H | L | ↑ | Next Address | Dummy Read |
| L | H | L | L | L | L | X | L | ↑ | External Address | Begin Burst Write Cycle |
| X | X | X | H | X | L | X | L | ↑ | Next Address | Continue Burst Write Cycle |
| L | H | L | L | L | H | X | L | ↑ | N/A | NOP/Write Abort |
| X | X | X | H | X | H | X | L | ↑ | Next Address | Write Abort |
| X | X | X | X | X | X | X | H | ↑ | Current Address | Ignore Clock |

**Notes :** 1. X means "Don't Care". 2. The rising edge of clock is symbolized by (↑).

3. A continue deselect cycle can only be enterd if a deselect cycle is executed first.

4. $\overline{WRITE}$ = L means Write operation in WRITE TRUTH TABLE.
   $\overline{WRITE}$ = H means Read operation in WRITE TRUTH TABLE.

5. Operation finally depends on status of asynchronous input pins(ZZ and $\overline{OE}$).

### WRITE TRUTH TABLE(x36/32)

| $\overline{WE}$ | $\overline{BWa}$ | $\overline{BWb}$ | $\overline{BWc}$ | $\overline{BWd}$ | OPERATION |
|---|---|---|---|---|---|
| H | X | X | X | X | READ |
| L | L | H | H | H | WRITE BYTE a |
| L | H | L | H | H | WRITE BYTE b |
| L | H | H | L | H | WRITE BYTE c |
| L | H | H | H | L | WRITE BYTE d |
| L | L | L | L | L | WRITE ALL BYTEs |
| L | H | H | H | H | WRITE ABORT/NOP |

**Notes :** 1. X means "Don't Care".

2. All inputs in this table must meet setup and hold time around the rising edge of CLK(↑).

### WRITE TRUTH TABLE(x18)

| $\overline{WE}$ | $\overline{BWa}$ | $\overline{BWb}$ | OPERATION |
|---|---|---|---|
| H | X | X | READ |
| L | L | H | WRITE BYTE a |
| L | H | L | WRITE BYTE b |
| L | L | L | WRITE ALL BYTEs |
| L | H | H | WRITE ABORT/NOP |

**Notes :** 1. X means "Don't Care".

2. All inputs in this table must meet setup and hold time around the rising edge of CLK(↑).

## ASYNCHRONOUS TRUTH TABLE

| Operation | ZZ | $\overline{OE}$ | I/O STATUS |
|---|---|---|---|
| Sleep Mode | H | X | High-Z |
| Read | L | L | DQ |
| | L | H | High-Z |
| Write | L | X | Din, High-Z |
| Deselected | L | X | High-Z |

**Notes**

1. X means "Don't Care".
2. Sleep Mode means power Sleep Mode of which stand-by current does not depend on cycle time.
3. Deselected means power Sleep Mode of which stand-by current depends on cycle time.

## ABSOLUTE MAXIMUM RATINGS*

| PARAMETER | | SYMBOL | RATING | UNIT |
|---|---|---|---|---|
| Voltage on $V_{DD}$ Supply Relative to $V_{SS}$ | | $V_{DD}$ | -0.3 to 4.6 | V |
| Voltage on Any Other Pin Relative to $V_{SS}$ | | $V_{IN}$ | -0.3 to $V_{DD}$+0.3 | V |
| Power Dissipation | | $P_D$ | 1.4 | W |
| Storage Temperature | | $T_{STG}$ | -65 to 150 | °C |
| Operating Temperature | Commercial | $T_{OPR}$ | 0 to 70 | °C |
| | Industrial | $T_{OPR}$ | -40 to 85 | °C |
| Storage Temperature Range Under Bias | | $T_{BIAS}$ | -10 to 85 | °C |

***Notes :** Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## OPERATING CONDITIONS($0°C \le T_A \le 70°C$)

| PARAMETER | SYMBOL | MIN | Typ. | MAX | UNIT |
|---|---|---|---|---|---|
| Supply Voltage | $V_{DD}$ | 2.375 | 2.5 | 2.625 | V |
| | $V_{DDQ}$ | 2.375 | 2.5 | 2.625 | V |
| Ground | $V_{SS}$ | 0 | 0 | 0 | V |

***Note :** $V_{DD}$ and $V_{DDQ}$ must be supplied with identical vlotage levels.

The above parameters are also guaranteed at industrial temperature range.

## CAPACITANCE*($T_A$=25°C, f=1MHz)

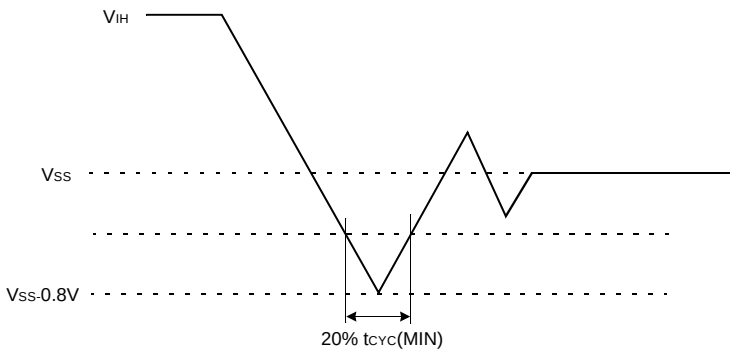
| PARAMETER | SYMBOL | TEST CONDI- | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| Input Capacitance | $C_{IN}$ | $V_{IN}$=0V | - | 5 | pF |
| Output Capacitance | $C_{OUT}$ | $V_{OUT}$=0V | - | 7 | pF |

***Note :** Sampled not 100% tested.

## DC ELECTRICAL CHARACTERISTICS($V_{DD}$=2.5V ±5%, $T_A$=0°C to +70°C)

| PARAMETER | SYMBOL | TEST CONDITIONS | | MIN | MAX | UNIT | NOTES |
|---|---|---|---|---|---|---|---|
| Input Leakage Current(except ZZ) | $I_{IL}$ | $V_{DD}$=Max ; $V_{IN}$=$V_{SS}$ to $V_{DD}$ | | -2 | +2 | µA | |
| Output Leakage Current | $I_{OL}$ | Output Disabled, | | -2 | +2 | µA | |
| Operating Current | $I_{CC}$ | $V_{DD}$=Max $I_{OUT}$=0mA<br>Cycle Time ≥ $t_{CYC}$ Min | -25 | - | 440 | mA | 1,2 |
| | | | -22 | - | 410 | | |
| | | | -20 | - | 380 | | |
| Standby Current | $I_{SB}$ | Device deselected, $I_{OUT}$=0mA,<br>ZZ≤$V_{IL}$, f=Max,<br>All Inputs≤0.2V or ≥ $V_{DD}$-0.2V | -25 | - | 160 | mA | |
| | | | -22 | - | 150 | | |
| | | | -20 | - | 140 | | |
| | $I_{SB1}$ | Device deselected, $I_{OUT}$=0mA, ZZ≤0.2V, f=0,<br>All Inputs=fixed ($V_{DD}$-0.2V or 0.2V) | | - | 100 | mA | |
| | $I_{SB2}$ | Device deselected, $I_{OUT}$=0mA, ZZ≥$V_{DD}$-0.2V,<br>f=Max, All Inputs≤$V_{IL}$ or ≥$V_{IH}$ | | - | 60 | mA | |
| Output Low Voltage | $V_{OL}$ | $I_{OL}$=1.0mA | | - | 0.4 | V | |
| Output High Voltage | $V_{OH}$ | $I_{OH}$=-1.0mA | | 2.0 | - | V | |
| Input Low Voltage | $V_{IL}$ | | | -0.3* | 0.7 | V | |
| Input High Voltage | $V_{IH}$ | | | 1.7 | $V_{DD}$+0.3** | V | 3 |

**Notes :** 1. The above parameters are also guaranteed at industrial temperature range.
2. Reference AC Operating Conditions and Characteristics for input and timing.
3. Data states are all zero.
4. In Case of I/O Pins, the Max. $V_{IH}$=$V_{DDQ}$+0.3V



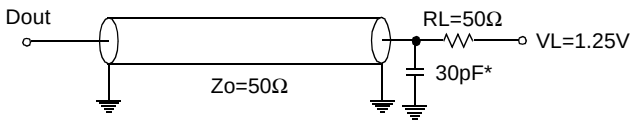

## TEST CONDITIONS

($T_A$=0 to 70°C, $V_{DD}$=2.5V ±5%, unless otherwise specified)

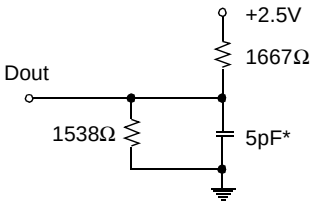
| PARAMETER | VALUE |
|---|---|
| Input Pulse Level | 0 to 2.5V |
| Input Rise and Fall Time(Measured at 20% to 80%) | 1.0V/ns |
| Input and Output Timing Reference Levels | 1.25V |
| Output Load | See Fig. 1 |

* The above parameters are also guaranteed at industrial temperature range.

Output Load(A)




Output Load(B),
(for $t_{LZC}$, $t_{LZOE}$, $t_{HZOE}$ & $t_{HZC}$)




* Including Scope and Jig Capacitance

**Fig. 1**

## AC TIMING CHARACTERISTICS($V_{DD}$=2.5V ±5%, $T_A$=0 to 70°C)

| PARAMETER | SYMBOL | -25 | | -22 | | -20 | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | MIN | MAX | |
| Cycle Time | $t_{CYC}$ | 4.0 | - | 4.4 | - | 5.0 | - | ns |
| Clock Access Time | $t_{CD}$ | - | 2.6 | - | 2.8 | - | 3.2 | ns |
| Output Enable to Data Valid | $t_{OE}$ | - | 2.6 | - | 2.8 | - | 3.2 | ns |
| Clock High to Output Low-Z | $t_{LZC}$ | 0.8 | - | 1.0 | - | 1.0 | - | ns |
| Output Hold from Clock High | $t_{OH}$ | 0.8 | - | 1.0 | - | 1.0 | - | ns |
| Output Enable Low to Output Low-Z | $t_{LZOE}$ | 0 | - | 0 | - | 0 | - | ns |
| Output Enable High to Output High-Z | $t_{HZOE}$ | - | 2.6 | - | 2.8 | - | 3.0 | ns |
| Clock High to Output High-Z | $t_{HZC}$ | - | 2.6 | - | 2.8 | - | 3.0 | ns |
| Clock High Pulse Width | $t_{CH}$ | 1.7 | - | 2.0 | - | 2.0 | - | ns |
| Clock Low Pulse Width | $t_{CL}$ | 1.7 | - | 2.0 | - | 2.0 | - | ns |
| Address Setup to Clock High | $t_{AS}$ | 1.2 | - | 1.4 | - | 1.4 | - | ns |
| $\overline{CKE}$ Setup to Clock High | $t_{CES}$ | 1.2 | - | 1.4 | - | 1.4 | - | ns |
| Data Setup to Clock High | $t_{DS}$ | 1.2 | - | 1.4 | - | 1.4 | - | ns |
| Write Setup to Clock High ($\overline{WE}$, $\overline{BW}$x) | $t_{WS}$ | 1.2 | - | 1.4 | - | 1.4 | - | ns |
| Address Advance Setup to Clock High | $t_{ADVS}$ | 1.2 | - | 1.4 | - | 1.4 | - | ns |
| Chip Select Setup to Clock High | $t_{CSS}$ | 1.2 | - | 1.4 | - | 1.4 | - | ns |
| Address Hold from Clock High | $t_{AH}$ | 0.3 | - | 0.4 | - | 0.4 | - | ns |
| $\overline{CKE}$ Hold from Clock High | $t_{CEH}$ | 0.3 | - | 0.4 | - | 0.4 | - | ns |
| Data Hold from Clock High | $t_{DH}$ | 0.3 | - | 0.4 | - | 0.4 | - | ns |
| Write Hold from Clock High ($\overline{WE}$, $\overline{BWE}$x) | $t_{WH}$ | 0.3 | - | 0.4 | - | 0.4 | - | ns |
| Address Advance Hold from Clock High | $t_{ADVH}$ | 0.3 | - | 0.4 | - | 0.4 | - | ns |
| Chip Select Hold from Clock High | $t_{CSH}$ | 0.3 | - | 0.4 | - | 0.4 | - | ns |
| ZZ High to Power Down | $t_{PDS}$ | 2 | - | 2 | - | 2 | - | cycle |
| ZZ Low to Power Up | $t_{PUS}$ | 2 | - | 2 | - | 2 | - | cycle |

**Notes :** 1. The above parameters are also guaranteed at industrial temperature range.
2. All address inputs must meet the specified setup and hold times for all rising clock(CLK) edges when ADV is sampled low and $\overline{CS}$ is sampled low. All other synchronous inputs must meet the specified setup and hold times whenever this device is chip selected.
3. Chip selects must be valid at each rising edge of CLK(when ADV is Low) to remain enabled.
4. A write cycle is defined by $\overline{WE}$ low having been registered into the device at ADV Low, A Read cycle is defined by $\overline{WE}$ High with ADV Low, Both cases must meet setup and hold times.
5. To avoid bus contention, At a given voltage and temperature $t_{LZC}$ is more than $t_{HZC}$.
The specs as shown do not imply bus contention because $t_{LZC}$ is a Min. parameter that is worst case at totally different test conditions (0°C,2.625V) than $t_{HZC}$, which is a Max. parameter(worst case at 70°C,2.375V)
It is not possible for two SRAMs on the same board to be at such different voltage and temperature.

## SLEEP MODE

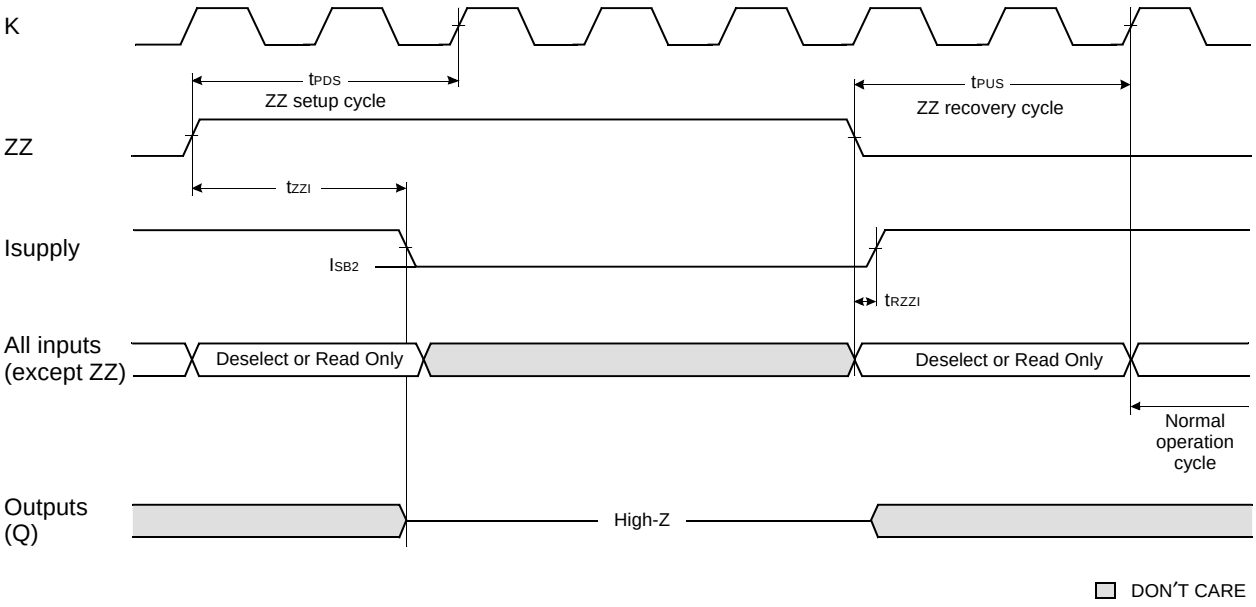
SLEEP MODE is a low current, power-down mode in which the device is deselected and current is reduced to $I_{SB2}$. The duration of SLEEP MODE is dictated by the length of time the ZZ is in a High state.
After entering SLEEP MODE, all inputs except ZZ become disabled and all outputs go to High-Z
The ZZ pin is an asynchronous, active high input that causes the device to enter SLEEP MODE.
When the ZZ pin becomes a logic High, $I_{SB2}$ is guaranteed after the time $t_{ZZI}$ is met. Any operation pending when entering SLEEP MODE is not guaranteed to successful complete. Therefore, SLEEP MODE (READ or WRITE) must not be initiated until valid pending operations are completed. similarly, when exiting SLEEP MODE during $t_{PUS}$, only a DESELECT or READ cycle should be given while the SRAM is transitioning out of SLEEP MODE.

## SLEEP MODE ELECTRICAL CHARACTERISTICS

($V_{DD}$,$V_{DDQ}$=2.5V ±5%)

| DESCRIPTION | CONDITIONS | SYMBOL | MIN | MAX | UNITS |
|---|---|---|---|---|---|
| Current during SLEEP MODE | ZZ ≥ $V_{IH}$ | $I_{SB2}$ | | 10 | mA |
| ZZ active to input ignored | | $t_{PDS}$ | 2 | | cycle |
| ZZ inactive to input sampled | | $t_{PUS}$ | 2 | | cycle |
| ZZ active to SLEEP current | | $t_{ZZI}$ | | 2 | cycle |
| ZZ inactive to exit SLEEP current | | $t_{RZZI}$ | 0 | | |

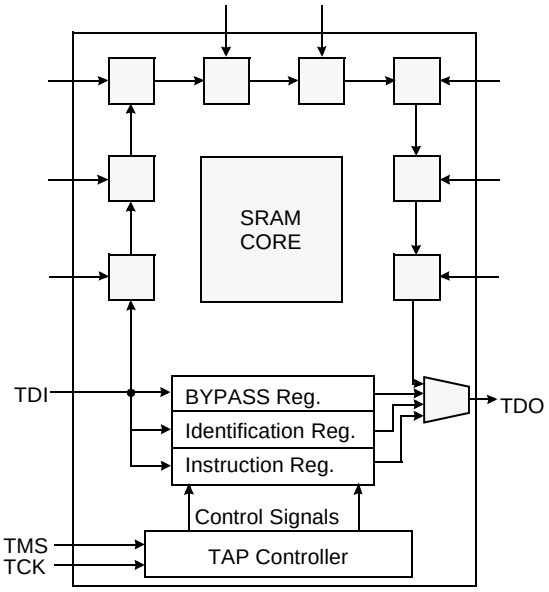
## SLEEP MODE WAVEFORM



## IEEE 1149.1 TEST ACCESS PORT AND BOUNDARY SCAN-JTAG

This part contains an IEEE standard 1149.1 Compatible Test Access Port(TAP). The package pads are monitored by the Serial Scan circuitry when in test mode. This is to support connectivity testing during manufacturing and system diagnostics. Internal data is not driven out of the SRAM under JTAG control. In conformance with IEEE 1149.1, the SRAM contains a TAP controller, Instruction Register, Bypass Register and ID register. The TAP controller has a standard 16-state machine that resets internally upon power-up, therefore, TRST signal is not required. It is possible to use this device without utilizing the TAP. To disable the TAP controller without interfacing with normal operation of the SRAM, TCK must be tied to $V_{SS}$ to preclude mid level input. TMS and TDI are designed so an undriven input will produce a response identical to the application of a logic 1, and may be left unconnected. But they may also be tied to $V_{DD}$ through a resistor. TDO should be left unconnected.

### JTAG Block Diagram



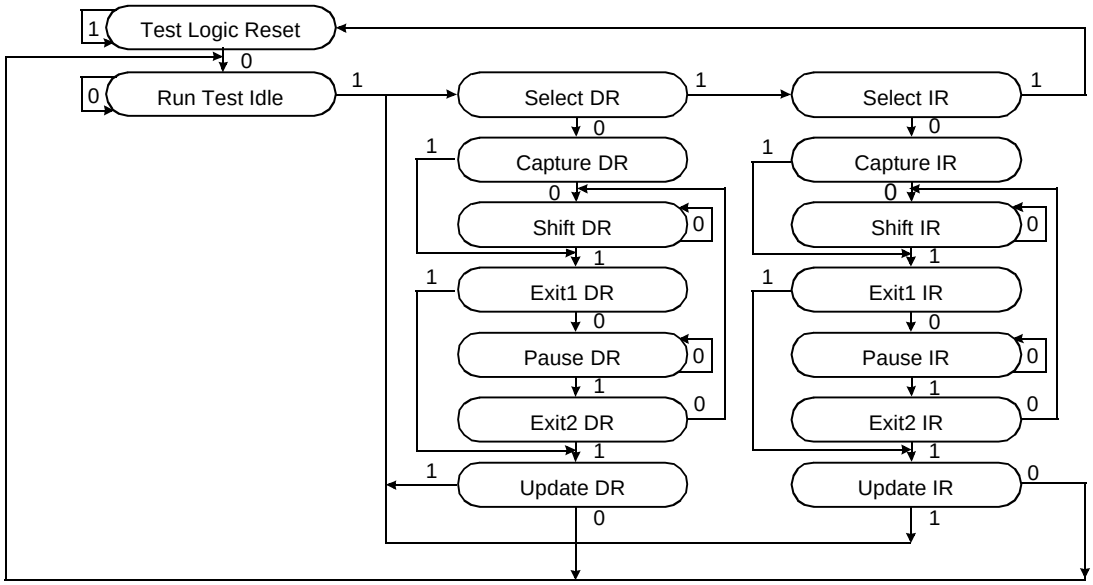

### JTAG Instruction Coding

| IR2 | IR1 | IR0 | Instruction | TDO Output | Notes |
|---|---|---|---|---|---|
| 0 | 0 | 0 | EXTEST | Boundary Scan Register | 1 |
| 0 | 0 | 1 | IDCODE | Identification Register | 3 |
| 0 | 1 | 0 | SAMPLE-Z | Boundary Scan Register | 2 |
| 0 | 1 | 1 | BYPASS | Bypass Register | 4 |
| 1 | 0 | 0 | SAMPLE | Boundary Scan Register | 5 |
| 1 | 0 | 1 | RESERVED | Do Not Use | 6 |
| 1 | 1 | 0 | BYPASS | Bypass Register | 4 |
| 1 | 1 | 1 | BYPASS | Bypass Register | 4 |

**NOTE** :

1. Places DQs in Hi-Z in order to sample all input data regardless of other SRAM inputs. This instruction is not IEEE 1149.1 compliant.
2. Places DQs in Hi-Z in order to sample all input data regardless of other SRAM inputs.
3. TDI is sampled as an input to the first ID register to allow for the serial shift of the external TDI data.
4. Bypass register is initiated to $V_{SS}$ when BYPASS instruction is invoked. The Bypass Register also holds serially loaded TDI when exiting the Shift DR states.
5. SAMPLE instruction dose not places DQs in Hi-Z.
6. This instruction is reserved for future use.

### TAP Controller State Diagram



## SCAN REGISTER DEFINITION

| Part | Instruction Register | Bypass Register | ID Register | Boundary Scan |
|---|---|---|---|---|
| 256Kx36 | 3 bits | 1 bits | 32 bits | 70 bits |
| 512Kx18 | 3 bits | 1 bits | 32 bits | 70 bits |

## ID REGISTER DEFINITION

| Part | Revision Number (31:28) | Part Configuration (27:18) | Vendor Definition (17:12) | Samsung JEDEC Code (11: 1) | Start Bit(0) |
|---|---|---|---|---|---|
| 256Kx36 | 0000 | 00110 00100 | XXXXXX | 00001001110 | 1 |
| 512Kx18 | 0000 | 00111 00011 | XXXXXX | 00001001110 | 1 |

## 119BGA BOUNDARY SCAN EXIT ORDER(x36)

| | | | | | | |
|---|---|---|---|---|---|---|
| 36 | 4B | ADV | | $\overline{OE}$ | 4F | 35 |
| 37 | 4E | $\overline{CS_1}$ | | A | 4G | 34 |
| 38 | 4H | $\overline{WE}$ | | CLK | 4K | 33 |
| 39 | 3G | $\overline{BW}$c | | $\overline{CKE}$ | 4M | 32 |
| 40 | 3C | A | | NC | 4A | 31 |
| 41 | 3B | A | | $\overline{BW}$b | 5G | 30 |
| 42 | 3A | A | | A | 5C | 29 |
| 43 | 2B | CS2 | | A | 5B | 28 |
| 44 | 2C | A | | A | 5A | 27 |
| 45 | 2A | A | | $\overline{CS_2}$ | 6B | 26 |
| 46 | 2D | DQPc | | A | 6A | 25 |
| 47 | 1E | DQc | | A | 6C | 24 |
| 48 | 2F | DQc | | DQPb | 6D | 23 |
| 49 | 1G | DQc | | DQb | 6E | 22 |
| 50 | 2H | DQc | | DQb | 6G | 21 |
| 51 | 1D | DQc | | DQb | 7H | 20 |
| 52 | 2E | DQc | | DQb | 7D | 19 |
| 53 | 2G | DQc | | DQb | 7E | 18 |
| 54 | 1H | DQc | | DQb | 6F | 17 |
| 55 | 2K | DQd | | DQb | 7G | 16 |
| 56 | 1L | DQd | | DQb | 6H | 15 |
| 57 | 2M | DQd | | DQa | 7K | 14 |
| 58 | 1N | DQd | | DQa | 6L | 13 |
| 59 | 1P | DQd | | DQa | 6N | 12 |
| 60 | 1K | DQd | | DQa | 7P | 11 |
| 61 | 2L | DQd | | DQa | 6K | 10 |
| 62 | 2N | DQd | | DQa | 7L | 9 |
| 63 | 2P | DQPd | | DQa | 6M | 8 |
| 64 | 3R | $\overline{LBO}$ | | DQa | 7N | 7 |
| 65 | 3L | $\overline{BW}$d | | DQPa | 6P | 6 |
| 66 | 2R | A | | ZZ | 7T | 5 |
| 67 | 3T | A | | A | 6R | 4 |
| 68 | 4N | A1 | | $\overline{BW}$a | 5L | 3 |
| 69 | 4P | A0 | | A | 5T | 2 |
| 70 | 2T | NC | | A | 4T | 1 |

## 119BGA BOUNDARY SCAN EXIT ORDER(x18)

| | | | | | | |
|---|---|---|---|---|---|---|
| 36 | 4B | ADV | | $\overline{OE}$ | 4F | 35 |
| 37 | 4E | $\overline{CS_1}$ | | A | 4G | 34 |
| 38 | 4H | $\overline{WE}$ | | CLK | 4K | 33 |
| 39 | 3G | $\overline{BW}$b | | $\overline{CKE}$ | 4M | 32 |
| 40 | 3C | A | | NC | 4A | 31 |
| 41 | 3B | A | | NC | 5G | 30 |
| 42 | 3A | A | | A | 5C | 29 |
| 43 | 2B | CS2 | | A | 5B | 28 |
| 44 | 2C | A | | A | 5A | 27 |
| 45 | 2A | A | | $\overline{CS_2}$ | 6B | 26 |
| 46 | 2D | NC | | A | 6A | 25 |
| 47 | 1E | NC | | A | 6C | 24 |
| 48 | 2F | NC | | NC | 7D | 23 |
| 49 | 1G | NC | | NC | 6E | 22 |
| 50 | 2H | NC | | NC | 6G | 21 |
| 51 | 1D | DQb | | NC | 7H | 20 |
| 52 | 2E | DQb | | DQPa | 6D | 19 |
| 53 | 2G | DQb | | DQa | 7E | 18 |
| 54 | 1H | DQb | | DQa | 6F | 17 |
| 55 | 2K | DQb | | DQa | 7G | 16 |
| 56 | 1L | DQb | | DQa | 6H | 15 |
| 57 | 2M | DQb | | DQa | 7K | 14 |
| 58 | 1N | DQb | | DQa | 6L | 13 |
| 59 | 2P | DQPb | | DQa | 6N | 12 |
| 60 | 1K | NC | | DQa | 7P | 11 |
| 61 | 2L | NC | | NC | 6K | 10 |
| 62 | 2N | NC | | NC | 7L | 9 |
| 63 | 1P | NC | | NC | 6M | 8 |
| 64 | 3R | $\overline{LBO}$ | | NC | 7N | 7 |
| 65 | 3L | NC | | NC | 6P | 6 |
| 66 | 2R | A | | ZZ | 7T | 5 |
| 67 | 3T | A | | A | 6R | 4 |
| 68 | 4N | A1 | | $\overline{BW}$a | 5L | 3 |
| 69 | 4P | A0 | | A | 5T | 2 |
| 70 | 2T | A | | A | 6T | 1 |

**NOTE** : NC ; Dont care.

## JTAG DC OPERATING CONDITIONS

| Parameter | Symbol | Min | Typ | Max | Unit | Note |
|---|---|---|---|---|---|---|
| Power Supply Voltage | $V_{DD}$ | 2.375 | 2.5 | 2.625 | V | |
| Input High Level | $V_{IH}$ | 1.7 | - | $V_{DD}$+0.3 | V | 1 |
| Input Low Level | $V_{IL}$ | -0.3 | - | 0.7 | V | |
| Output High Voltage | $V_{OH}$ | 2.0 | - | - | V | |
| Output Low Voltage | $V_{OL}$ | - | - | 0.4 | V | |

**NOTE** : The input level of SRAM pin is to follow the SRAM DC specification.

1. In Case of I/O Pins, the Max. $V_{IH}=V_{DDQ}$+0.3V

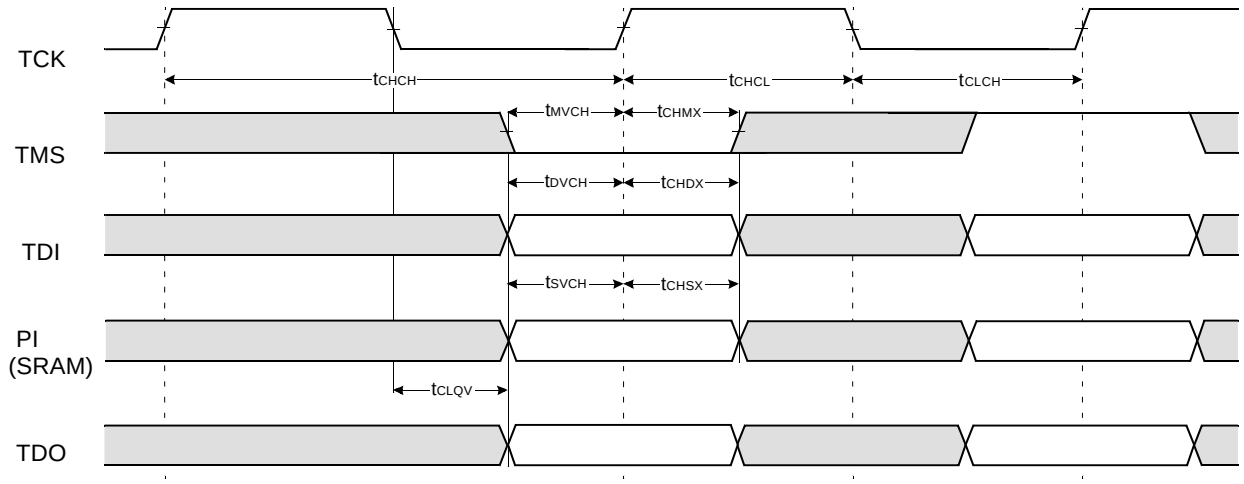
## JTAG AC TEST CONDITIONS

| Parameter | Symbol | Min | Unit | Note |
|---|---|---|---|---|
| Input High/Low Level | $V_{IH}/V_{IL}$ | 2.5 / 0 | V | |
| Input Rise/Fall Time | TR/TF | 1.0 /1 .0 | ns | |
| Input and Output Timing Reference Level | | $V_{DDQ}/2$ | V | |

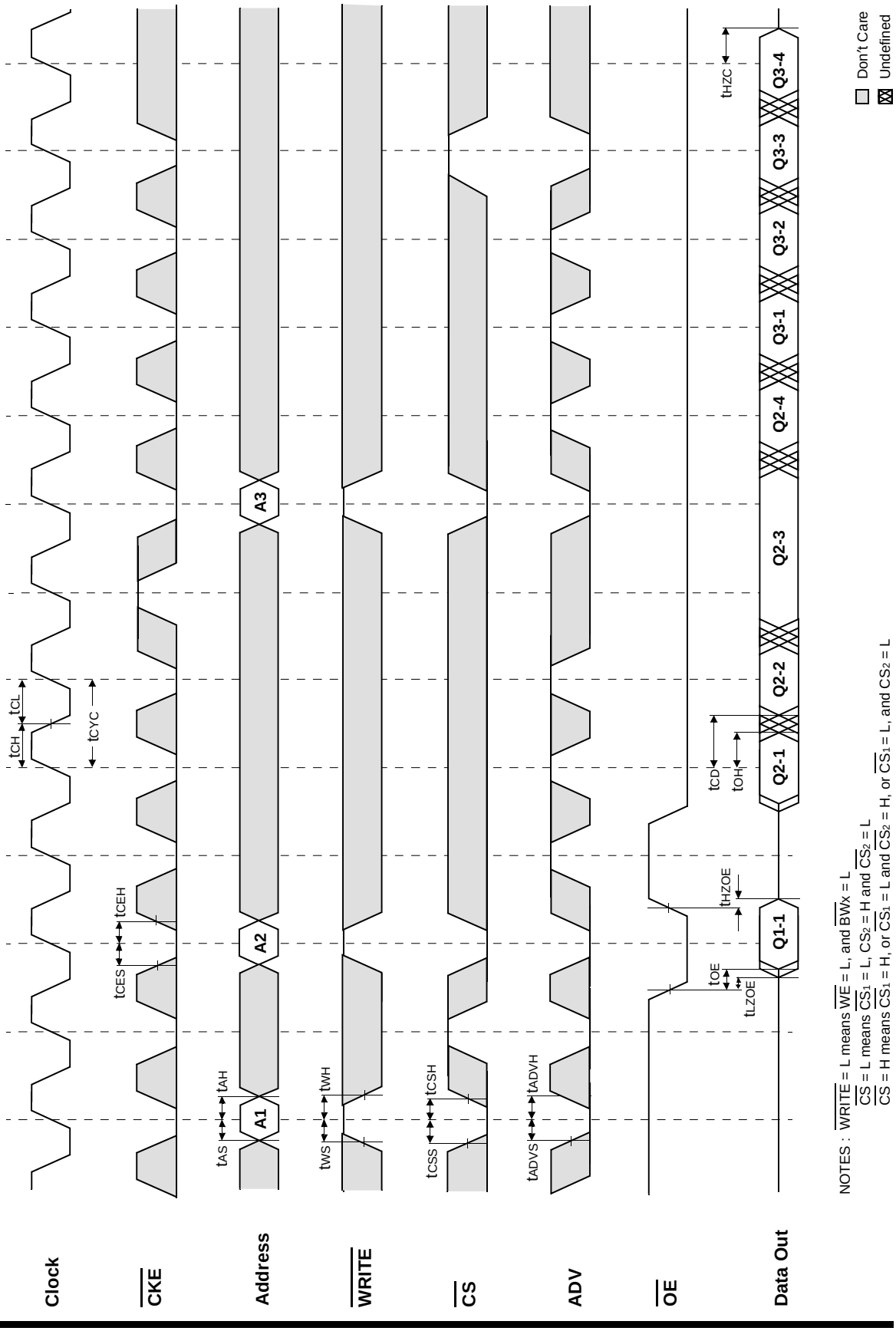
## JTAG AC Characteristics

| Parameter | Symbol | Min | Max | Unit | Note |
|---|---|---|---|---|---|
| TCK Cycle Time | $t_{CHCH}$ | 50 | - | ns | |
| TCK High Pulse Width | $t_{CHCL}$ | 20 | - | ns | |
| TCK Low Pulse Width | $t_{CLCH}$ | 20 | - | ns | |
| TMS Input Setup Time | $t_{MVCH}$ | 5 | - | ns | |
| TMS Input Hold Time | $t_{CHMX}$ | 5 | - | ns | |
| TDI Input Setup Time | $t_{DVCH}$ | 5 | - | ns | |
| TDI Input Hold Time | $t_{CHDX}$ | 5 | - | ns | |
| SRAM Input Setup Time | $t_{SVCH}$ | 5 | - | ns | |
| SRAM Input Hold Time | $t_{CHSX}$ | 5 | - | ns | |
| Clock Low to Output Valid | $t_{CLQV}$ | 0 | 10 | ns | |

## JTAG TIMING DIAGRAM

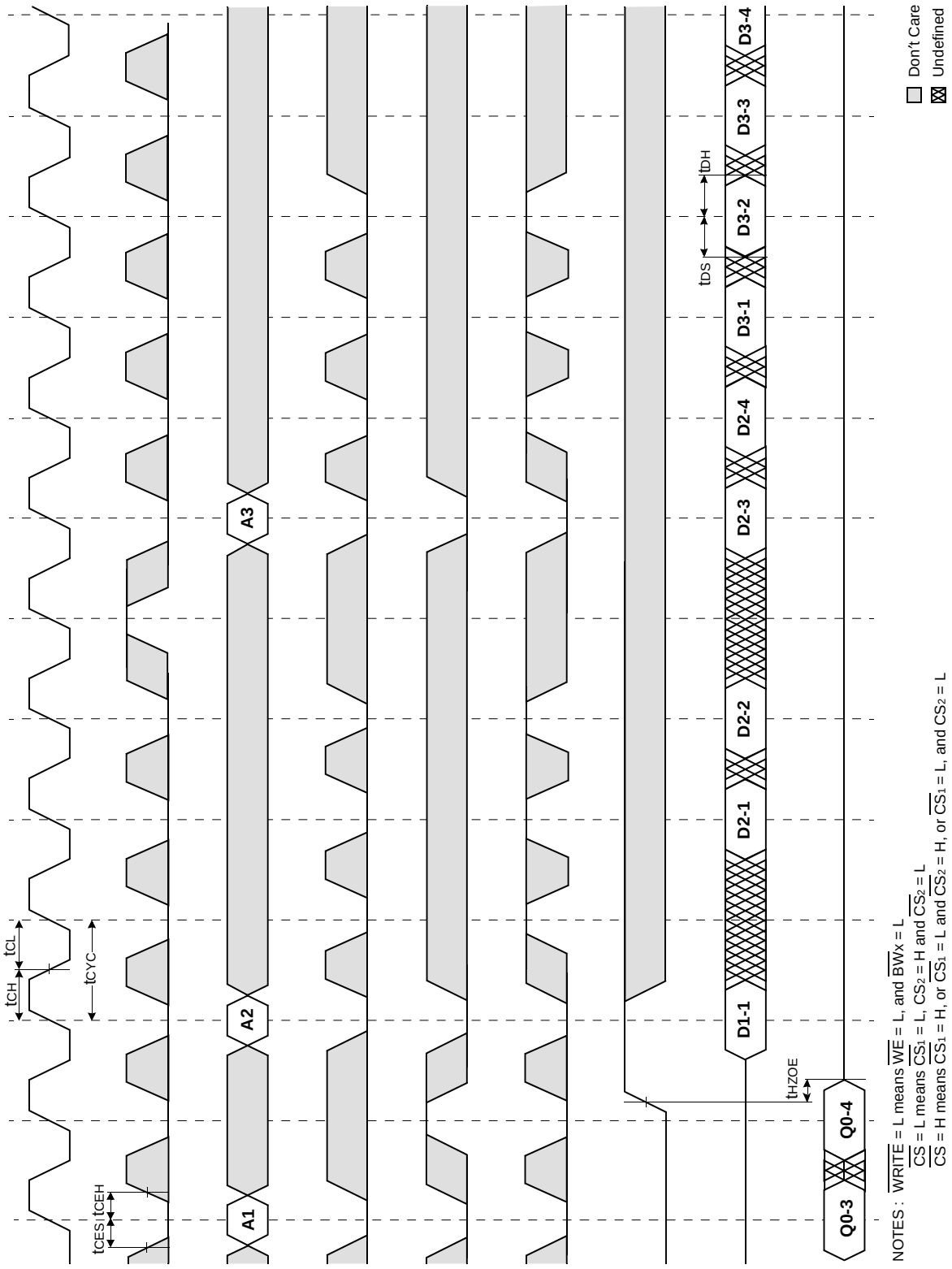


## TIMING WAVEFORM OF READ CYCLE



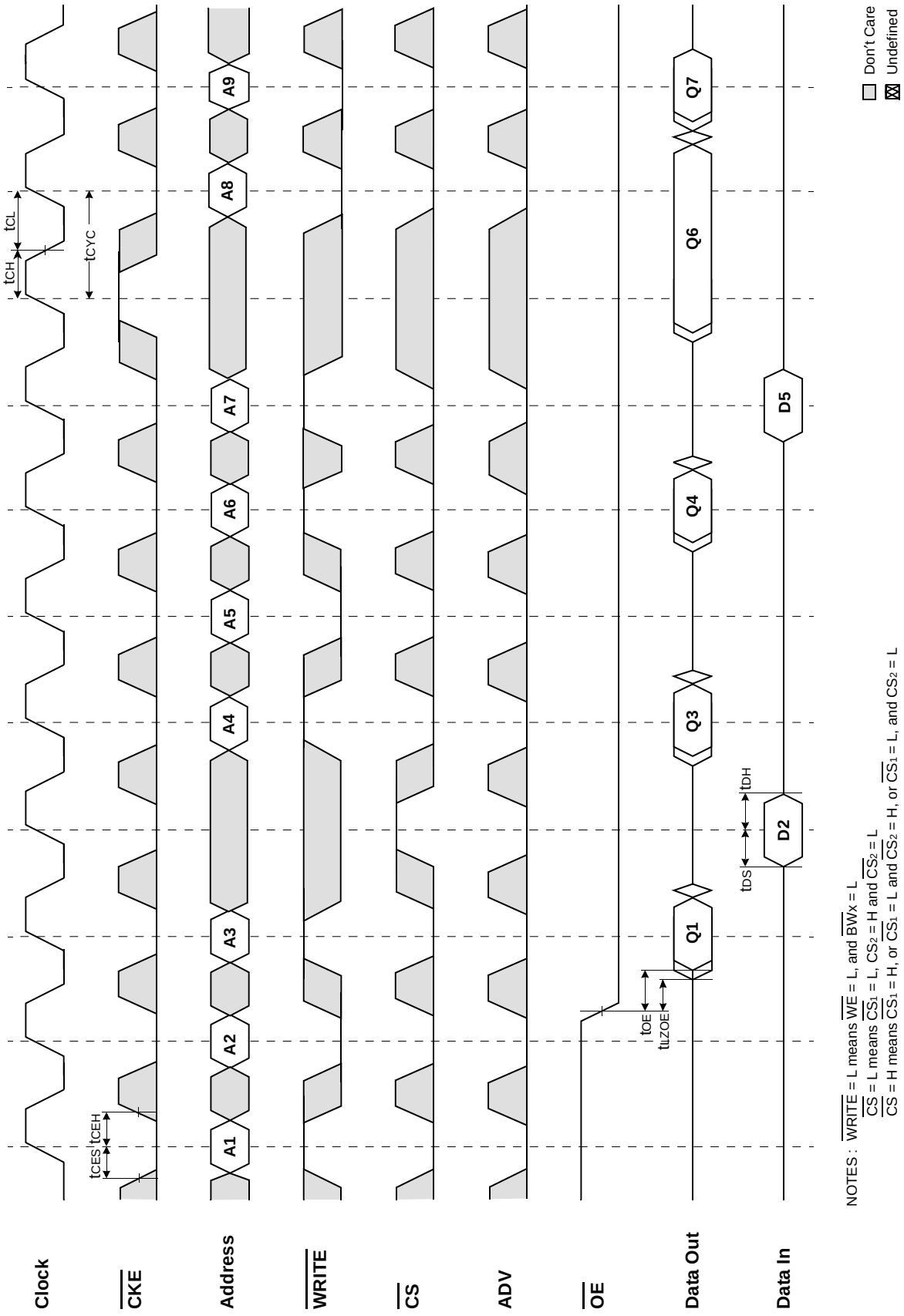

NOTES : $\overline{WRITE}$ = L means $\overline{WE}$ = L, and $\overline{BWx}$ = L
$\overline{CS}$ = L means $\overline{CS_1}$ = L, $CS_2$ = H and $\overline{CS_2}$ = L
CS = H means $\overline{CS_1}$ = H, or $\overline{CS_1}$ = L and $\overline{CS_2}$ = H, or $\overline{CS_1}$ = L, and $\overline{CS_2}$ = L

## TIMING WAVEFORM OF WRTE CYCLE

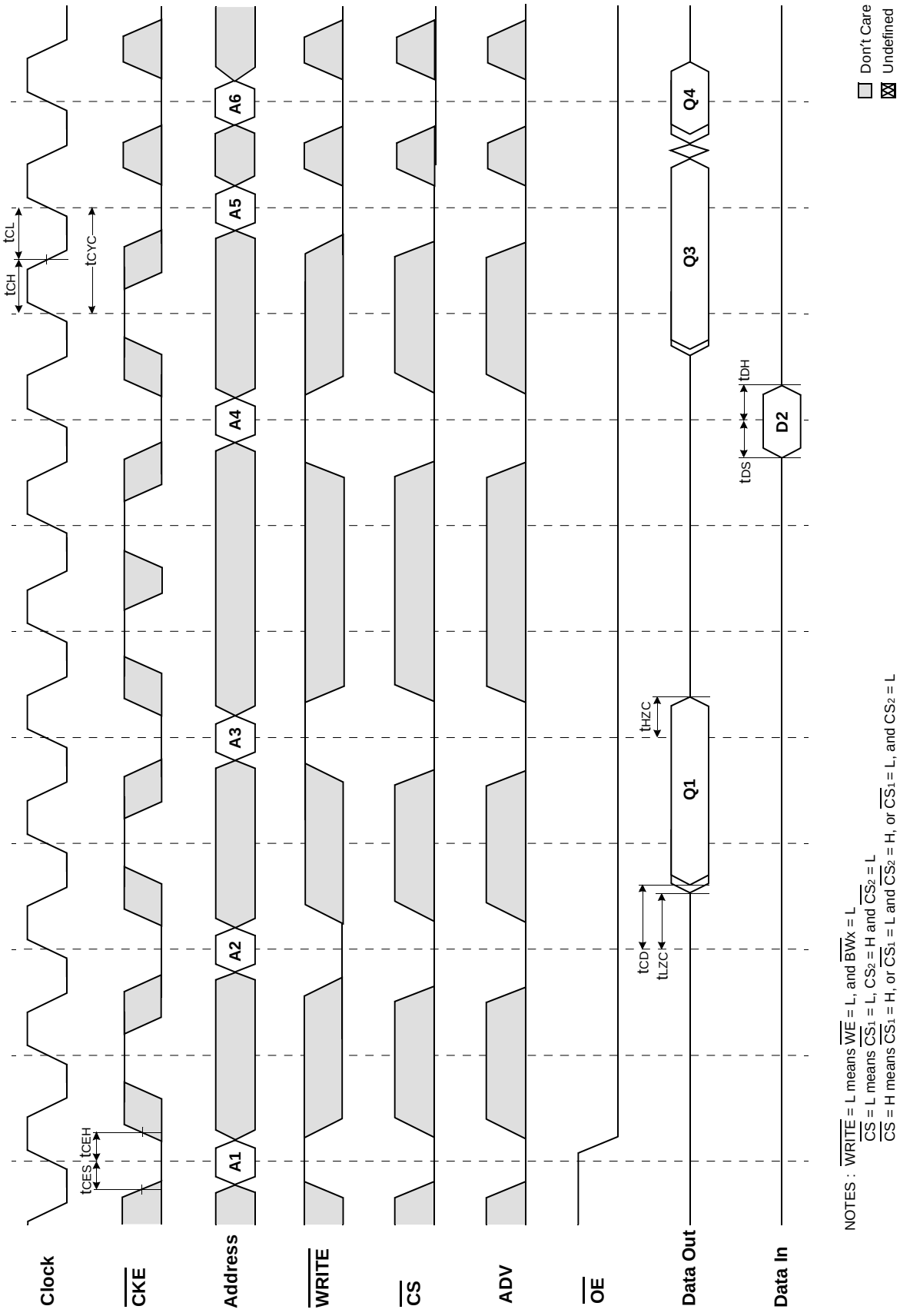



NOTES : WRITE = L means WE = L, and BWx = L
CS = L means CS1 = L, CS2 = H and CS2 = L
CS = H means CS1 = H, or CS1 = L and CS2 = H, or CS1 = L, and CS2 = L

## TIMING WAVEFORM OF SINGLE READ/WRITE

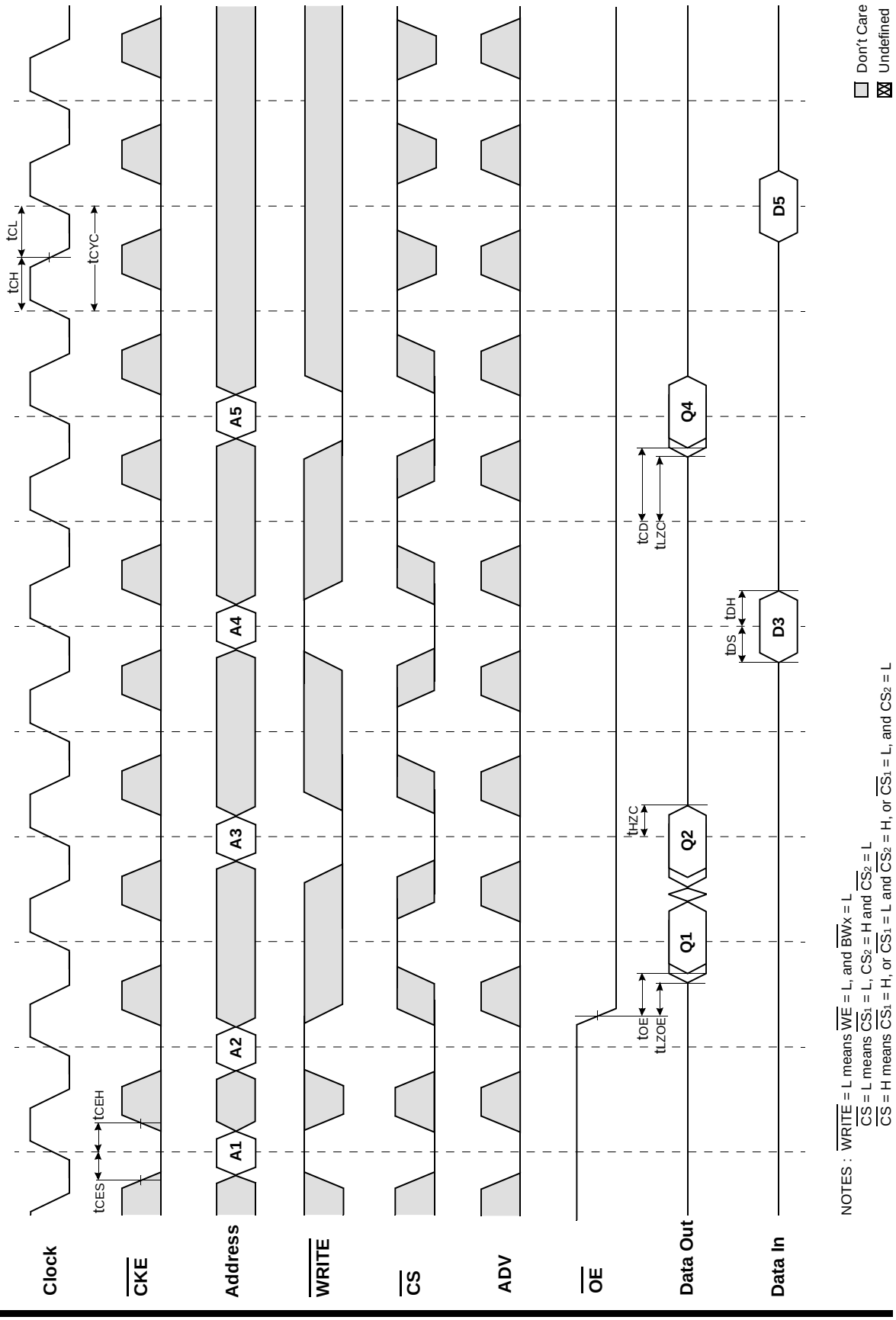


## TIMING WAVEFORM OF $\overline{CKE}$ OPERATION




NOTES : $\overline{WRITE}$ = L means $\overline{WE}$ = L, and $\overline{BWx}$ = L
$\overline{CS}$ = L means $\overline{CS_1}$ = L, $CS_2$ = H and $\overline{CS_2}$ = L
$\overline{CS}$ = H means $\overline{CS_1}$ = H, or $\overline{CS_1}$ = L and $\overline{CS_2}$ = H, or $\overline{CS_1}$ = L, and $\overline{CS_2}$ = L

## TIMING WAVEFORM OF $\overline{CS}$ OPERATION

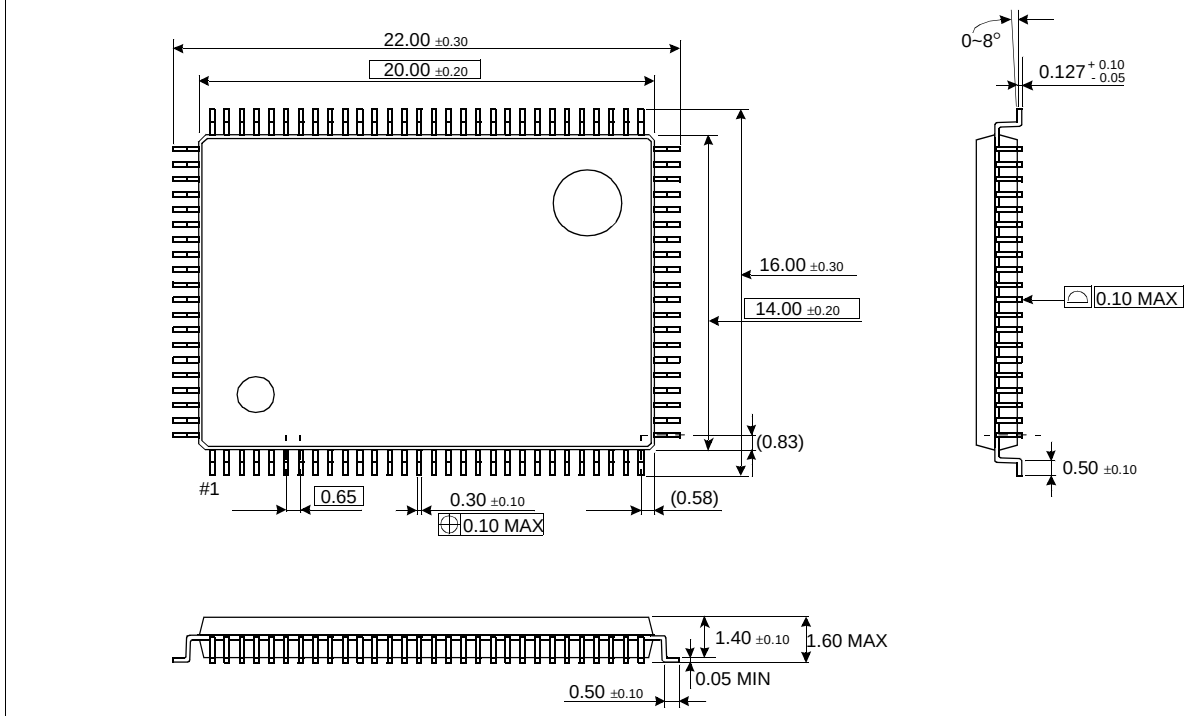



NOTES : $\overline{WRITE}$ = L means $\overline{WE}$ = L, and $\overline{BWx}$ = L
$\overline{CS}$ = L means $\overline{CS_1}$ = L, $CS_2$ = H and $\overline{CS_2}$ = L
$\overline{CS}$ = H means $\overline{CS_1}$ = H, or $\overline{CS_1}$ = L and $\overline{CS_2}$ = H, or $\overline{CS_1}$ = L, and $CS_2$ = L

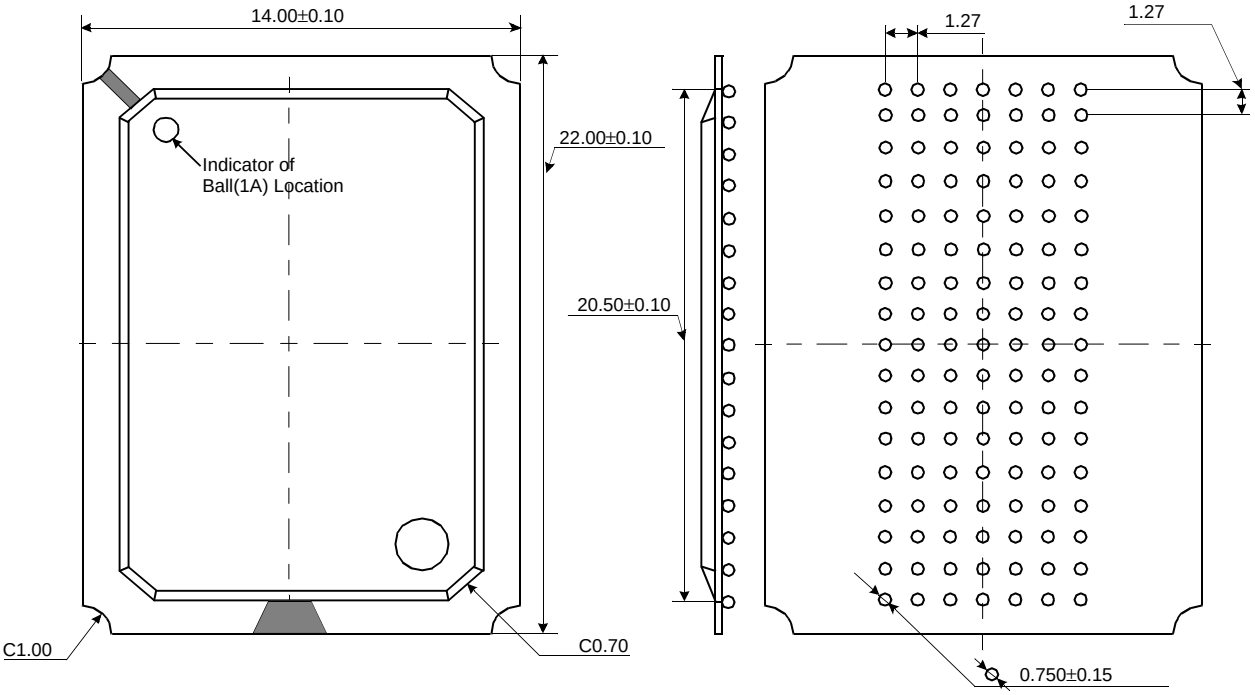
## PACKAGE DIMENSIONS

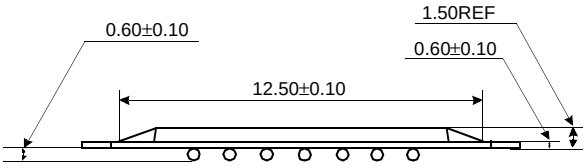
**100-TQFP-1420A**

Units ; millimeters/Inches



## 119BGA PACKAGE DIMENSIONS




**Notes**

1. All Dimensions are in Millimeters.
2. Solder Ball to PCB Offset : 0.10 MAX.
3. PCB to Cavity Offset : 0.10 MAX.