Document Title

32Kx8 bit Low Power and Low Voltage CMOS Static RAM

Revision History

Revision No.	History	Draft Data	Remark
0.0	Initial draft	April 1, 1997	Preliminary
1.0	Finalize - Add 70ns part in KM62U256D Family - Show I_{CC} read only, and increased value I_{CC} = 2mA →I_{CC} Read = 5mA - Seperate I_{CC1} read and write I_{CC1} = 5mA→I_{CC1} Read = 5mA, I_{CC1} Write = 10mA - Improved standby current(I_{SB1}) Commercial part: 10μA→5μA Extended and Industrial part: 20μA→5μA - Improved V_{IL}(Min.): 0.4V→0.6V - Improved power dissipation: 0.7W→1W	November 12, 1997	Final
1.01	Errata correction - Removed 'TTL Compatible'from Features - Errata correction from 4.5V to 3.0/2.7V for DATA RETENTION WAVE FORM	October 24, 2001	Final

32Kx8 bit Low Power and Low Voltage CMOS Static RAM

FEATURES

- Process Technology: 0.4μm CMOS
- Organization: 32Kx8
- Power Supply Voltage
  K6T0808V1D family: 3.0~3.6V
  K6T0808U1D family: 2.7~3.3V
- Low Data Retention Voltage: 2V(Min)
- Three State Outputs
- Package Type: 28-SOP-450, 28-TSOP1-0813.4F/R

GENERAL DESCRIPTION

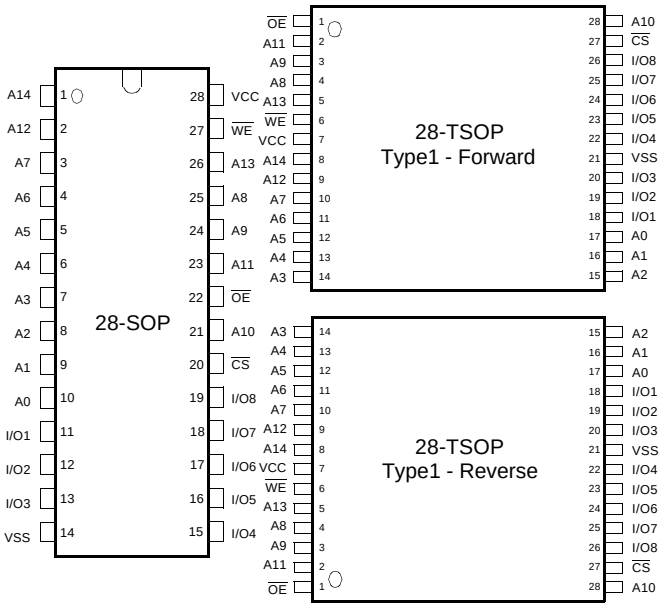
The K6T0808V1D and K6T0808U1D families are fabricated by SAMSUNG's advanced CMOS process technology. The families support various operating temperature range and have various package types for user flexibility of system design. The families also support low data retention voltage for battery back-up operation with low data retention current.

PRODUCT FAMILY

Product Family	Operating Temperature	Vcc Range	Speed	Power Dissipation		PKG Type
				Standby (I_{SB1}, Max)	Operating (I_{CC2}, Max)	
K6T0808V1D-B	Commercial(0~70°C)	3.0V ~3.6V	70[1]/100ns	5μA	35mA	28-SOP-450[2] 28-TSOP1-0813.4F/R
K6T0808U1D-B		2.7V ~ 3.3V	70[1]/85/100ns			
K6T0808V1D-D	Extended(-25~85°C)	3.0V ~3.6V	70[1]/100ns			
K6T0808U1D-D		2.7V ~ 3.3V	70[1]/85/100ns			
K6T0808V1D-F	Industrial(-40~85°C)	3.0V ~3.6V	70[1]/100ns			
K6T0808U1D-F		2.7V ~ 3.3V	70[1]/85/100ns			

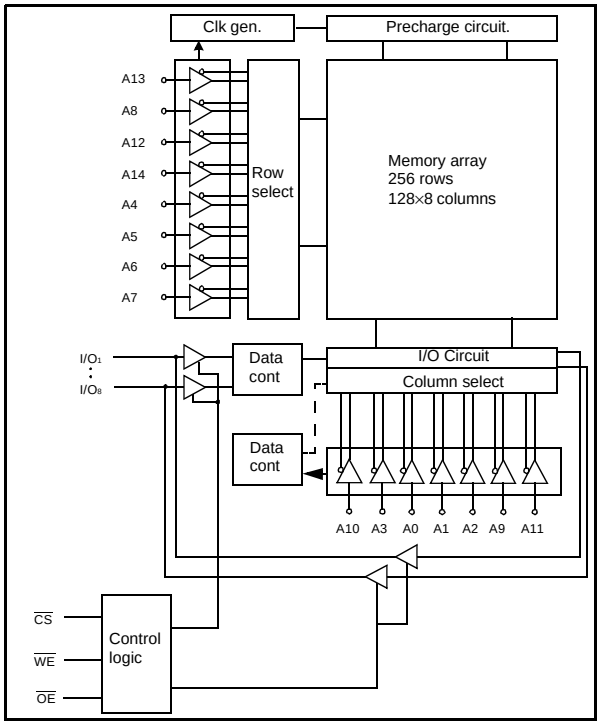
1. The parameter is measured with 30pF test load.
2. K6T0808V1D Family support SOP package without 100ns speed bin.

PIN DESCRIPTION



Pin Name	Function	Pin Name	Function
A_0~A_{14}	Address Inputs	I/O_1~I/O_8	Data Inputs/Outputs
$\overline{WE}$	Write Enable Input	Vcc	Power
$\overline{CS}$	Chip Select Input	Vss	Ground
$\overline{OE}$	Output Enable Input	NC	No connect

FUNCTIONAL BLOCK DIAGRAM



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PRODUCT LIST

Commercial Temp. Product (0~70°C)		Extended Temp. Products (-25~85°C)		Industrial Temp Products (-40~85°C)	
Part Name	**Function**	**Part Name**	**Function**	**Part Name**	**Function**
K6T0808V1D-GB70	28-SOP, 70ns, 3.3V	K6T0808V1D-GD70	28-SOP, 70ns, 3.3V	K6T0808V1D-GF70	28-SOP, 70ns, 3.3V
K6T0808V1D-TB70	28-TSOP-F, 70ns, 3.3V	K6T0808V1D-TD70	28-TSOP F, 70ns, 3.3V	K6T0808V1D-TF70	28-TSOP F, 70ns, 3.3V
K6T0808V1D-TB10	28-TSOP-F, 100ns, 3.3V	K6T0808V1D-TD10	28-TSOP F, 100ns, 3.3V	K6T0808V1D-TF10	28-TSOP F, 100ns, 3.3V
K6T0808V1D-RB70	28-TSOP-R, 70ns, 3.3V	K6T0808V1D-RD70	28-TSOP R, 70ns, 3.3V	K6T0808V1D-RF70	28-TSOP R, 70ns, 3.3V
K6T0808V1D-RB10	28-TSOP-R, 100ns, 3.3V	K6T0808V1D-RD10	28-TSOP R, 100ns, 3.3V	K6T0808V1D-RF10	28-TSOP R, 100ns, 3.3V
K6T0808U1D-GB70	28-SOP, 70ns, 3.0V	K6T0808U1D-GD70	28-SOP, 70ns, 3.0V	K6T0808U1D-GF70	28-SOP, 70ns, 3.0V
K6T0808U1D-GB85	28-SOP, 85ns, 3.0V	K6T0808U1D-GD85	28-SOP, 85ns, 3.0V	K6T0808U1D-GF85	28-SOP, 85ns, 3.0V
K6T0808U1D-GB10	28-SOP, 100ns, 3.0V	K6T0808U1D-GD10	28-SOP, 100ns, 3.0V	K6T0808U1D-GF10	28-SOP, 100ns, 3.0V
K6T0808U1D-TB70	28-TSOP-F, 70ns, 3.0V	K6T0808U1D-TD70	28-TSOP-F, 70ns, 3.0V	K6T0808U1D-TF70	28-TSOP-F, 70ns, 3.0V
K6T0808U1D-TB85	28-TSOP-F, 85ns, 3.0V	K6T0808U1D-TD85	28-TSOP-F, 85ns, 3.0V	K6T0808U1D-TF85	28-TSOP-F, 85ns, 3.0V
K6T0808U1D-TB10	28-TSOP-F, 100ns, 3.0V	K6T0808U1D-TD10	28-TSOP-F, 100ns, 3.0V	K6T0808U1D-TF10	28-TSOP-F, 100ns, 3.0V
K6T0808U1D-RB70	28-TSOP-R, 70ns, 3.0V	K6T0808U1D-RD70	28-TSOP-R, 70ns, 3.0V	K6T0808U1D-RF70	28-TSOP-R, 70ns, 3.0V
K6T0808U1D-RB85	28-TSOP-R, 85ns, 3.0V	K6T0808U1D-RD85	28-TSOP-R, 85ns, 3.0V	K6T0808U1D-RF85	28-TSOP-R, 85ns, 3.0V
K6T0808U1D-RB10	28-TSOP-R, 100ns, 3.0V	K6T0808U1D-RD10	28-TSOP-R, 100ns, 3.0V	K6T0808U1D-RF10	28-TSOP-R, 100ns, 3.0V

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	I/O	Mode	Power
H	X[1]	X[1]	High-Z	Deselected	Standby
L	H	H	High-Z	Output Disabled	Active
L	L	H	Dout	Read	Active
L	X[1]	L	Din	Write	Active

1. X means don't care (Must be in high or low states)

ABSOLUTE MAXIMUM RATINGS[1]

Item	Symbol	Ratings	Unit	Remark
Voltage on any pin relative to Vss	V_{IN},V_{OUT}	-0.5 to V_{CC}+0.5	V	-
Voltage on Vcc supply relative to Vss	V_{CC}	-0.5 to 4.6	V	-
Power Dissipation	P_D	1.0	W	-
Storage temperature	T_{STG}	-65 to 150	°C	-
Operating Temperature	T_A	0 to 70	°C	K6T0808V1D-B, K6T0808U1D-B
		-25 to 85	°C	K6T0808V1D-D, K6T0808U1D-D
		-40 to 85	°C	K6T0808V1D-F, K6T0808U1D-F
Soldering temperature and time	T_{SOLDER}	260°C, 10sec (Lead Only)	-	-

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation should be restricted to recommended operating condition. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS[1)]

Item	Symbol	Product	Min	Typ	Max	Unit
Supply voltage	Vcc	K6T0808V1D Family	3.0	3.3	3.6	V
		K6T0808U1D Family	2.7	3.0	3.3	
Ground	Vss	ALL	0	0	0	V
Input high voltage	V_{IH}	K6T0808V1D, K6T0808U1D Family	2.2	-	Vcc+0.3	V
Input low voltage	V_{IL}	K6T0808V1D, K6T0808U1D Family	-0.3[3)]	-	0.6	V

Note:
1. Commercial Product: T_A=0 to 70°C, otherwise specified
   Industrial Product: T_A=-40 to 85°C, otherwise specified
2. Overshoot: V_{CC}+3.0V in case of pulse width≤30ns
3. Undershoot: -3.0V in case of pulse width≤30ns
4. Overshoot and undershoot are sampled, not 100% tested

CAPACITANCE[1)] (f=1MHz, TA=25°C)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	C_{IN}	V_{IN}=0V	-	8	pF
Input/Output capacitance	C_{IO}	V_{IO}=0V	-	10	pF

1. Capacitance is sampled, not 100% tested

DC AND OPERATING CHARACTERISTICS

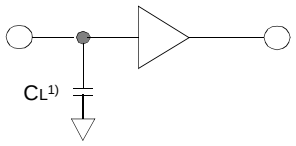
Item	Symbol	Test Conditions		Min	Typ	Max	Unit
Input leakage current	I_{LI}	V_{IN}=Vss to Vcc		-1	-	1	µA
Output leakage current	I_{LO}	$\overline{CS}$=V_{IH} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL}, V_{IO}=Vss to Vcc		-1	-	1	µA
Operating power supply current	I_{CC}	I_{IO}=0mA, $\overline{CS}$=V_{IL}, V_{IN}=V_{IH} or V_{IL}, Read		-	2	5	mA
Average operating current	I_{CC1}	Cycle time=1µs, 100% duty, I_{IO}=0mA, $\overline{CS}$≤0.2V, V_{IN}≤0.2V, V_{IN}≥Vcc -0.2V	Read	-	1.5	5	mA
			Write	-	6	10	
	I_{CC2}	Cycle time=Min,100% duty, I_{IO}=0mA, $\overline{CS}$=V_{IL}, V_{IN}=V_{IH} or V_{IL}		-	23	35	mA
Output low voltage	V_{OL}	I_{OL}=2.1mA		-	-	0.4	V
Output high voltage	V_{OH}	I_{OH}=-1.0mA		2.4	-	-	V
Standby Current(TTL)	I_{SB}	$\overline{CS}$=V_{IH}, Other inputs = V_{IL} or V_{IH}		-	-	0.3	mA
Standby Current (CMOS)	I_{SB1}	$\overline{CS}$≥Vcc-0.2V, Other inputs=0~Vcc		-	0.1	5	µA

AC OPERATING CONDITIONS

TEST CONDITIONS (Test Load and Test Input/Output Reference)

Input pulse level: 0.4 to 2.4V
Input rising and falling time: 5ns
Input and output reference voltage: 1.5V
Output load (See right): C_L=100pF+1TTL
C_L[1)]=30pF+1TTL

1. Refer to AC CHARACTERISTICS



1. Including scope and jig capacitance

AC CHARACTERISTICS (K6T0808V1D Family: Vcc=3.0~3.6V, , K6T0808U1D Family: Vcc=2.7~3.3V

Commercial product: T_A=0 to 70°C, Extended product: T_A=-25 to 85°C, Industrial product: T_A=-40 to 85°C)

Parameter List		Symbol	Speed Bins						Units
			70[1)]ns		85ns		100ns		
			Min	Max	Min	Max	Min	Max	
Read	Read cycle time	t_{RC}	70	-	85	-	100	-	ns
	Address access time	t_{AA}	-	70	-	85	-	100	ns
	Chip select to output	t_{CO}	-	70	-	85	-	100	ns
	Output enable to valid output	t_{OE}	-	35	-	40	-	50	ns
	Chip select to low-Z output	t_{LZ}	10	-	10	-	10	-	ns
	Output enable to low-Z output	t_{OLZ}	5	-	5	-	5	-	ns
	Chip disable to high-Z output	t_{HZ}	0	30	0	30	0	35	ns
	Output disable to high-Z output	t_{OHZ}	0	30	0	30	0	35	ns
	Output hold from address	t_{OH}	5	-	10	-	15	-	ns
Write	Write cycle time	t_{WC}	70	-	85	-	100	-	ns
	Chip select to end of write	t_{CW}	60	-	70	-	80	-	ns
	Address set-up time	t_{AS}	0	-	0	-	0	-	ns
	Address valid to end of write	t_{AW}	60	-	70	-	80	-	ns
	Write pulse width	t_{WP}	50	-	60	-	70	-	ns
	Write recovery time	t_{WR}	0	-	0	-	0	-	ns
	Write to output high-Z	t_{WHZ}	0	25	0	25	0	35	ns
	Data to write time overlap	t_{DW}	30	-	35	-	40	-	ns
	Data hold from write time	t_{DH}	0	-	0	-	0	-	ns
	End write to output low-Z	t_{OW}	5	-	10	-	10	-	ns

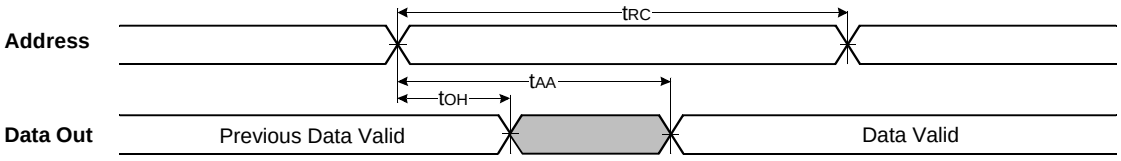
1. The parameter is measured with 30pF test load

DATA RETENTION CHARACTERISTICS

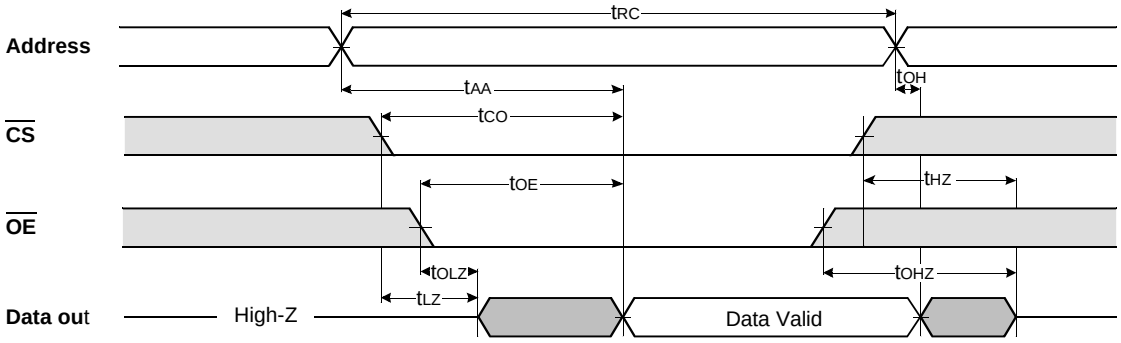
Item	Symbol	Test Condition	Min	Typ	Max	Unit
Vcc for data retention	V_{DR}	$\overline{CS}$≥Vcc-0.2V	2.0	-	3.6	V
Data retention current	I_{DR}	Vcc=3.0V, $\overline{CS}$≥Vcc-0.2V	-		5	µA
Data retention set-up time	t_{SDR}	See data retention waveform	0	-	-	ms
Recovery time	t_{RDR}		5	-	-	

TIMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled, $\overline{CS}$=$\overline{OE}$=V_{IL}, $\overline{WE}$=V_{IH})



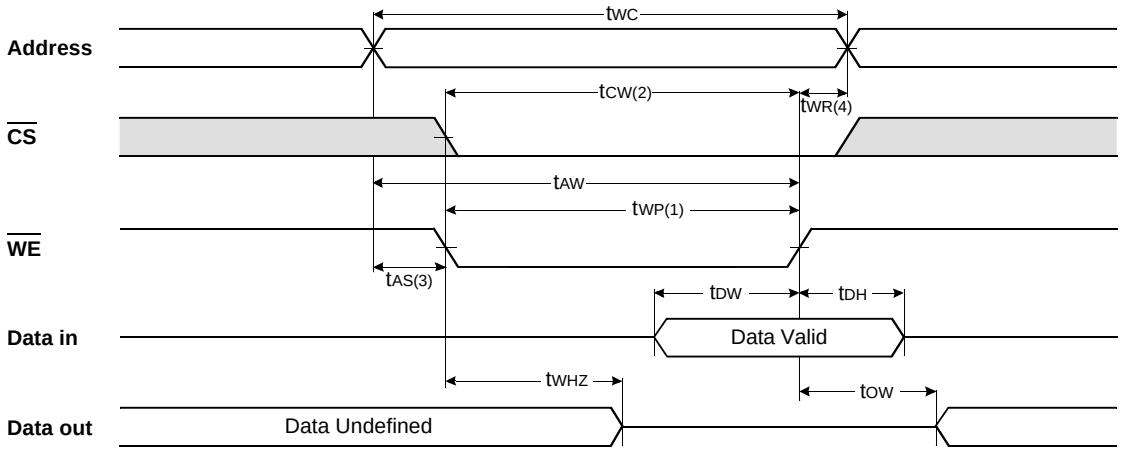
TIMING WAVEFORM OF READ CYCLE(2) ($\overline{WE}$=V_{IH})



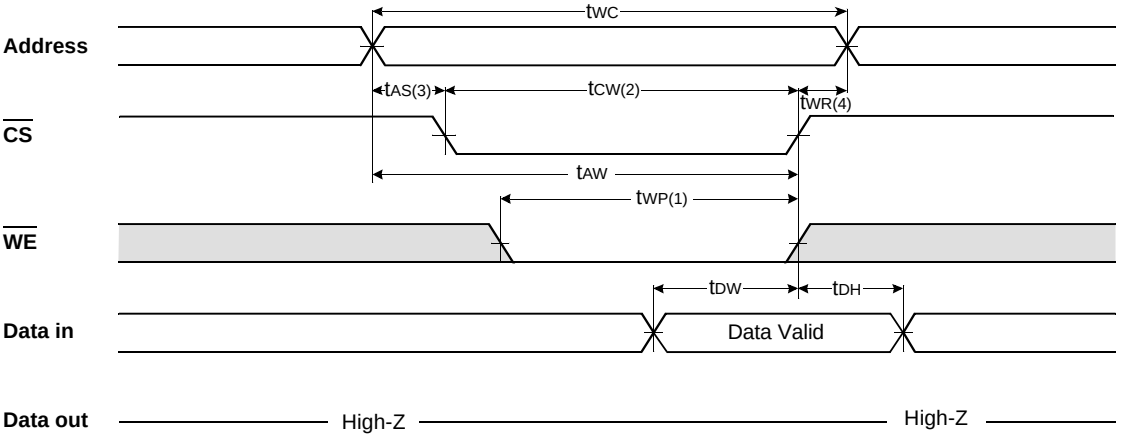
NOTES (READ CYCLE)

1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, t_{HZ}(Max.) is less than t_{LZ}(Min.) both for a given device and from device to device interconnection.

TIMING WAVEFORM OF WRITE CYCLE(1) ($\overline{WE}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE(2) ($\overline{CS}$ Controlled)

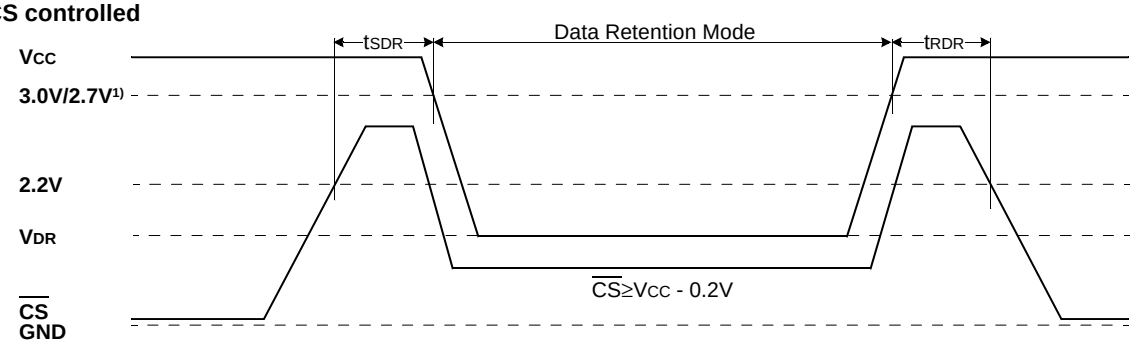


NOTES (WRITE CYCLE)

1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$. A write begins at the latest transition among $\overline{CS}$ going Low and $\overline{WE}$ going low : A write end at the earliest transition among $\overline{CS}$ going high and $\overline{WE}$ going high, t_{WP} is measured from the begining of write to the end of write.
2. t_{CW} is measured from the $\overline{CS}$ going low to the end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change. t_{WR} is applied in case a write ends with $\overline{CS}$ or $\overline{WE}$ going high.

DATA RETENTION WAVE FORM

$\overline{CS}$ controlled

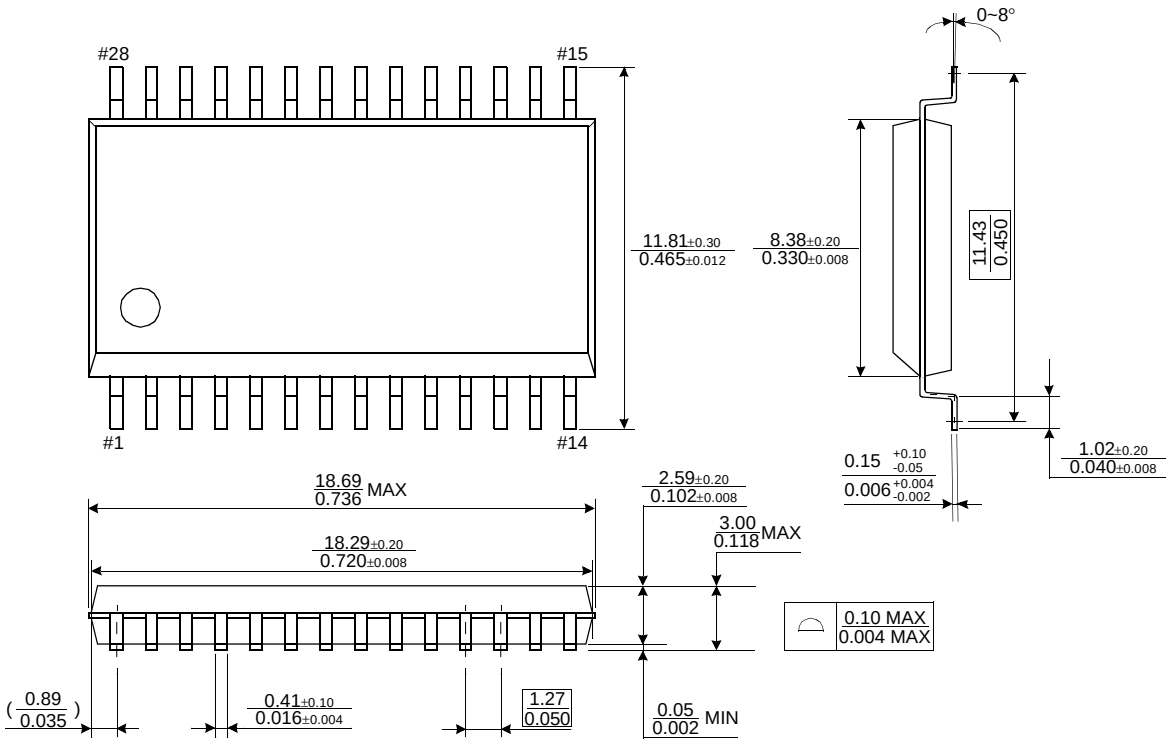


1. 3.0V for K6T0808V1D Family, 2.7V for K6T0808U1D Family

PACKAGE DIMENSIONS

Units: millimeter(inch)

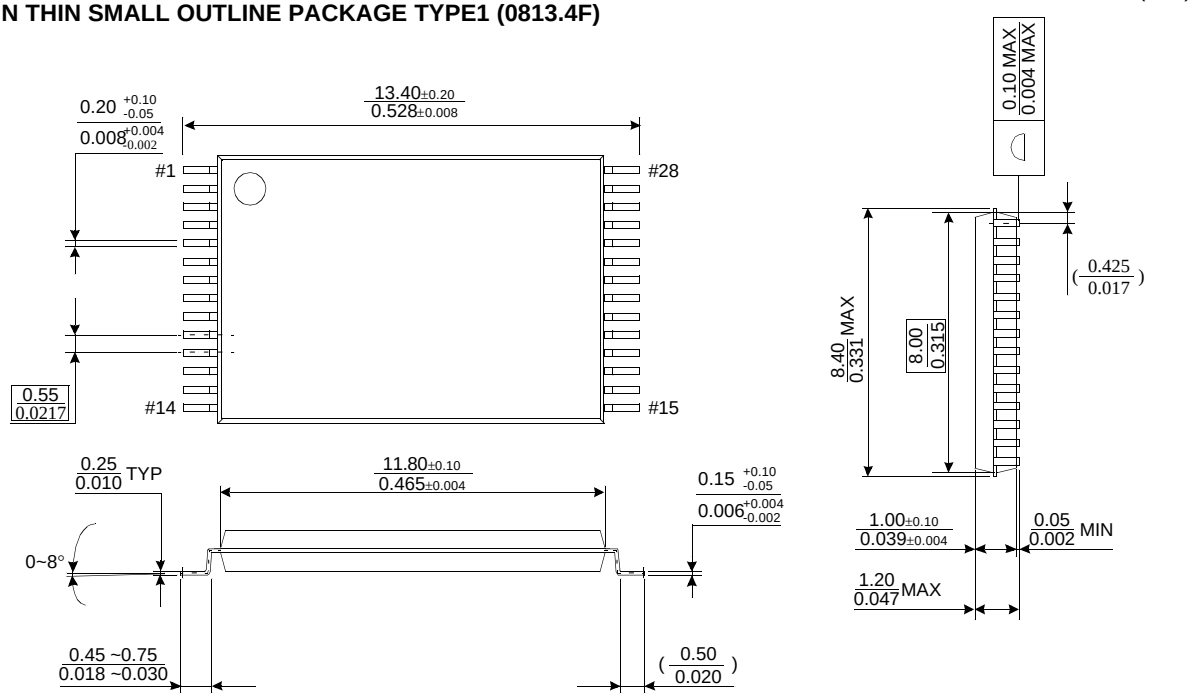
28 PIN PLASTIC SMALL OUTLINE PACKAGE(450mil)



PACKAGE DIMENSIONS

Units: millimeter(inch)

28 PIN THIN SMALL OUTLINE PACKAGE TYPE1 (0813.4F)



28 PIN THIN SMALL OUTLINE PACKAGE TYPE1 (0813.4R)