MICRON

MT5C6405 883C

MILITARY SRAM

16K x 4 SRAM

WITH OUTPUT ENABLE

T-46-23-10

FAST SRAM

AVAILABLE AS MILITARY SPECIFICATIONS

- SMD (consult factory for reference number)
- JAN (consult factory for reference number)
- RAD-tolerant (consult factory)

FEATURES

- High speed: 15, 20, 25, 30 and 35ns
- Battery backup – 2 volt data retention
- High performance, low power, CMOS double metal process
- Single +5V (±10%) power supply
- Easy memory expansion with $\overline{CE}$
- All inputs and outputs are TTL compatible
- MIL-STD 883 Rev. C, Class B

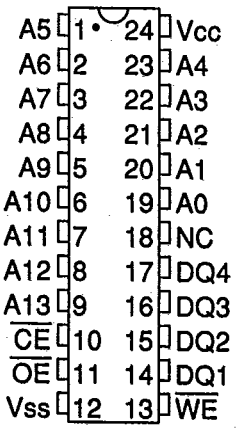
OPTIONS

	MARKING
• Timing	
15ns access	-15
20ns access	-20
25ns access	-25
30ns access	-30
35ns access	-35
45ns access	-45*
55ns access	-55*
70ns access	-70*
• Packages	
Ceramic DIP (300 mil)	C
Ceramic LCC (28 leads)	EC
• Two Volt Data Retention	L

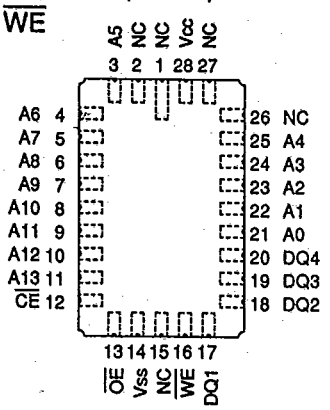
* Electrical characteristics identical to those provided for the 35ns access devices.

PIN ASSIGNMENT (Top View)

24L/300 DIP



28L/LCC (C-11A)



GENERAL DESCRIPTION

The Micron SRAM family employs high speed, low power CMOS designs using a 4-transistor memory cell. They are fabricated using double layer metal, double layer polysilicon technology. All fabrication is 100% domestic.

For flexibility in high speed memory applications, Micron offers chip enable ($\overline{CE}$) on all organizations. This enhancement can place the outputs in a high impedance state for additional flexibility in system design. The x 1 configuration features separate data input and output.

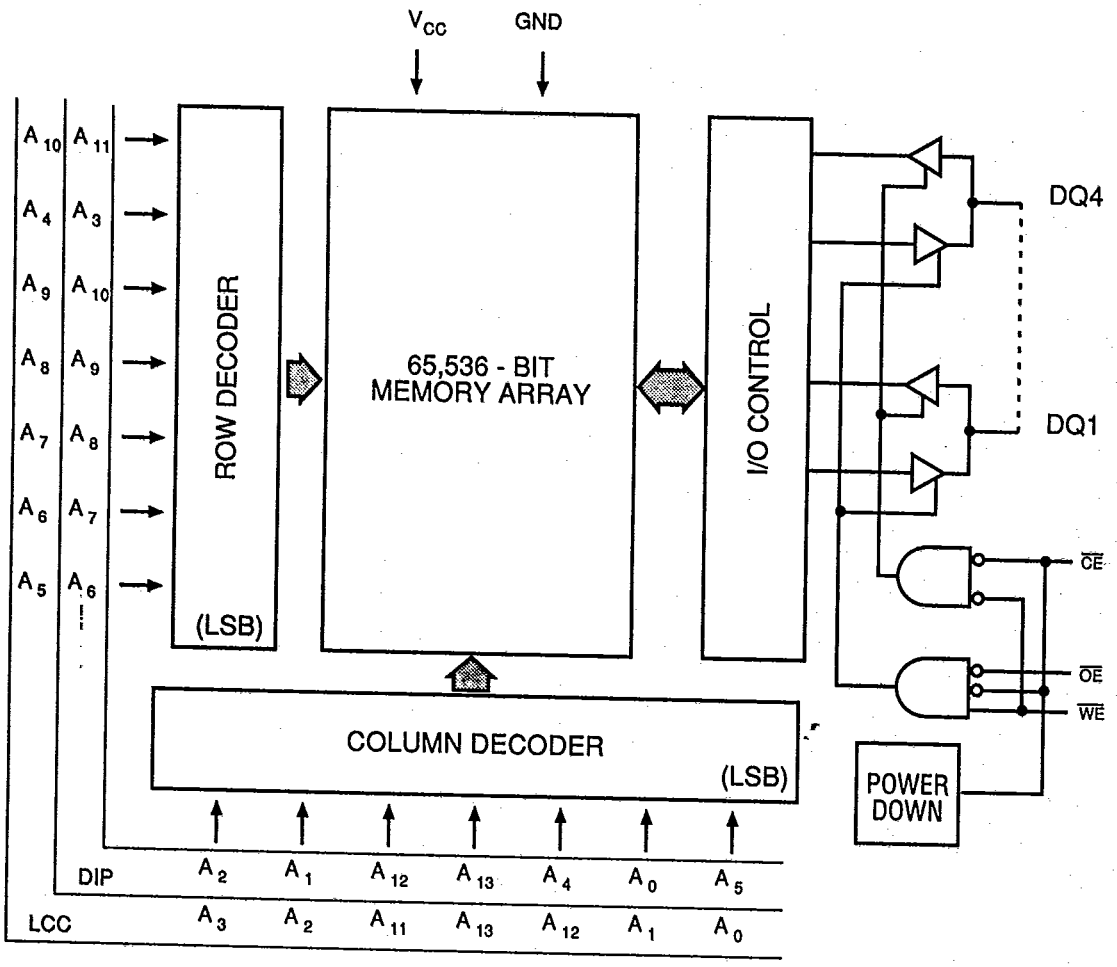
Writing to these devices is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ goes to LOW. The device offers a reduced power standby mode when disabled. This allows system designs to achieve low standby power requirements.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible.

Micron Technology, Inc. reserves the right to change products or specifications without notice.

FAST SRAM

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{OE}$	$\overline{CE}$	$\overline{WE}$	DQ	POWER
STANDBY	X	H	X	HIGH Z	STANDBY
READ	L	L	H	Q	ACTIVE
READ	H	L	H	HIGH Z	ACTIVE
WRITE	X	L	L	D	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on any input or DQ relative to Vss ..-2.0 to +7.0V
Voltage on Vcc supply relative to Vss .....-1.0V to +7.0V
Storage Temperature .....-65°C to +150°C
Power Dissipation .....1 Watt
Short Circuit Output Current 50mA
Lead Temperature (soldering, 10 seconds) .....+260°C
Junction Temperature .....+175°C

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($-55°C \le T_C \le 125°C$; $V_{CC} = 5V \pm 10\%$)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	6.0	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	I_{LI}	-10	10	µA	
Output Leakage Current	Outputs Disabled, $0V \le V_{OUT} \le V_{CC}$	I_{LO}	-10	10	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1

DESCRIPTION	CONDITIONS	SYMBOL	MAX -15	MAX -20	MAX -25	MAX -30	MAX -35	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE} \le V_{IL}$, V_{CC} = Max., Outputs Open	I_{CC}	130	120	110	100	90	mA	3
Power Supply Current: Standby	$\overline{CE} \ge V_{IH}$, V_{CC} = Max., $f = \frac{1}{T_{RC(MIN)}} = \frac{1}{T_{WC(MIN)}}$ Hz	I_{SBT1}	50	40	35	30	30	mA	
	$\overline{CE} \ge V_{IH}$, all other inputs $\le V_{IL}$ or $\ge V_{IH}$, V_{CC} = Max., f = 0Hz	I_{SBT2}	25	25	25	25	25	mA	
	$\overline{CE} \ge (V_{CC} - 0.2)$, V_{CC} = Max., all other inputs $\le 0.2V$ or $\ge (V_{CC} - 0.2V)$, f = 0Hz	I_{SBC2}	10	10	10	10	10	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C, f = 1MHz, V_{CC} = 5V	C_I		8	pF	4
Output Capacitance		C_O		8	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) (-55°C ≤ T_C ≤ 125°C; Vcc = 5V ± 10%)

DESCRIPTION		-15		-20		-25		-30		-35			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle													
READ cycle time	t_{RC}	15		20		25		30		35		ns	
Address access time	t_{AA}		15		20		25		30		35	ns	
Chip enable access time	t_{ACE}		15		20		25		30		35	ns	
Output hold from address change	t_{OH}	3		3		3		3		3		ns	
Chip enable to output in low Z	t_{LZCE}	3		3		3		3		3		ns	
Chip disable to output in high Z	t_{HZCE}		10		15		15		20		20	ns	6,7
Chip enable to power-up time	t_{PU}	0		0		0		0		0		ns	
Chip disable to power-down time	t_{PD}		15		20		25		30		35	ns	
Output enable access time	t_{AOE}		12		15		15		20		20	ns	
Output enable to output in low Z	t_{LZOE}	0		0		0		0		0		ns	
Output disable to output in high Z	t_{HZOE}		10		15		15		20		20	ns	6
WRITE Cycle													
WRITE cycle time	t_{WC}	15		20		25		30		35		ns	
Chip enable to end of write	t_{CW}	13		15		20		25		25		ns	
Address valid to end of write	t_{AW}	15		15		20		25		25		ns	
Address set-up time	t_{AS}	0		0		0		0		0		ns	
Address hold from end of write	t_{AH}	0		0		0		0		0		ns	
Write pulse width	t_{WP}	13		15		20		25		25		ns	
Data set-up time	t_{DS}	10		12		15		15		15		ns	
Data hold time	t_{DH}	0		0		0		0		0		ns	
Write disable to output in low Z	t_{LZWE}	0		0		0		0		0		ns	
Write enable to output in high Z	t_{HZWE}	0	10	0	12	0	15	0	15	0	15	ns	6

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	5ns
Input timing reference level	1.5V
Output reference level	1.5V
Output load	See figures 1 and 2

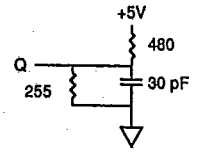


Fig. 1 OUTPUT LOAD EQUIVALENT

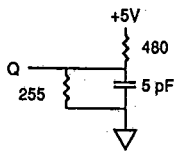


Fig. 2 OUTPUT LOAD EQUIVALENT

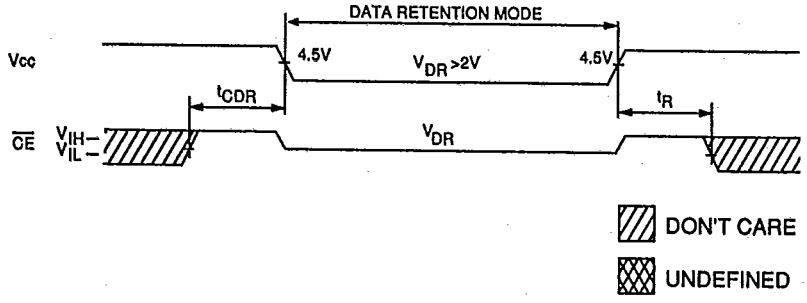
NOTES

1. All voltages referenced to Vss (GND).
2. -3.0V for pulse width < 20ns.
3. Icc is dependent on output loading and cycle rates. The specified value applies with the outputs unloaded, and $f = \frac{1}{T_{RC(MIN)}} = \frac{1}{T_{WC(MIN)}}$ = Hz.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^tHZCE and ^tHZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ± 500mV from steady state voltage, allowing for actual tester RC time constant.
7. At any given temperature and voltage condition, ^tHZCE is less than ^tLZCE.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables held in their active state.
10. Address valid prior to or coincident with latest occurring chip enable.
11. ^tRC = Read cycle time.

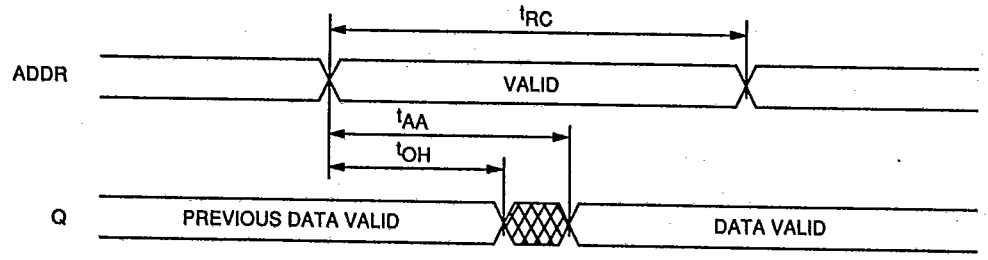
DATA RETENTION ELECTRICAL CHARACTERISTICS (L Version Only)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	MAX	UNIT	NOTES
Vcc for Retention Data			V_{DR}	2	—	V	
Data Retention Current	$\overline{CE} \geq$ (Vcc - 0.2V) $V_{IN} \geq$ (Vcc - 0.2V) or ≤ 0.2V	Vcc=2v	I_{CCDR}		300	µA	
		Vcc=3v			600	µA	
Chip Deselect to Data Retention Time			^tCDR	0	—	ns	4
Operation Recovery Time			^tR	^tRC		ns	4, 11

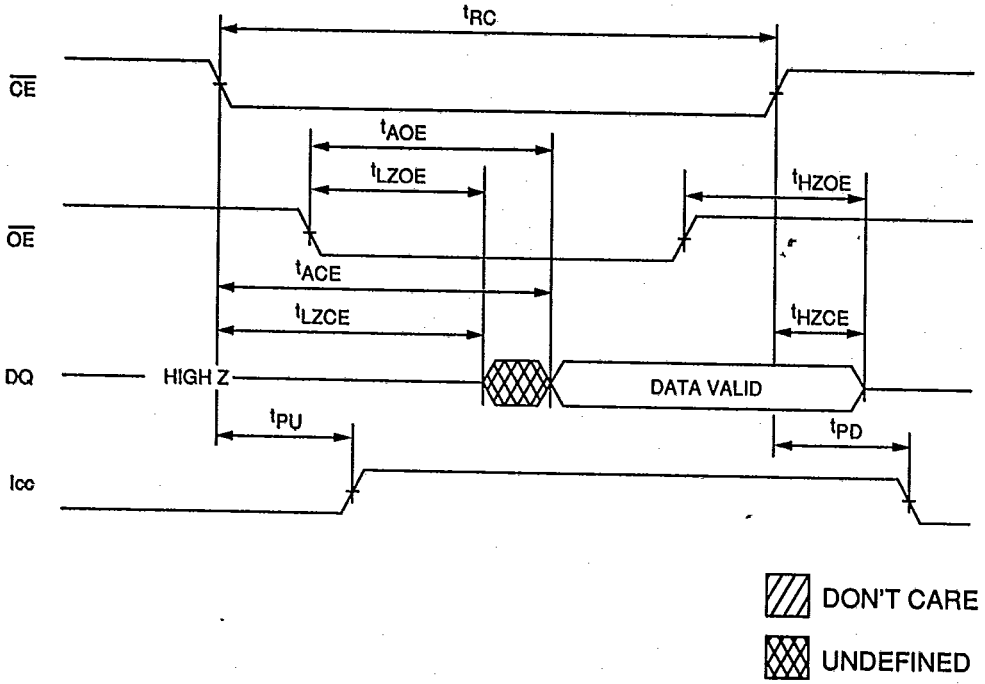
LOW Vcc DATA RETENTION WAVEFORM



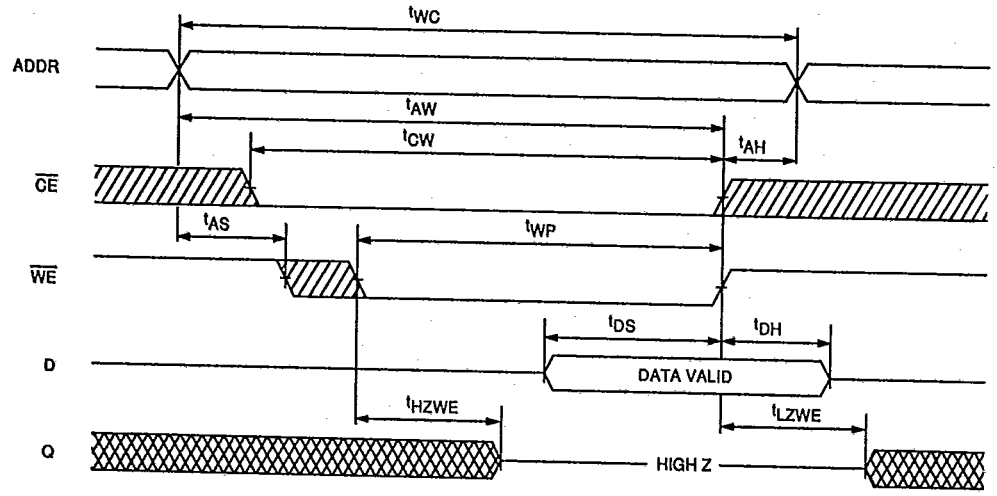
READ CYCLE NO. 1 (NOTES 8, 9)



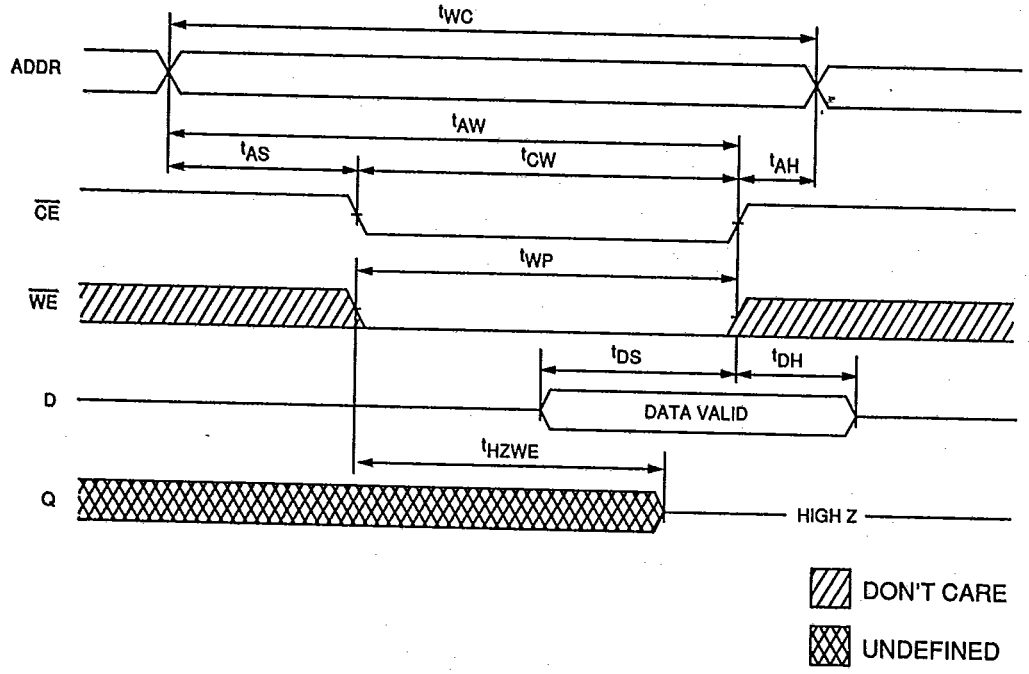
READ CYCLE NO. 2 (NOTES 7, 8, 10)



WRITE CYCLE NO. 1
(Write Enable Controlled)



WRITE CYCLE NO. 2
(Chip Enable Controlled)



ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (per method 5005, Table I)
FINAL ELECTRICAL TEST PARAMETERS (Method 5004)	1*, 2, 3, 7*, 8, 9, 10, 11
GROUP A TEST REQUIREMENTS (Method 5005)	1, 2, 3, 4**, 7, 8, 9, 10, 11
GROUP C AND D END-POINT ELECTRICAL PARAMETERS (Method 5005)	1, 2, 3, 7, 8

* PDA applies to subgroup 1 and 7.
** Subgroup 4 shall be measured only for initial qualification and after process or design changes which may affect input or output capacitance.

FACT CDAM