

MITSUBISHI LSIs
M5M51288BKP,KJ,J-15,-20,-25,-20L,-25L
M5M51288BVP-20,-25,-20L,-25L
 1048576-BIT(131072-WORD BY 8-BIT)CMOS STATIC RAM

DESCRIPTION

The M5M51288BKP,KJ,J,VP are a family of 131072-word by 8-bit static RAMs, fabricated with the high performance CMOS silicon gate process and designed for high-speed application.

The M5M51288BKP,KJ,J,VP are offered in a 32-pin plastic dual-in-line package(DIP), 32-pin plastic small outline J-lead package(SOJ), 32-pin thin small outline package (TSOP).

These devices operate on a single 5V supply, and are directly TTL compatible. They include power down feature as well.

FEATURES

Type name	Access time (max)	Power supply current	
		Active (max)	Stand-by (max)
M5M51288BKP,KJ,J - 15	15ns	190 mA	10mA
M5M51288BKP,KJ,J,VP - 20	20ns	170 mA	
M5M51288BKP,KJ,J,VP - 20L			100µA
M5M51288BKP,KJ,J,VP - 25	25ns	150 mA	10mA
M5M51288BKP,KJ,J,VP - 25L			100µA

- Single +5V power supply
- Fully static operation : No clocks, No refresh
- Common data I/O
- Easy memory expansion by \bar{S}_1, S_2
- Three-state outputs : OR-tie capability
- \bar{OE} prevents data contention in the I/O bus
- Directly TTL compatible : All inputs and outputs

PACKAGE

M5M51288BKP	32pin 300mil DIP
M5M51288BKJ	32pin 300mil SOJ
M5M51288BJ	32pin 400mil SOJ
M5M51288BVP	32pin 8X20mm ² TSOP(I)

APPLICATION

High speed memory units

FUNCTION

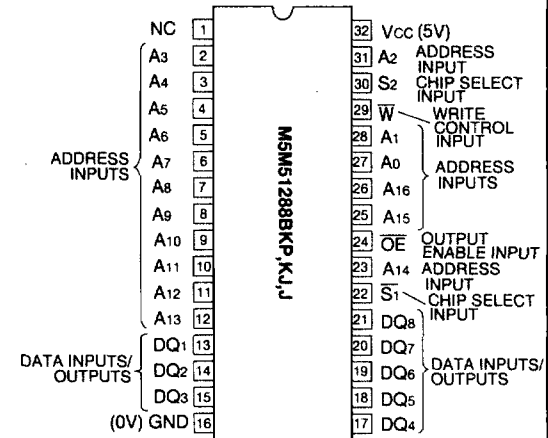
The operation mode of the M5M51288B series is determined by a combination of the device control inputs \bar{S}_1, S_2, \bar{W} and \bar{OE} . Each mode is summarized in the function table shown in next page.

A write cycle is executed whenever the low level \bar{W} overlaps with the low level \bar{S}_1 and the high level S_2 . The address must be set up before the write cycle and must be stable during the entire cycle. The data is latched into a cell on the trailing edge of \bar{W} , \bar{S}_1 or S_2 , whichever occurs first, requiring the set-up and hold time relative to these edge to be maintained. The output enable input \bar{OE} directly controls the output stage. Setting the \bar{OE} at a high level, the output stage is in a high-impedance state, and the data bus contention problem in the write cycle is eliminated.

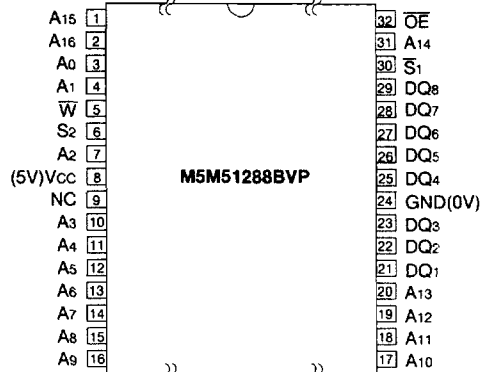
FUNCTION TABLE

\bar{S}_1	S_2	\bar{W}	\bar{OE}	Mode	DQ	I _{cc}
X	L	X	X	Non selection	High-impedance	Active
H	X	X	X	Non selection	High-impedance	Stand-by
L	H	L	X	Write	Din	Active
L	H	H	L	Read	Dout	Active
L	H	H	H		High-impedance	Active

PIN CONFIGURATION (TOP VIEW)



Outline 32P4Y(KP)
 32P0J(KJ)
 32P0K(J)



Outline 32P3H-E

NC : NO CONNECTION

A read cycle is executed by setting \bar{W} at a high level and \bar{OE} at a low level while \bar{S}_1 and S_2 are in an active state ($\bar{S}_1=L, S_2=H$)

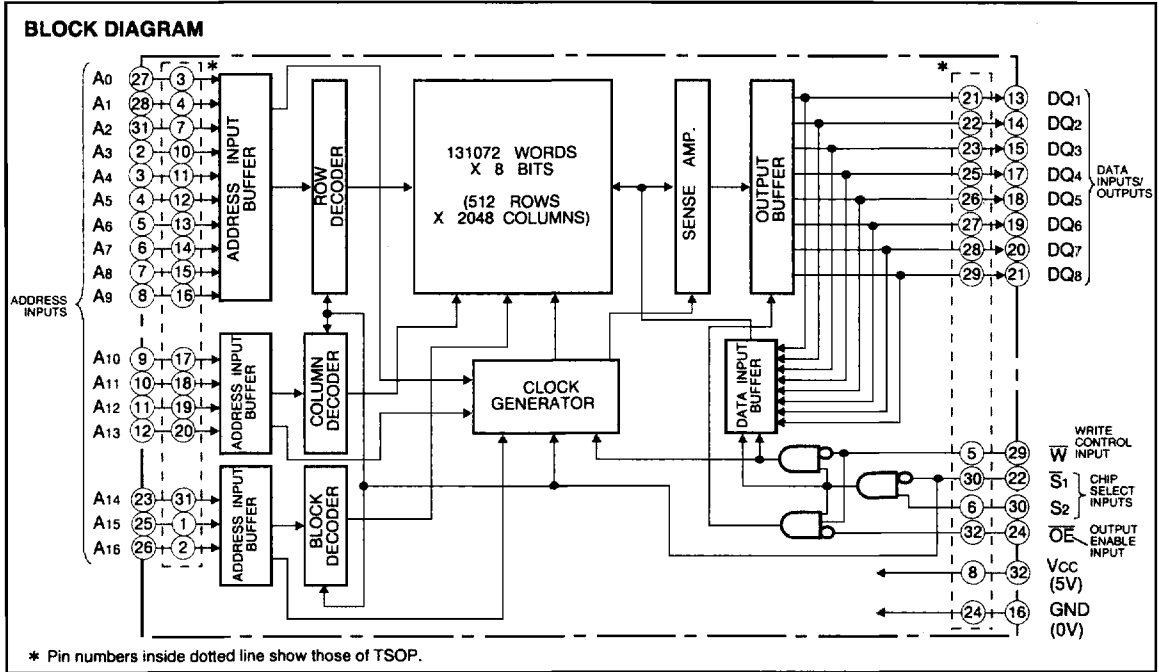
When setting \bar{S}_1 at a high level or S_2 at a low level, the chip is in a non-selectable mode in which both reading and writing are disabled. In this mode, the output stage is in a high-impedance state, allowing OR-tie with other chips and memory expansion by \bar{S}_1 and S_2 .

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ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V _{CC}	Supply voltage	With respect to GND	-3.5*~7	V
V _I	Input voltage		-3.5*~V _{CC} +0.3	V
V _O	Output voltage		-3.5*~V _{CC} +0.3	V
P _d	Power dissipation	T _a =25°C	1000	mW
T _{opr}	Operating temperature		0~70	°C
T _{stg(bias)}	Storage temperature(bias)		-10~85	°C
T _{stg}	Storage temperature		-65~150	°C

*Pulse width ≤ 20ns, in case of DC: - 0.5V

DC ELECTRICAL CHARACTERISTICS (T_a=0~70°C, V_{CC}=5V±10%, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V _{IH}	High-level input voltage		2.2		V _{CC} +0.3V	V
V _{IL}	Low-level input voltage		-0.3*		0.8	V
V _{OH}	High-level output voltage	I _{OH} =-4mA	2.4			V
V _{OL}	Low-level output voltage	I _{OL} =8mA			0.4	V
I _I	Input current	V _I =0~V _{CC}			2	μA
I _{oz}	Output current in off-state	V _I (\bar{S})=V _{IH} V _{I/O} =0~V _{CC}			10	μA
I _{CC1}	Active supply current (TTL level)	V _I (\bar{S})=V _{IL} other inputs=V _{IH} or V _{IL} Output-open(duty 100%)	AC (15ns cycle)		190	mA
			AC (20ns cycle)		170	
			AC (25ns cycle)		150	
			DC	70	85	
I _{CC2}	Stand-by supply current (TTL level)	V _I (\bar{S})=V _{IH}	AC (15ns cycle)		60	mA
			AC (20/25ns cycle)		50	
			DC		35	
I _{CC3}	Stand-by current (MOS level)	V _I (\bar{S}) ≥ V _{CC} -0.2V other inputs V _I ≤ 0.2V or V _I ≥ V _{CC} -0.2V	-15, -20, -25	1	10	mA
			-20L, -25L	10	100	μA

*Pulse width ≤ 20ns, in case of AC: - 3.0V

CAPACITANCE (T_a=0~70°C, V_{CC}=5V±10%, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
C _I	Input capacitance	V _I =GND, V _I =25mVrms, f=1MHz			6	pF
C _O	Output capacitance	V _O =GND, V _O =25mVrms, f=1MHz			6	pF

Note 1: Direction for current flowing into an IC is positive (no mark).

2: Typical value is V_{CC}=5V, T_a=25°C

3: C_I, C_O are periodically sampled and are not 100% tested.

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AC ELECTRICAL CHARACTERISTICS (Ta = 0 ~ 70°C, Vcc=5V±10%, unless otherwise noted)

(1) MEASUREMENT CONDITIONS

Input pulse levels V_{IH} = 3.0V, V_{IL} = 0V
 Input rise and fall time 3ns
 Input timing reference levels V_{IH} = 1.5V, V_{IL} = 1.5V
 Output timing reference levels V_{OH} = 1.5V, V_{OL} = 1.5V
 Output loads Fig1, Fig2

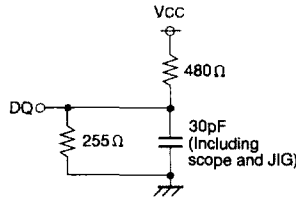


Fig.1 Output load

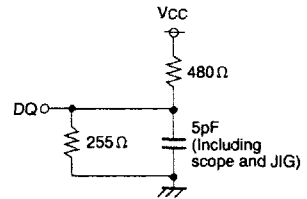


Fig.2 Output load for ten, tdis

(2) READ CYCLE

Symbol	Parameter	Limits						Unit
		M5M51288BKP,KJ,J -15		M5M51288BKP,KJ,J, VP-20,-20L		M5M51288BKP,KJ,J, VP-25,-25L		
		Min	Max	Min	Max	Min	Max	
t _{CR}	Read cycle time	15		20		25		ns
t _{a(A)}	Address access time		15		20		25	ns
t _{a(S1)}	Chip select 1 access time		15		20		25	ns
t _{a(S2)}	Chip select 2 access time		14		17		20	ns
t _{a(OE)}	Output enable access time		8		10		13	ns
t _{dis(S1)}	Output disable time after $\overline{S1}$ high	0	7	0	7	0	8	ns
t _{dis(S2)}	Output disable time after $\overline{S2}$ low	0	7	0	7	0	8	ns
t _{dis(OE)}	Output disable time after \overline{OE} high	0	7	0	7	0	8	ns
t _{en(S1)}	Output enable time after $\overline{S1}$ low	6		6		6		ns
t _{en(S2)}	Output enable time after $\overline{S2}$ high	6		6		6		ns
t _{en(OE)}	Output enable time after \overline{OE} low	0		0		0		ns
t _{v(A)}	Data valid time after address change	7		7		7		ns
t _{PU}	Power-up time after chip selection	0		0		0		ns
t _{PD}	Power-down time after chip selection		15		20		25	ns

(3) WRITE CYCLE

Symbol	Parameter	Limits						Unit
		M5M51288BKP,KJ,J -15		M5M51288BKP,KJ,J, VP-20,-20L		M5M51288BKP,KJ,J, VP-25,-25L		
		Min	Max	Min	Max	Min	Max	
t _{CW}	Write cycle time	15		20		25		ns
t _{w(W)}	Write pulse width	12		15		20		ns
t _{su(A)1}	Address setup time (\overline{W})	0		0		0		ns
t _{su(A)2}	Address setup time ($\overline{S1}$, $\overline{S2}$)	0		0		0		ns
t _{su(S1)}	Chip select 1 setup time	12		15		20		ns
t _{su(S2)}	Chip select 2 setup time	12		15		20		ns
t _{su(D)}	Data setup time	8		12		15		ns
t _{h(D)}	Data hold time	0		0		0		ns
t _{rec(W)}	Write recovery time	0		0		0		ns
t _{dis(W)}	Output disable time after \overline{W} low	0	7	0	7	0	8	ns
t _{dis(OE)}	Output disable time after \overline{OE} high	0	7	0	7	0	8	ns
t _{en(W)}	Output enable time after \overline{W} high	0		0		0		ns
t _{en(OE)}	Output enable time after \overline{OE} low	0		0		0		ns
t _{su(A-\overline{WH})}	Address to \overline{W} high	12		15		20		ns

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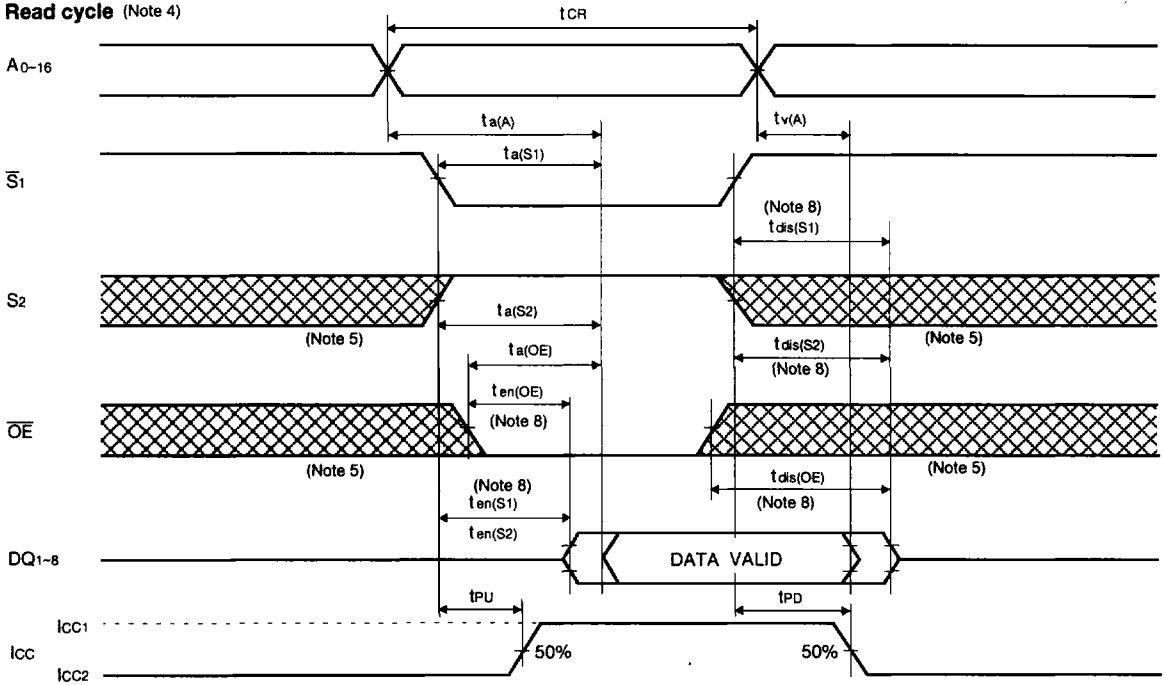
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(4) TIMING DIAGRAMS

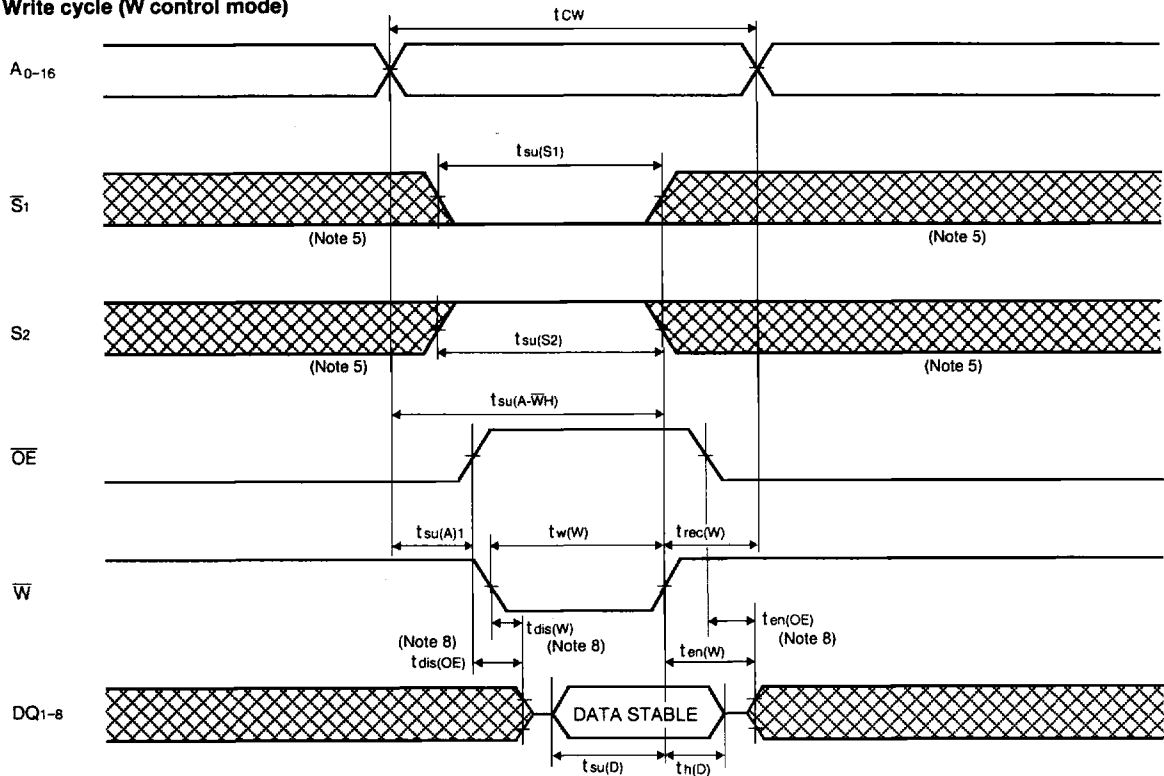
Read cycle (Note 4)



$\bar{W} = H$

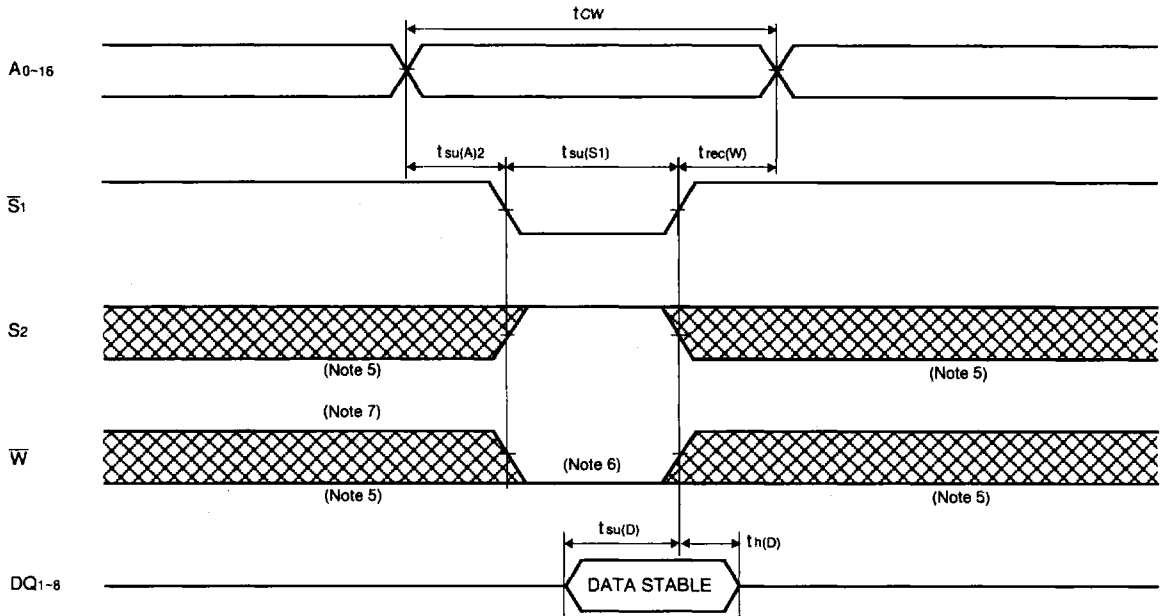
Note 4: Addresses and $\bar{S}1, S2$ valid prior to \bar{OE} transition low by $(tA(A) - tA(OE))$, $(tA(S1) - tA(OE))$, $tA(S2) - tA(OE)$.

Write cycle (\bar{W} control mode)

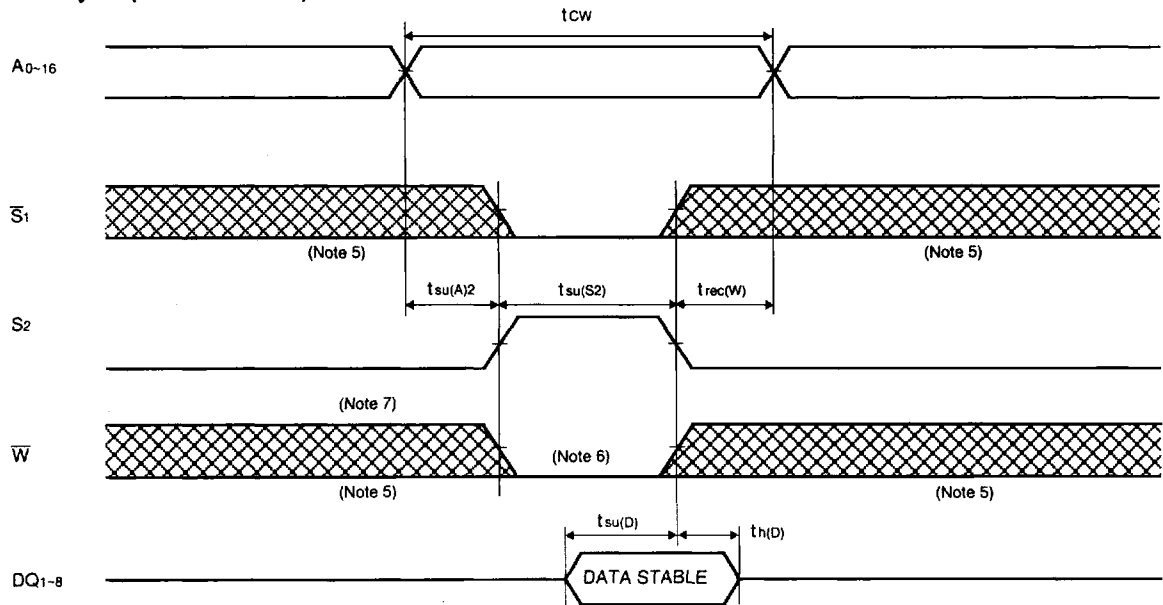


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Write cycle (\bar{S}_1 control mode)



Write cycle (S_2 control mode)



Note 5: Hatching indicates the state is "don't care".

6: Writing is executed while S_2 high overlaps \bar{S}_1 and \bar{W} low.

7: When the falling edge of \bar{W} is simultaneously or prior to the falling edge of \bar{S}_1 or rising edge of S_2 , the outputs are maintained in the high impedance state.

8: Transition is measured $\pm 500mV$ from steady state voltage with specified loading in Figure 2.

9: t_{en} , t_{is} are periodically sampled and are not 100% tested.

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POWER DOWN CHARACTERISTICS (Ta = 0~70°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V _{CC} (PD)	Power down supply voltage	V _I (\bar{S} ₁) ≥ V _{CC} - 0.2V V _I ≥ V _{CC} - 0.2V or 0V ≤ V _I ≤ 0.2V	2			V
V _I (\bar{S} ₁)	Chip select input voltage		V _{CC} - 0.2			V
t _{su} (PD)	Power down setup time		0			ns
t _{rec} (PD)	Power down recovery time		-20L	20		ns
			-25L	25		
I _{CC} (PD)	Power down supply current	V _{CC} = 3.0V			50	μA
		V _{CC} = 5.5V			100	

Note 10 : This is only M5M51288BKP, KJ, J, VP-20L, -25L

TIMING WAVEFORM FOR POWER DOWN

