

AC821 • ACT821 • AC822 • ACT822

54AC/74AC821 • 54ACT/74ACT821 54AC/74AC822 • 54ACT/74ACT822

10-Bit D-Type Flip-Flop

Description

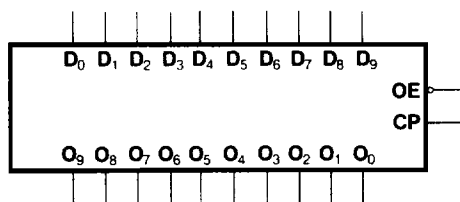
The 'AC/'ACT821 and 'AC/'ACT822 are 10-bit D-type flip-flops with 3-state outputs arranged in a broadside pinout.

The 'AC/'ACT821 and 'AC/'ACT822 are functionally identical to the AM29821 and AM29822.

- 3-State Outputs for Bus Interfacing
- Inverting ('822) or Noninverting ('821) Outputs
- Outputs Source/Sink 24 mA
- 'ACT821 and 'ACT822 have TTL-Compatible Inputs

Ordering Code: See Section 6

Logic Symbol ('AC/'ACT821)*

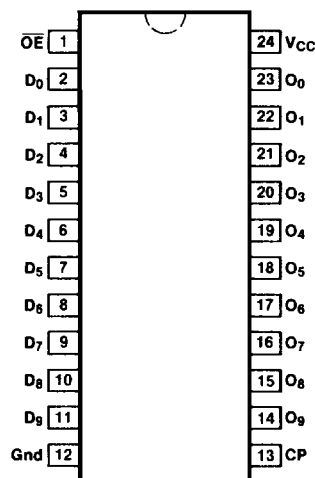


*The 'AC/'ACT822 has inverting outputs.

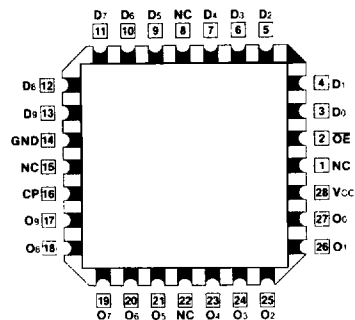
Pin Names

- D₀ - D₉ Data Inputs
- O₀ - O₉ Data Outputs ('AC/'ACT821)
- \bar{O}_0 - \bar{O}_9 Data Outputs ('AC/'ACT822)
- OE Output Enable
- CP Clock Input

Connection Diagrams



**Pin Assignment
for DIP, Flatpak and SOIC**



**Pin Assignment
for LCC**

Functional Description

The 'AC/'ACT821 and 'AC/'ACT822 consist of ten D-type edge-triggered flip-flops. The buffered Clock (CP) and buffered Output Enable (\overline{OE}) are common to all flip-flops. The flip-flops will store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH CP transition. With \overline{OE} LOW the contents of the flip-flops are available at the outputs. When \overline{OE} is

HIGH the outputs go to the high impedance state. Operation of the \overline{OE} input does not affect the state of the flip-flops.

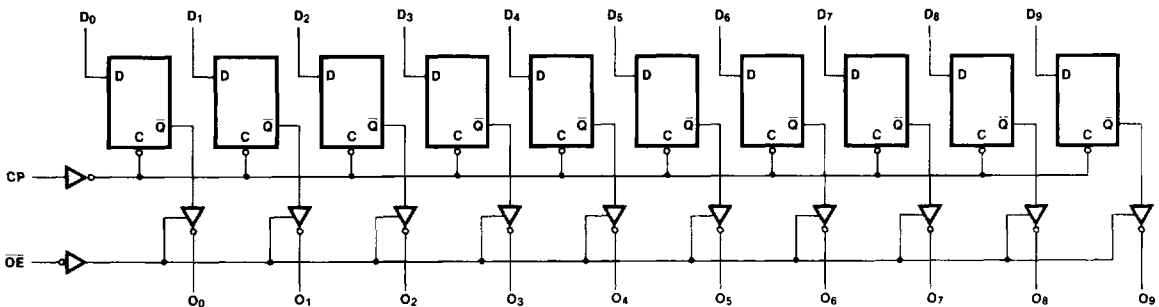
The 'AC/'ACT821 and 'AC/'ACT822 are functionally and pin compatible with the AM29821 and AM29822.

Function Table

Inputs			Internal	Outputs		Function
\overline{OE}	CP	D	Q	O ('821)	\overline{O} ('822)	
H	\uparrow	L	L	Z	Z	High Z
H	\uparrow	H	H	Z	Z	High Z
L	\uparrow	L	L	L	H	Load
L	\uparrow	H	H	H	L	Load

H = HIGH Voltage Level
 L = LOW Voltage Level
 Z = High Impedance
 \uparrow = LOW-to-HIGH Clock Transition

Logic Diagram ('AC/'ACT821)



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays. The 'AC/'ACT822 also has the same logic diagram with inverting outputs.

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DC Characteristics (unless otherwise specified)

Symbol	Parameter	54AC/ACT	74AC/ACT	Units	Conditions
I _{CC}	Maximum Quiescent Supply Current	160	80	μA	V _{IN} = V _{CC} or Ground, V _{CC} = 5.5 V, T _A = Worst Case
I _{CC}	Maximum Quiescent Supply Current	8.0	8.0	μA	V _{IN} = V _{CC} or Ground, V _{CC} = 5.5 V, T _A = 25°C
I _{CC(T)}	Maximum Additional I _{CC} /Input (*ACT821/822)	1.6	1.5	mA	V _{IN} = V _{CC} - 2.1 V, V _{CC} = 5.5 V, T _A = Worst Case

AC Characteristics

Symbol	Parameter	V _{CC} * (V)	74AC			54AC		74AC		Units	Fig. No.
			T _A = +25°C C _L = 50 pF			T _A = -55°C to +125°C C _L = 50 pF		T _A = -40°C to +85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max	Min	Max		
f _{max}	Maximum Clock Frequency	3.3 5.0	100 125						MHz	3-3	
t _{PLH}	Propagation Delay CP to O _n	3.3 5.0	9.5 6.6						ns	3-6	
t _{PHL}	Propagation Delay CP to O _n	3.3 5.0	9.5 6.6						ns	3-6	
t _{PZH}	Output Enable Time OE to O _n	3.3 5.0	7.5 5.5						ns	3-7	
t _{PZL}	Output Enable Time OE to O _n	3.3 5.0	8.0 6.0						ns	3-8	
t _{PHZ}	Output Disable Time OE to O _n	3.3 5.0	10.5 7.5						ns	3-7	
t _{PLZ}	Output Disable Time OE to O _n	3.3 5.0	9.0 6.5						ns	3-8	

*Voltage Range 3.3 is 3.3 V ± 0.3 V

Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

AC Operating Requirements

Symbol	Parameter	Vcc* (V)	74AC		54AC		74AC		Units	Fig. No.
			TA = +25°C CL = 50 pF		TA = -55°C to +125°C CL = 50 pF		TA = -40°C to +85°C CL = 50 pF			
			Typ	Guaranteed Minimum						
ts	Setup Time, HIGH or LOW Dn to CP	3.3 5.0	3.0 2.0						ns	3-9
th	Hold Time, HIGH or LOW Dn to CP	3.3 5.0	2.0 1.5						ns	3-9
tw	CP Pulse Width HIGH or LOW	3.3 5.0	3.5 2.5						ns	3-6

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

AC Characteristics

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Symbol	Parameter	Vcc* (V)	74ACT			54ACT		74ACT		Units	Fig. No.
			TA = +25°C CL = 50 pF			TA = -55°C to +125°C CL = 50 pF		TA = -40°C to +85°C CL = 50 pF			
			Min	Typ	Max	Min	Max	Min	Max		
fmax	Maximum Clock Frequency	5.0	120	110			110		MHz	3-3	
tPLH	Propagation Delay CP to On	5.0	1.0	8.0	9.5			1.0 10.5	ns	3-6	
tPHL	Propagation Delay CP to On	5.0	1.0	8.0	9.5			1.0 10.5	ns	3-6	
tpZH	Output Enable Time OE to On	5.0	1.0	7.0	10.5			1.0 11.5	ns	3-7	
tpZL	Output Enable Time OE to On	5.0	1.0	7.5	10.5			1.0 12.0	ns	3-8	
tPHZ	Output Disable Time OE to On	5.0	1.0	10.0	12.0			1.0 13.0	ns	3-7	
tPLZ	Output Disable Time OE to On	5.0	1.0	9.5	10.5			1.0 11.5	ns	3-8	

*Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

AC Operating Requirements

Symbol	Parameter	Vcc* (V)	74ACT		54ACT	74ACT		Units	Fig. No.
			TA = +25°C CL = 50 pF		TA = -55°C to +125°C CL = 50 pF	TA = -40°C to +85°C CL = 50 pF			
			Typ	Guaranteed Minimum					
ts	Setup Time, HIGH or LOW Dn to CP	5.0	2.0	2.0			2.5	ns	3-9
th	Hold Time, HIGH or LOW Dn to CP	5.0	-0.5	2.0			2.5	ns	3-9
tw	CP Pulse Width HIGH or LOW	5.0	3.0	4.5			5.5	ns	3-6

*Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

Capacitance

Symbol	Parameter	54/74AC/ACT	Units	Conditions
		Typ		
CIN	Input Capacitance	4.5	pF	Vcc = 5.5 V
CPD	Power Dissipation Capacitance	35.0	pF	Vcc = 5.5 V