ICS840021I

FEMTOCLOCKS™ CRYSTAL-TO-LVCMOS/LVTTL CLOCK GENERATOR

GENERAL DESCRIPTION

The ICS840021I is a Gigabit Ethernet Clock Generator and a member of the HiPerClocks™ family of high performance devices from ICS. The ICS840021I uses a 25MHz crystal to synthesize 125MHz. The ICS840021I has excellent phase jitter performance, over the 1.875MHz – 20MHz integration range. The ICS840021I is packaged in a small 8-pin TSSOP, making it ideal for use in systems with limited board space.

FEATURES

- 1 LVCMOS/LVTTL output, 15Ω output impedence

- Crystal oscillator interface designed for 25MHz, 18pF parallel resonant crystal

- Output frequency: 125MHz

- VCO range: 560MHz to 680MHz

- RMS phase jitter @ 125MHz, using a 25MHz crystal (1.875MHz - 20MHz): 0.48ps (typical) (3.3V)
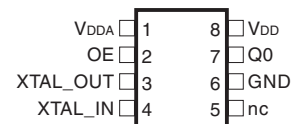
Offset	Noise Power
100Hz	-97.8 dBc/Hz
1kHz	-124.6 dBc/Hz
10kHz	-132.5 dBc/Hz
100kHz	-131.1 dBc/Hz

- Voltage supply modes:
  V_{DD}/V_{DDA} = 3.3V
  V_{DD}/V_{DDA} = 2.5V

- -40°C to 85°C ambient operating temperature

- Lead-Free package fully RoHS compliant

BLOCK DIAGRAM
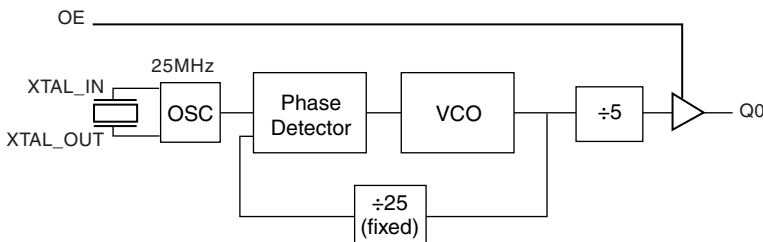
PIN ASSIGNMENT

ICS840021I

8-Lead TSSOP
4.40mm x 3.0mm x 0.925mm package body
G Package
Top View

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1	V_{DDA}	Power		Analog supply pin.
2	OE	Input	Pullup	Output enable pin. When HIGH, Q0 output is enabled. When LOW, forces Q0 to HiZ state. LVCMOS/LVTTL interface levels.
3, 4	XTAL_OUT, XTAL_IN	Input		Crystal oscillator interface. XTAL_IN is the input, XTAL_OUT is the output.
5	nc	Unused		No connect.
6	GND	Power		Power supply ground.
7	Q0	Output		Single-ended clock output. LVCMOS/LVTTL interface levels. 15Ω output impedence.
8	V_{DD}	Power		Core supply pin.

NOTE: *Pullup* refers to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
C_{PD}	Power Dissipation Capacitance	V_{DD}, V_{DDA} = 3.465V		7		pF
		V_{DD}, V_{DDA} = 2.625V		7		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
R_{OUT}	Output Impedance			15		Ω

TABLE 3. CONTROL FUNCTION TABLE

Control Inputs	Output
OE	Q0
0	Hi-Z
1	Active

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5 V
Outputs, V_O	-0.5V to V_{DD} + 0.5V
Package Thermal Impedance, θ_{JA}	101.7°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 4A. POWER SUPPLY DC CHARACTERISTICS, $V_{DD} = V_{DDA} = 3.3V \pm 5\%$, T_A = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current				65	mA
I_{DDA}	Analog Supply Current				10	mA

TABLE 4B. POWER SUPPLY DC CHARACTERISTICS, $V_{DD} = V_{DDA} = 2.5V \pm 5\%$, T_A = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		2.375	2.5	2.625	V
V_{DDA}	Analog Supply Voltage		2.375	2.5	2.625	V
I_{DD}	Power Supply Current				60	mA
I_{DDA}	Analog Supply Current				10	mA

TABLE 4C. LVCMOS/LVTTL DC CHARACTERISTICS, $V_{DD} = V_{DDA} = 3.3V \pm 5\%$ OR $2.5V \pm 5\%$, T_A = -40°C TO 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		V_{DD} = 3.3V	2		V_{DD} + 0.3	V
			V_{DD} = 2.5V	1.7		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage		V_{DD} = 3.3V	-0.3		0.8	V
			V_{DD} = 2.5V	-0.3		0.7	V
I_{IH}	Input High Current	OE	$V_{DD} = V_{IN}$ = 3.465V or 2.625V			5	µA
I_{IL}	Input Low Current	OE	V_{DD} = 3.465V or 2.625V, V_{IN} = 0V	-150			µA
V_{OH}	Output High Voltage; NOTE 1		V_{DD} = 3.465V	2.6			V
			V_{DD} = 2.625V	1.8			V
V_{OL}	Output Low Voltage; NOTE 1		V_{DD} = 3.465V or 2.625V			0.5	V

NOTE 1: Outputs terminated with 50Ω to V_{DD}/2. See Parameter Measurement Information Section, "Output Load Test Circuit" diagrams.

TABLE 5. CRYSTAL CHARACTERISTICS

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency			25		MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF
Drive Level				1	mW

TABLE 6A. AC CHARACTERISTICS, V_{DD} = V_{DDA} = 3.3V±5%, T_A = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency			125		MHz
$tjit(\emptyset)$	RMS Phase Jitter (Random); NOTE 1	Integration Range: 1.875MHz to 20MHz		0.48		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	200		500	ps
odc	Output Duty Cycle		48		52	%

NOTE 1: Please refer to the Phase Noise Plot.

TABLE 6A. AC CHARACTERISTICS, V_{DD} = V_{DDA} = 2.5V±5%, T_A = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency			125		MHz
$tjit(\emptyset)$	RMS Phase Jitter (Random); NOTE 1	Integration Range: 1.875MHz to 20MHz		0.50		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	250		550	ps
odc	Output Duty Cycle		48		52	%

NOTE 1: Please refer to the Phase Noise Plot.

TYPICAL PHASE NOISE AT 125MHz (3.3V OR 2.5V)

Gigabit Ethernet Filter

125MHz
RMS Phase Jitter (Random)
1.875MHz to 20MHz (3.3V) = 0.48ps (typical)
1.875MHz to 20MHz (2.5V) = 0.50ps (typical)

Raw Phase Noise Data

Phase Noise Result by adding
Gigabit Ethernet Filter to raw data
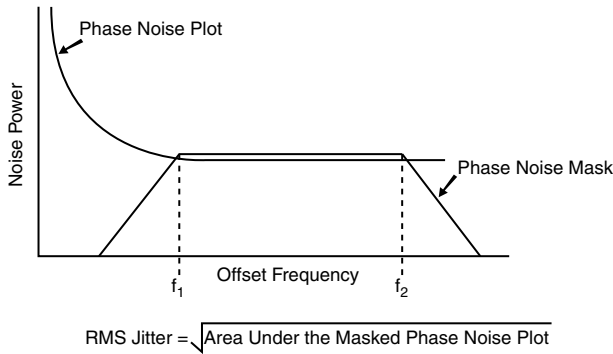
NOISE POWER $\frac{dBc}{Hz}$

OFFSET FREQUENCY (Hz)
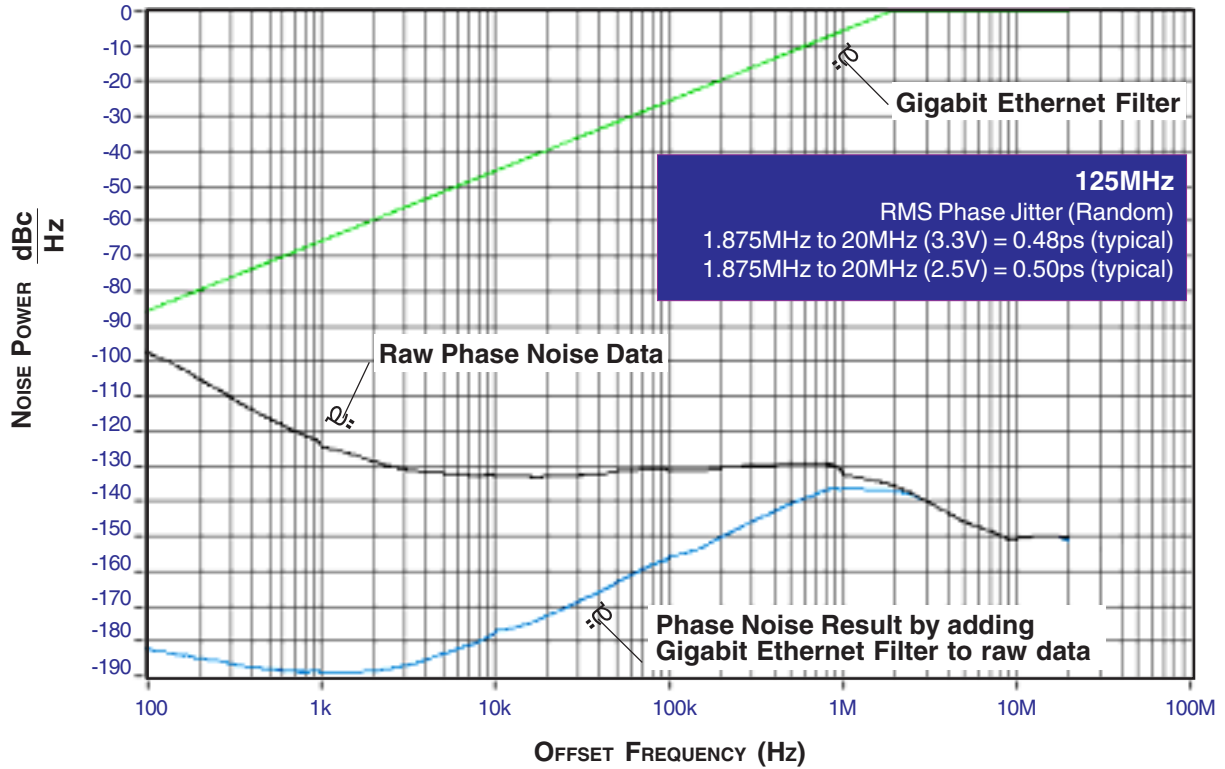
PARAMETER MEASUREMENT INFORMATION
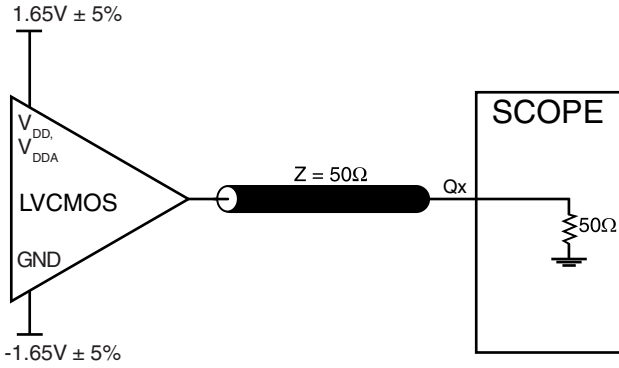
3.3V OUTPUT LOAD AC TEST CIRCUIT


2.5V OUTPUT LOAD AC TEST CIRCUIT
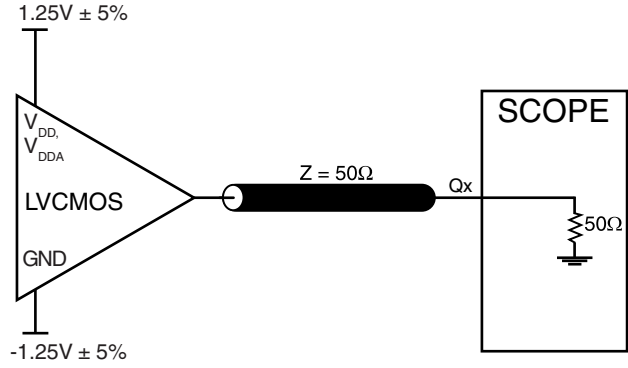
$$RMS\ Jitter = \sqrt{Area\ Under\ the\ Masked\ Phase\ Noise\ Plot}$$

RMS PHASE JITTER
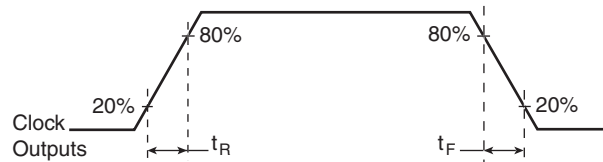
OUTPUT RISE/FALL TIME
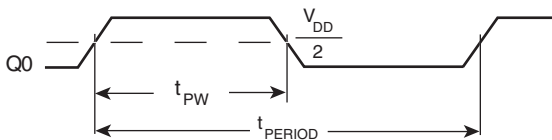
$$odc = \frac{t_{PW}}{t_{PERIOD}} \times 100\%$$

OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD

Aᴘᴘʟɪᴄᴀᴛɪᴏɴ Iɴꜰᴏʀᴍᴀᴛɪᴏɴ

Pᴏᴡᴇʀ Sᴜᴘᴘʟʏ Fɪʟᴛᴇʀɪɴɢ TᴇᴄʜɴɪQᴜᴇꜱ

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The ICS840021I provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{DD} and V_{DDA} should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, power supply isolation is required. *Figure 1* illustrates how a 10Ω resistor along with a 10µF and a .01µF bypass capacitor should be connected to each V_{DDA} pin.

Fɪɢᴜʀᴇ 1. Pᴏᴡᴇʀ Sᴜᴘᴘʟʏ Fɪʟᴛᴇʀɪɴɢ

Cʀʏꜱᴛᴀʟ Iɴᴘᴜᴛ Iɴᴛᴇʀꜰᴀᴄᴇ
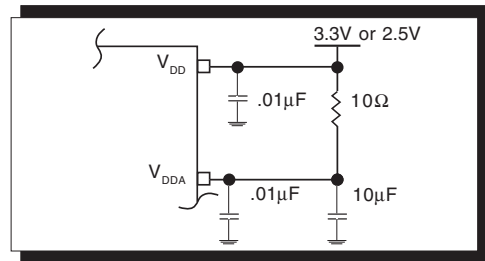
The ICS840021I has been characterized with 18pF parallel resonant crystals. The capacitor values, C1 and C2, shown in *Figure 2* below were determined using a 25MHz, 18pF parallel resonant crystal and were chosen to minimize the ppm error. The optimum C1 and C2 values can be slightly adjusted for different board layouts.

Figure 2. Cʀʏꜱᴛᴀʟ Iɴᴘᴜᴛ Iɴᴛᴇʀꜰᴀᴄᴇ
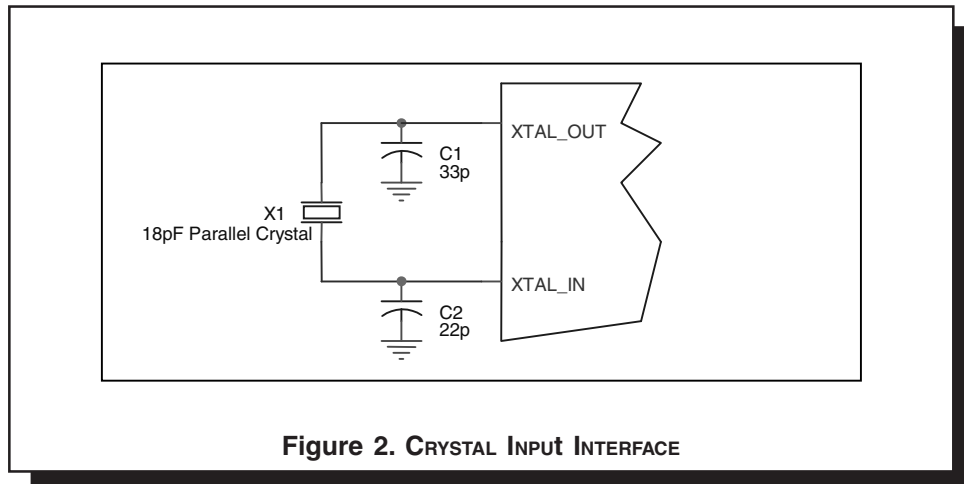
APPLICATION SCHEMATIC

Figure 3A shows a schematic example of the ICS840021I. An example of LVCMOS termination is shown in this schematic. Additional LVCMOS termination approaches are shown in the LVCMOS Termination Application Note. In this example, an 18pF parallel resonant 25MHz crystal is used for generating 125MHz

output frequency. The C1 = 22pF and C2 = 33pF are recommended for frequency accuracy. For different board layout, the C1 and C2 values may be slightly adjusted for optimizing frequency accuracy.
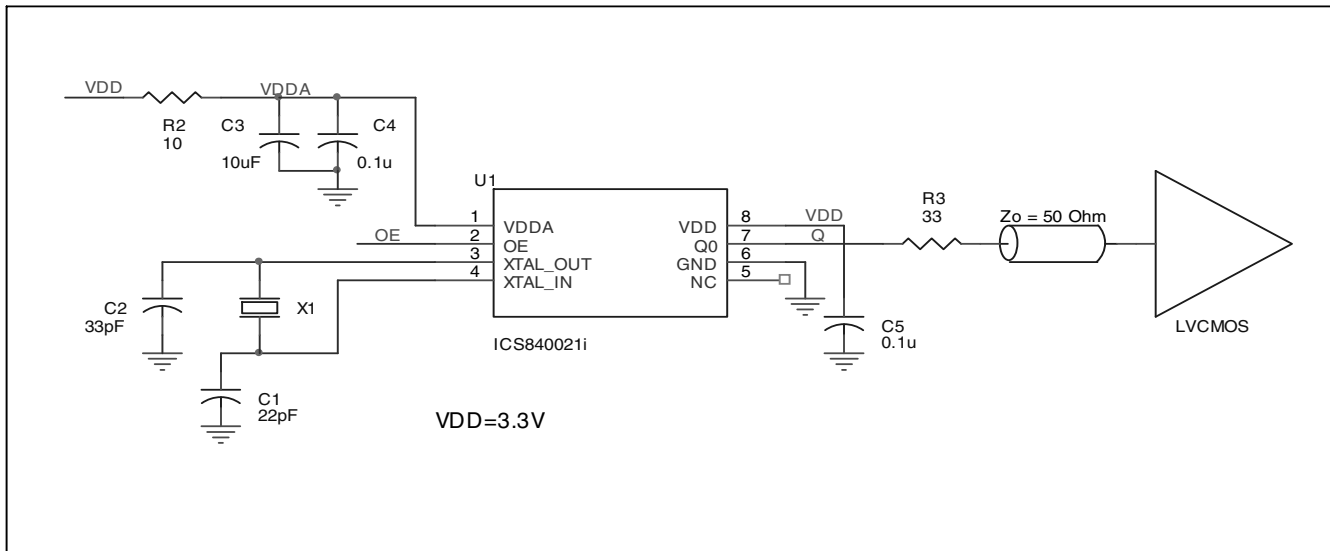
FIGURE 3A. ICS840021I SCHEMATIC EXAMPLE

PC BOARD LAYOUT EXAMPLE

Figure 3B shows an example of ICS840021I P.C. board layout. The crystal X1 footprint shown in this example allows installation of either surface mount HC49S or through-hole HC49 package. The footprints of other components in this example are listed

in the *Table 7.* There should be at least one decoupling capacitor per power pin. The decoupling capacitors should be located as close as possible to the power pins. The layout assumes that the board has clean analog power ground plane.
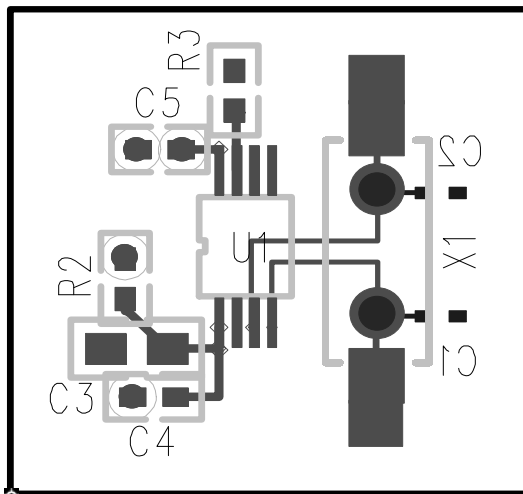

FIGURE 3B. ICS840021I PC BOARD LAYOUT EXAMPLE

TABLE 7. FOOTPRINT TABLE

Reference	Size
C1, C2	0402
C3	0805
C4, C5	0603
R2, R3	0603

NOTE: Table 7, lists component sizes shown in this layout example.

RELIABILITY INFORMATION

TABLE 8. θ_{JA} VS. AIR FLOW TABLE FOR 8 LEAD TSSOP

θ_{JA} by Velocity (Meters per Second)			
	0	1	2.5
Multi-Layer PCB, JEDEC Standard Test Boards	101.7°C/W	90.5°C/W	89.8°C/W

TRANSISTOR COUNT

The transistor count for ICS840021I is: 1961
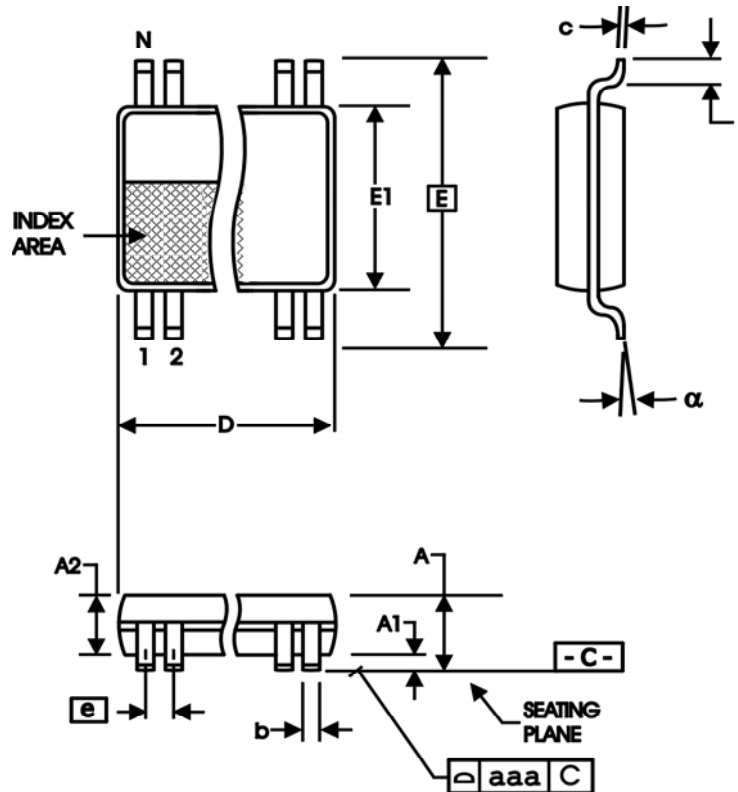
PACKAGE OUTLINE - G SUFFIX FOR 8 LEAD TSSOP

TABLE 9. PACKAGE DIMENSIONS

SYMBOL	Millimeters	
	Minimum	Maximum
N	8	
A	--	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	2.90	3.10
E	6.40 BASIC	
E1	4.30	4.50
e	0.65 BASIC	
L	0.45	0.75
α	0°	8°
aaa	--	0.10

Reference Document: JEDEC Publication 95, MO-153

TABLE 10. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
ICS840021AGI	021AI	8 lead TSSOP	tube	-40°C to 85°C
ICS840021AGIT	021AI	8 lead TSSOP	2500 tape & reel	-40°C to 85°C
ICS840021AGILF	21AIL	8 lead "Lead-Free" TSSOP	tube	-40°C to 85°C
ICS840021AGILFT	21AIL	8 lead "Lead-Free" TSSOP	2500 tape & reel	-40°C to 85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

REVISION HISTORY SHEET				
Rev	**Table**	**Page**	**Description of Change**	**Date**
A	T10	11	Ordering Information Table - Added Lead Free marking	7-30-07