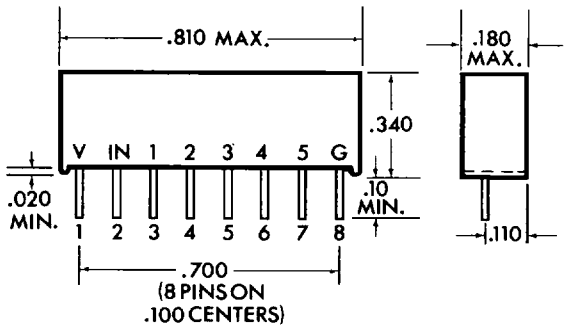
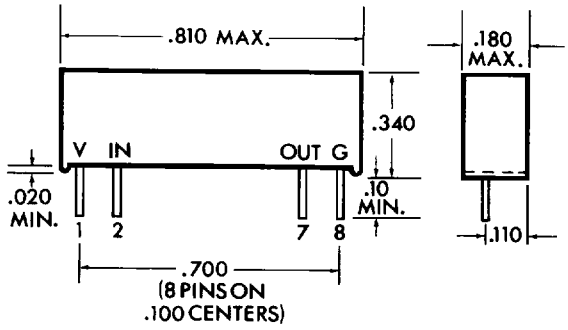
DIGITAL DELAY LINES
8 PIN SINGLE-IN-LINE PACKAGES
TTL COMPATIBLE
5 TAPS AND SINGLE OUTPUT

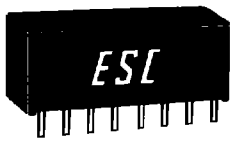
SERIES 5T AND 5G

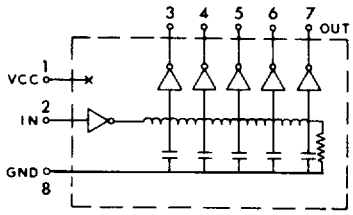


White Dot locates Pin 1

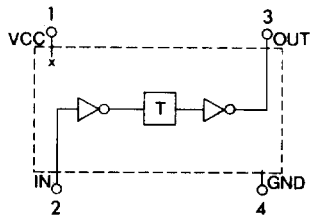


5T





5G



Intermediate delay values available upon request.

Model No.	TD (ns)	TD/Tap (ns)
5T25	25	5
5T30	30	6
5T35	35	7
5T40	40	8
5T45	45	9
5T50	50	10
5T75	75	15
5T100	100	20
5T150	150	30
5T200	200	40
5T250	250	50
5T300	300	60
5T350	350	70
5T400	400	80

Model No.	Delay (ns)
5G10	10
5G25	25
5G30	30
5G35	35
5G40	40
5G50	50
5G75	75
5G100	100
5G150	150
5G200	200
5G250	250
5G300	300
5G350	350
5G400	400

For variations in delay from above listing, modify part number by changing delay.
Example: 120ns, 5T series becomes 5T120.

DC PARAMETERS		LIMITS Min.	LIMITS Max.
V_{oh}	Vcc = min, I_{oh} = 1.0 mA	2.5V	—
V_{ol}	Vcc = min, I_{ol} = 20 mA	—	0.5V
I_{ih}	Vcc = max, V_{ih} = 2.7V	—	50 µA
I_{il}	Vcc = max, V_{il} = 0.5V	-2.0 mA	—
I_i	Vcc = max, V_i = 5.5V	—	1.0 mA
V_i	Vcc = min, I_{in} = -18 madc	-1.2vdc	—
I_{cc}	Vcc = max, outputs low	Series 5T Series 5G	70mA 55mA

SPECIFICATIONS:

- Supply voltage(Vcc): 5.0VDC ± 5%
- Delay tolerances: ± 2ns or ± 5% wig
- Rise Time: 4ns max
- Minimum Pulse Width: 40% of Total delay
- Maximum Duty Cycle: 50%
- Operating temp. range: 0 to 70°C
- Temp. coeff. of delay: 1.0ns + 500ppm/°C
- Terminals: Electro tin plated Alloy 42 .020w x .010th

TEST CONDITIONS:

- Temperature: 25° ± 5°C; Vcc=5.0VDC
- Input pulse width: 1.2 times the total delay time
- Pulse spacing: 5 times the total delay time
- Input rise time: 2ns; input pulse amplitude 3.0VDC
- All outputs loaded with 15pf
- Time delays measured at the 1.5 volts level on the leading edges
- Rise time measured from .75 to 2.4V