

# FDC6333C

## 30V N & P-Channel PowerTrench<sup>®</sup> MOSFETs

### General Description

These N & P-Channel MOSFETs are produced using Fairchild Semiconductor's advanced PowerTrench process that has been especially tailored to minimize on-state resistance and yet maintain superior switching performance.

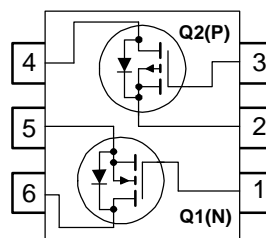
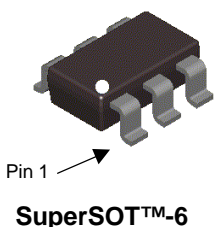
These devices have been designed to offer exceptional power dissipation in a very small footprint for applications where the bigger more expensive SO-8 and TSSOP-8 packages are impractical.

### Applications

- DC/DC converter
- Load switch
- LCD display inverter

### Features

- **Q1** 2.5 A, 30V.  $R_{DS(ON)} = 95 \text{ m}\Omega @ V_{GS} = 10 \text{ V}$   
 $R_{DS(ON)} = 150 \text{ m}\Omega @ V_{GS} = 4.5 \text{ V}$
- **Q2** -2.0 A, 30V.  $R_{DS(ON)} = 150 \text{ m}\Omega @ V_{GS} = -10 \text{ V}$   
 $R_{DS(ON)} = 220 \text{ m}\Omega @ V_{GS} = -4.5 \text{ V}$
- Low gate charge
- High performance trench technology for extremely low  $R_{DS(ON)}$ .
- SuperSOT -6 package: small footprint (72% smaller than SO-8); low profile (1mm thick).



### Absolute Maximum Ratings T<sub>A</sub>=25°C unless otherwise noted

Symbol	Parameter	Q1	Q2	Units
V <sub>DSS</sub>	Drain-Source Voltage	30	-30	V
V <sub>GSS</sub>	Gate-Source Voltage	±16	±25	V
I <sub>D</sub>	Drain Current – Continuous (Note 1a)	2.5	-2.0	A
	– Pulsed	8	-8	
P <sub>D</sub>	Power Dissipation for Single Operation (Note 1a) (Note 1b) (Note 1c)	0.96		W
		0.9		
		0.7		
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Junction Temperature Range	-55 to +150		°C

### Thermal Characteristics

R <sub>θJA</sub>	Thermal Resistance, Junction-to-Ambient (Note 1a)	130	°C/W
R <sub>θJC</sub>	Thermal Resistance, Junction-to-Case (Note 1)	60	°C/W

### Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
.333	FDC6333C	7"	8mm	3000 units

## Electrical Characteristics

T<sub>A</sub> = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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### Off Characteristics

BV <sub>DSS</sub>	Drain–Source Breakdown Voltage	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA V <sub>GS</sub> = 0 V, I <sub>D</sub> = –250 μA	Q1 Q2	30 –30		V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I <sub>D</sub> = 250 μA, Ref. to 25°C I <sub>D</sub> = –250 μA, Ref. to 25°C	Q1 Q2		27 –22	mV/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 24 V, V <sub>GS</sub> = 0 V V <sub>DS</sub> = –24 V, V <sub>GS</sub> = 0 V	Q1 Q2		1 –1	μA
I <sub>GSSF</sub>	Gate–Body Leakage, Forward	V <sub>GS</sub> = 16 V, V <sub>DS</sub> = 0 V V <sub>GS</sub> = 25 V, V <sub>DS</sub> = 0 V	Q1 Q2		100 100	nA
I <sub>GSSR</sub>	Gate–Body Leakage, Reverse	V <sub>GS</sub> = –16 V, V <sub>DS</sub> = 0 V V <sub>GS</sub> = –25 V, V <sub>DS</sub> = 0 V	Q1 Q2		–100 –100	nA

### On Characteristics (Note 2)

V <sub>GS(th)</sub>	Gate Threshold Voltage	Q1	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	1	1.8	3	V
		Q2	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = –250 μA	–1	–1.8	–3	
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	Q1	I <sub>D</sub> = 250 μA, Ref. To 25°C		4		mV/°C
		Q2	I <sub>D</sub> = –250 μA, Ref. to 25°C		–4		
R <sub>DS(on)</sub>	Static Drain–Source On–Resistance	Q1	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 2.5 A V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 2.0 A V <sub>GS</sub> = 10 V, I <sub>D</sub> = 2.5 A, T <sub>J</sub> = 125°C		73 90 106	95 150 148	mΩ
		Q2	V <sub>GS</sub> = –10 V, I <sub>D</sub> = –2.0 A V <sub>GS</sub> = –4.5 V, I <sub>D</sub> = –1.7 A V <sub>GS</sub> = 10 V, I <sub>D</sub> = –2.0 A, T <sub>J</sub> = 125°C		95 142 149	130 220 216	
I <sub>D(on)</sub>	On–State Drain Current	Q1	V <sub>GS</sub> = 10 V, V <sub>DS</sub> = 5 V	8			A
		Q2	V <sub>GS</sub> = –10 V, V <sub>DS</sub> = –5 V	–8			
g <sub>FS</sub>	Forward Transconductance	Q1	V <sub>DS</sub> = 5 V, I <sub>D</sub> = 2.5 A		7		S
		Q2	V <sub>DS</sub> = –5 V, I <sub>D</sub> = –2.0 A		3		

### Dynamic Characteristics

C <sub>iss</sub>	Input Capacitance	Q1	V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 0 V, f = 1.0 MHz		282		pF
		Q2	V <sub>DS</sub> = –15 V, V <sub>GS</sub> = 0 V, f = 1.0 MHz		185		
C <sub>oss</sub>	Output Capacitance	Q1	V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 0 V, f = 1.0 MHz		49		pF
		Q2	V <sub>DS</sub> = –15 V, V <sub>GS</sub> = 0 V, f = 1.0 MHz		56		
C <sub>rss</sub>	Reverse Transfer Capacitance	Q1	V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 0 V, f = 1.0 MHz		20		pF
		Q2	V <sub>DS</sub> = –15 V, V <sub>GS</sub> = 0 V, f = 1.0 MHz		26		

### Switching Characteristics (Note 2)

t <sub>d(on)</sub>	Turn–On Delay Time	Q1	For Q1: V <sub>DS</sub> = 15 V, I <sub>DS</sub> = 1 A V <sub>GS</sub> = 10 V, R <sub>GEN</sub> = 6 Ω		4.5	9	ns
		Q2			4.5	9	
t <sub>r</sub>	Turn–On Rise Time	Q1	For Q2: V <sub>DS</sub> = –15 V, I <sub>DS</sub> = –1 A V <sub>GS</sub> = –10 V, R <sub>GEN</sub> = 6 Ω		6	12	ns
		Q2			13	23	
t <sub>d(off)</sub>	Turn–Off Delay Time	Q1			19	34	ns
		Q2			11	20	
t <sub>f</sub>	Turn–Off Fall Time	Q1			1.5	3	ns
		Q2			2	4	
Q <sub>g</sub>	Total Gate Charge	Q1	For Q1: V <sub>DS</sub> = 15 V, I <sub>DS</sub> = 2.5 A V <sub>GS</sub> = 10 V, R <sub>GEN</sub> = 6 Ω		4.7	6.6	nC
		Q2			4.1	5.7	
Q <sub>gs</sub>	Gate–Source Charge	Q1	For Q2: V <sub>DS</sub> = –15 V, I <sub>DS</sub> = –2.0 A V <sub>GS</sub> = –10 V,		0.9		nC
		Q2			0.8		
Q <sub>gd</sub>	Gate–Drain Charge	Q1			0.6		nC
		Q2			0.4		

### Electrical Characteristics

$T_A = 25^\circ\text{C}$  unless otherwise noted

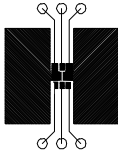
Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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#### Drain–Source Diode Characteristics and Maximum Ratings

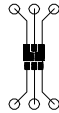
$I_S$	Maximum Continuous Drain–Source Diode Forward Current	Q1			0.8	A	
		Q2			-0.8		
$V_{SD}$	Drain–Source Diode Forward Voltage	Q1	$V_{GS} = 0\text{ V}, I_S = 0.8\text{ A}$ (Note 2)		0.8	1.2	V
		Q2	$V_{GS} = 0\text{ V}, I_S = 0.8\text{ A}$ (Note 2)		0.8	-1.2	

**Notes:**

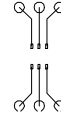
1.  $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



- a)  $130^\circ\text{C/W}$  when mounted on a  $0.125\text{ in}^2$  pad of 2 oz. copper.



- b)  $140^\circ\text{C/W}$  when mounted on a  $.004\text{ in}^2$  pad of 2 oz copper



- c)  $180^\circ\text{C/W}$  when mounted on a minimum pad.

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width <  $300\mu\text{s}$ , Duty Cycle < 2.0%

## Typical Characteristics: N-Channel

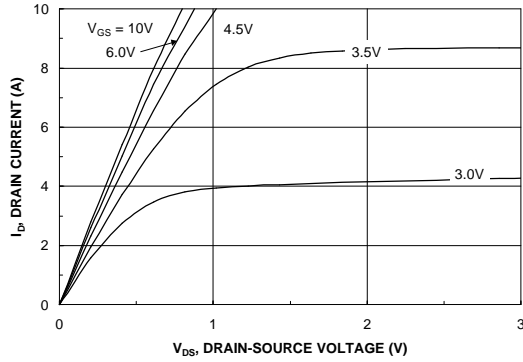


Figure 1. On-Region Characteristics.

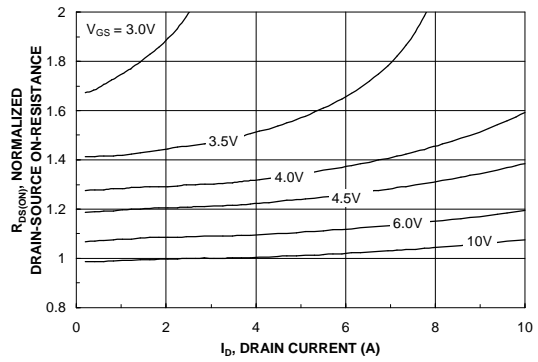


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

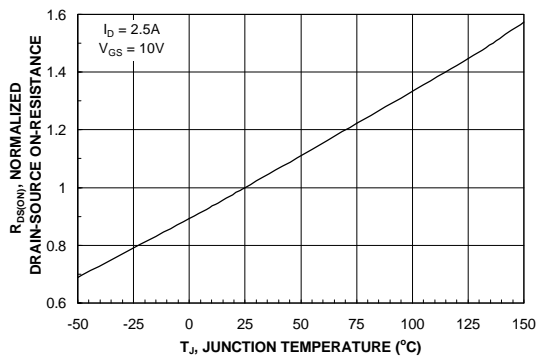


Figure 3. On-Resistance Variation with Temperature.

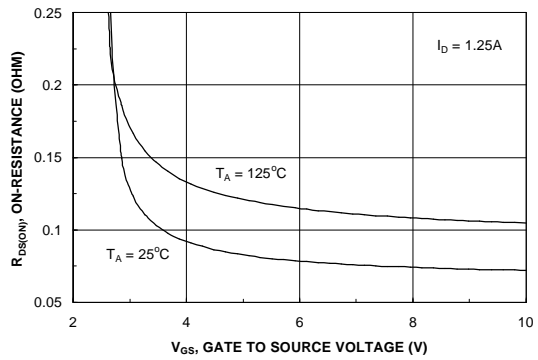


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

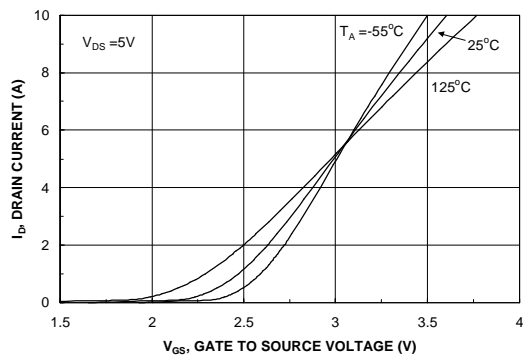


Figure 5. Transfer Characteristics.

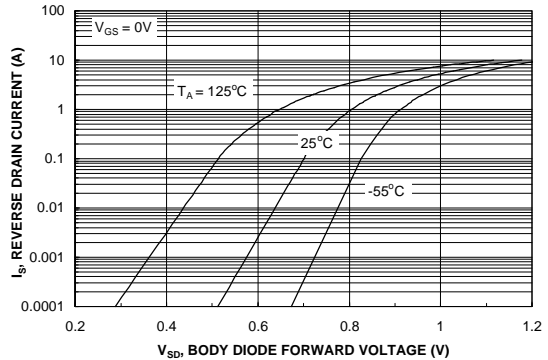
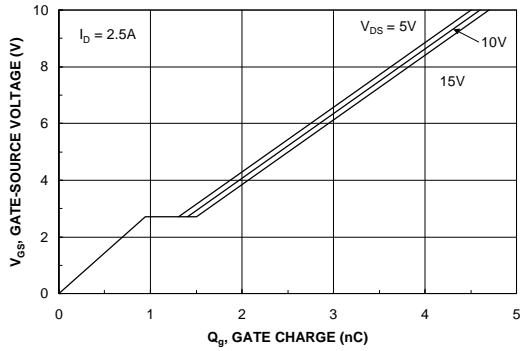
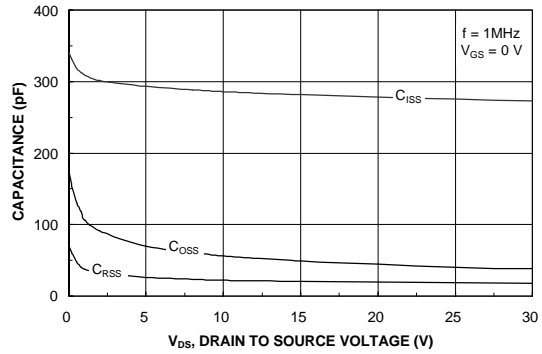


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

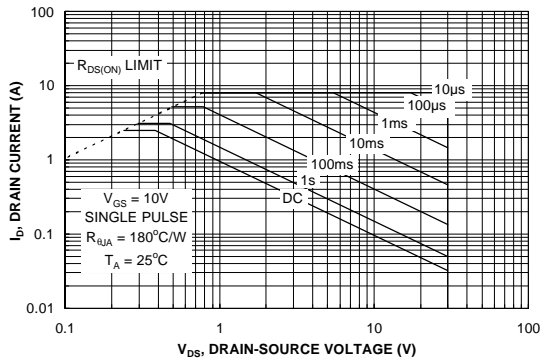
**Typical Characteristics: N-Channel** (continued)



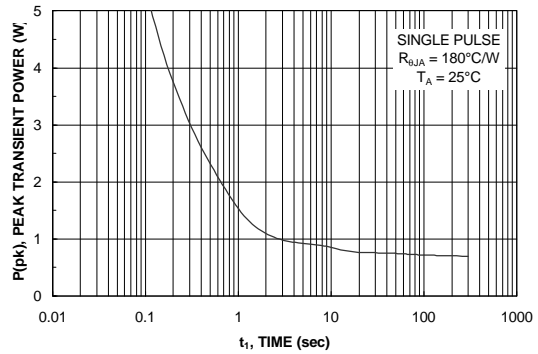
**Figure 7. Gate Charge Characteristics.**



**Figure 8. Capacitance Characteristics.**



**Figure 9. Maximum Safe Operating Area.**



**Figure 10. Single Pulse Maximum Power Dissipation.**

Typical Characteristics: P-Channel

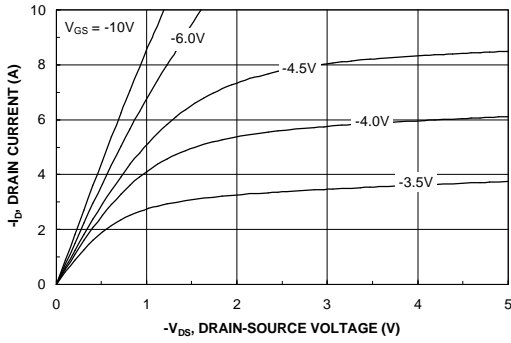


Figure 11. On-Region Characteristics.

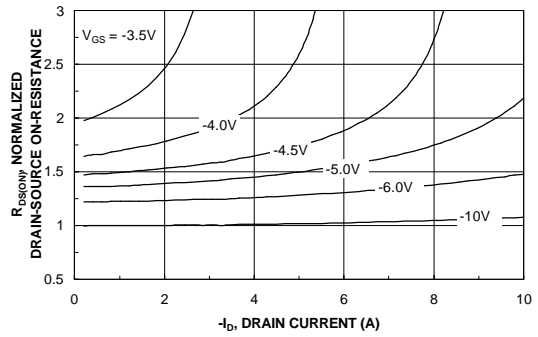


Figure 12. On-Resistance Variation with Drain Current and Gate Voltage.

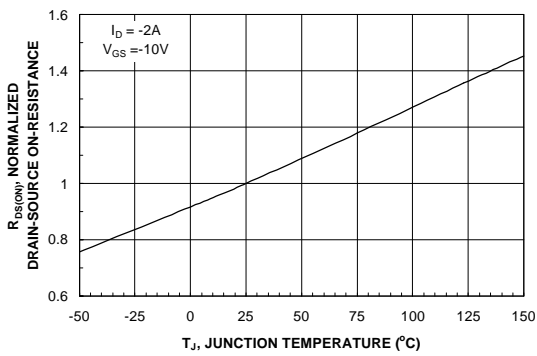


Figure 13. On-Resistance Variation with Temperature.

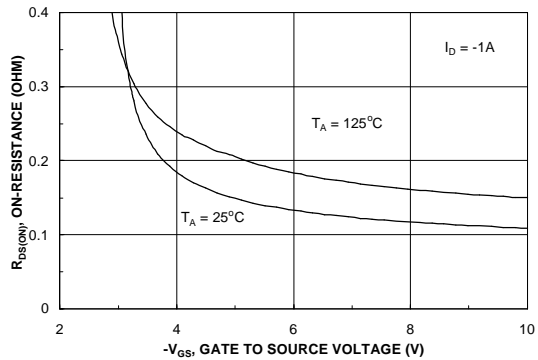


Figure 14. On-Resistance Variation with Gate-to-Source Voltage.

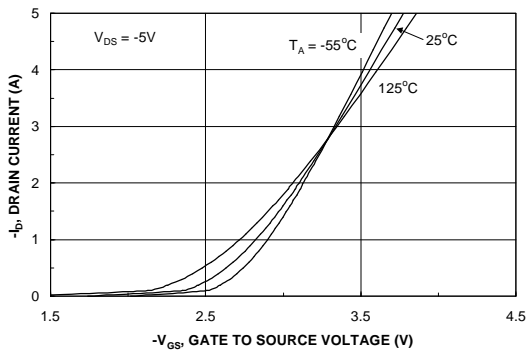


Figure 15. Transfer Characteristics.

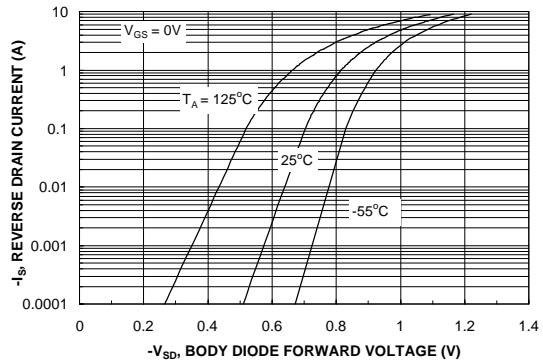
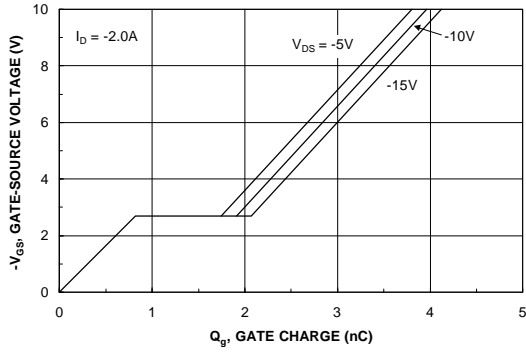
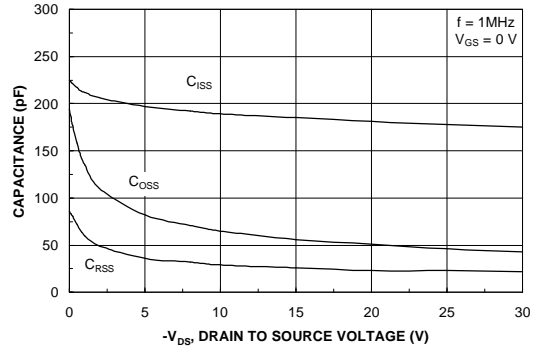


Figure 16. Body Diode Forward Voltage Variation with Source Current and Temperature.

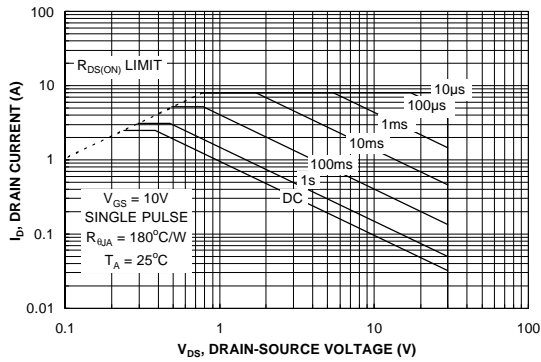
**Typical Characteristics: P-Channel** (continued)



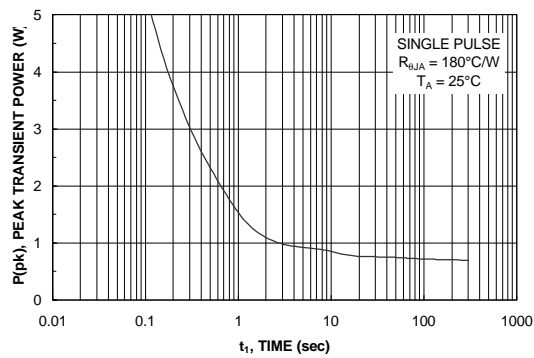
**Figure 17. Gate Charge Characteristics.**



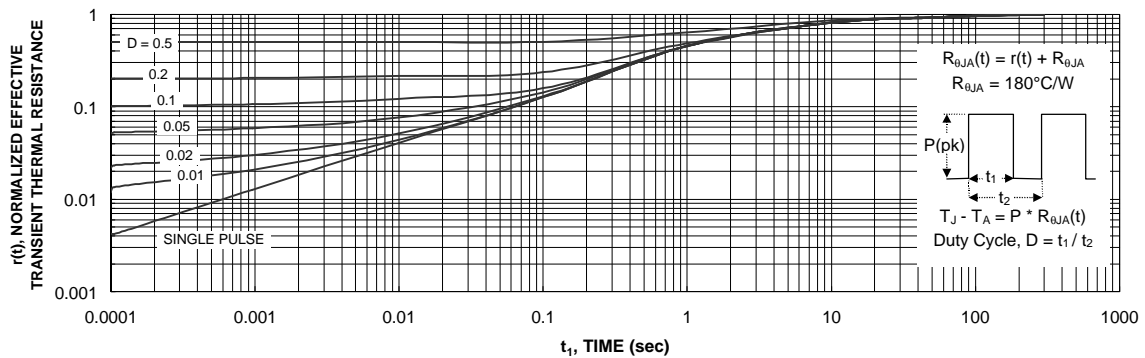
**Figure 18. Capacitance Characteristics.**



**Figure 19. Maximum Safe Operating Area.**



**Figure 20. Single Pulse Maximum Power Dissipation.**



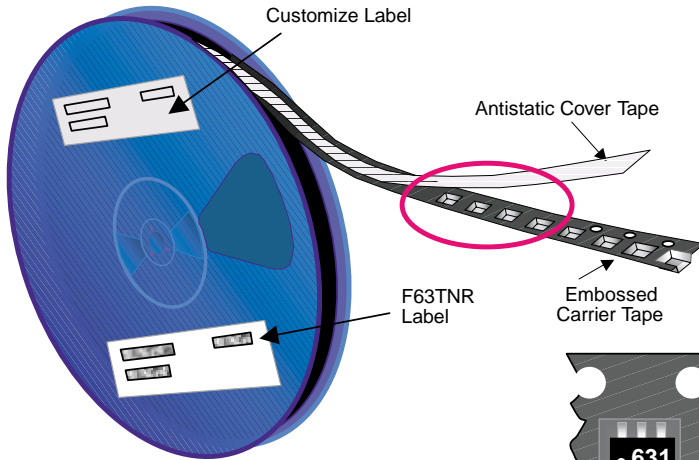
**Figure 21. Transient Thermal Response Curve.**

Thermal characterization performed using the conditions described in Note 1c.  
Transient thermal response will change depending on the circuit board design.

# SuperSOT™-6 Tape and Reel Data



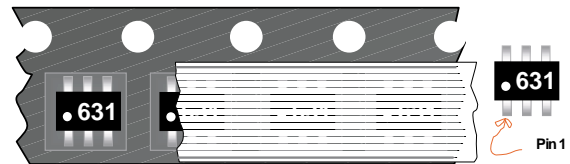
## SSOT-6 Packaging Configuration: Figure 1.0



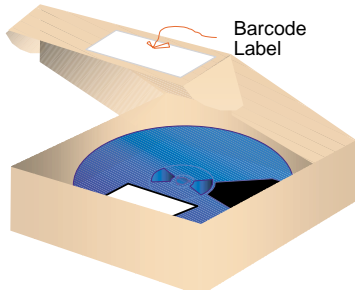
**Packaging Description:**  
 SSOT-6 parts are shipped in tape. The carrier tape is made from a dissipative (carbon filled) polycarbonate resin. The cover tape is a multilayer film (Heat Activated Adhesive in nature) primarily composed of polyester film, adhesive layer, sealant, and anti-static sprayed agent. These reeled parts in standard option are shipped with 3,000 units per 7" or 177cm diameter reel. The reels are dark blue in color and is made of polystyrene plastic (anti-static coated). Other option comes in 10,000 units per 13" or 330cm diameter reel. This and some other options are described in the Packaging Information table.

These full reels are individually barcode labeled and placed inside a pizza box (illustrated in figure 1.0) made of recyclable corrugated brown paper with a Fairchild logo printing. One pizza box contains five reels maximum. And these pizza boxes are placed inside a barcode labeled shipping box which comes in different sizes depending on the number of parts shipped.

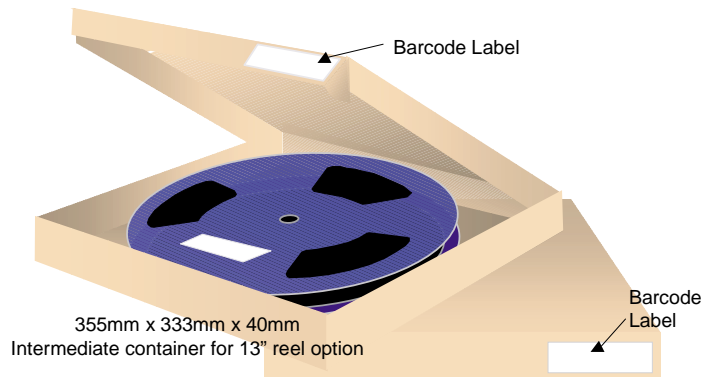
SSOT-6 Packaging Information		
Packaging Option	Standard (no flow code)	D87Z
Packaging type	TNR	TNR
Qty per Reel/Tube/Bag	3,000	10,000
Reel Size	7" Dia	13"
Box Dimension (mm)	193x183x80	355x333x40
Max qty per Box	15,000	30,000
Weight per unit (gm)	0.0158	0.0158
Weight per Reel (kg)	0.1440	0.4700
Note/Comments		



### SSOT-6 Unit Orientation



193mm x 183mm x 80mm  
 Pizza Box for Standard Option

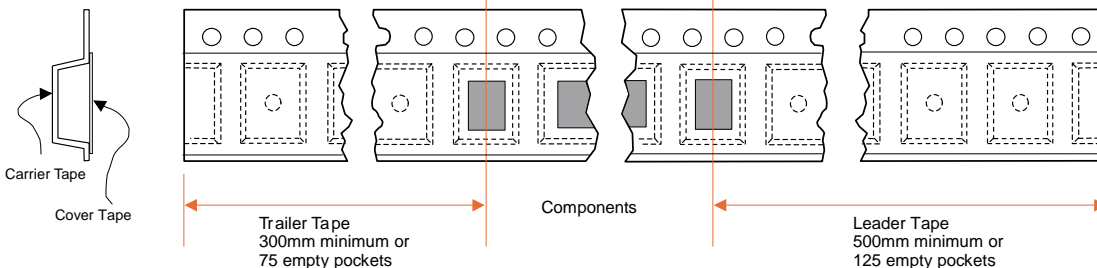


355mm x 333mm x 40mm  
 Intermediate container for 13" reel option

### Barcode Label sample



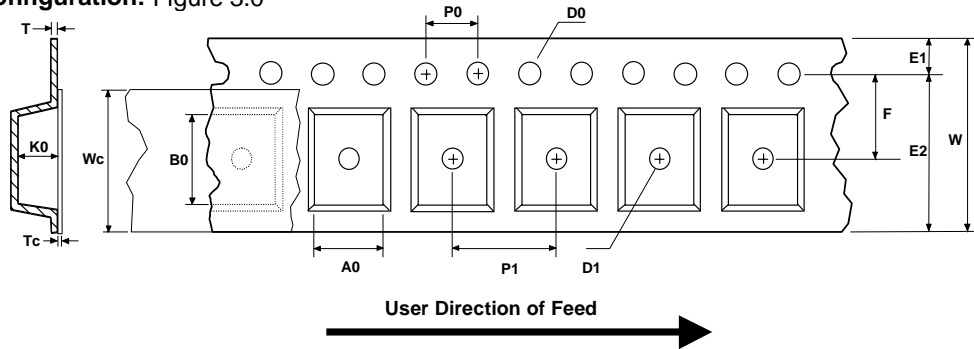
## SSOT-6 Tape Leader and Trailer Configuration: Figure 2.0





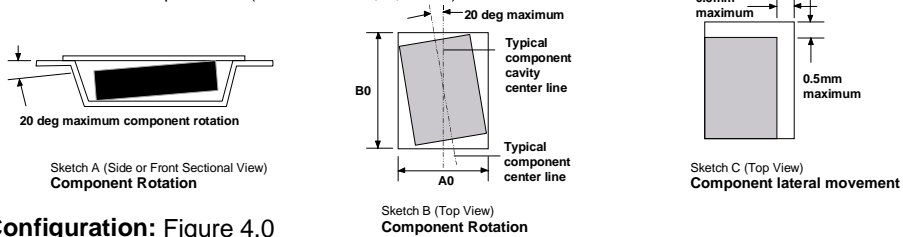
# SuperSOT™-6 Tape and Reel Data, continued

## SSOT-6 Embossed Carrier Tape Configuration: Figure 3.0

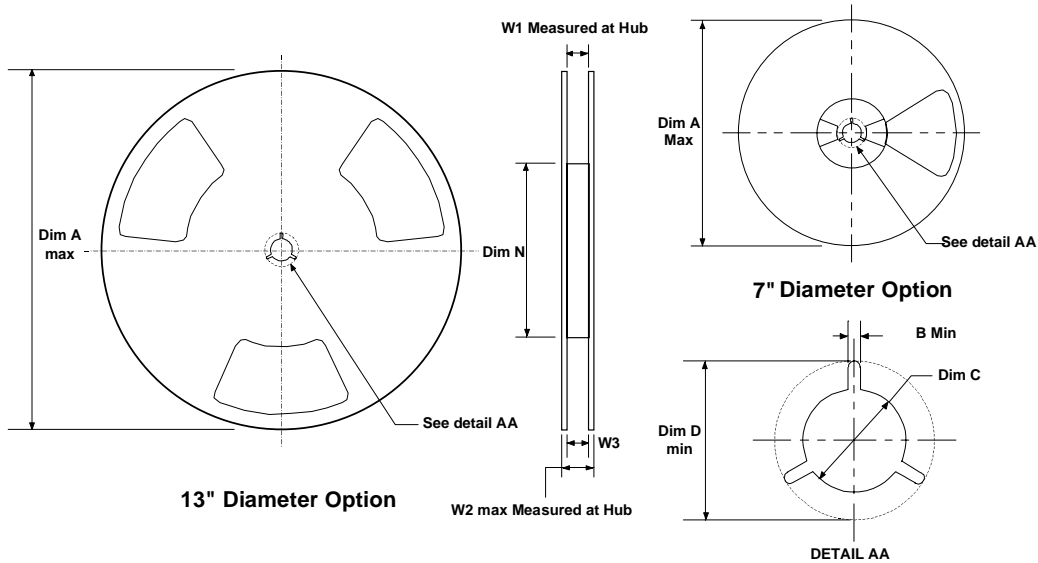


Dimensions are in millimeter														
Pkg type	A0	B0	W	D0	D1	E1	E2	F	P1	P0	K0	T	Wc	Tc
SSOT-6 (8mm)	3.23 +/-0.10	3.18 +/-0.10	8.0 +/-0.3	1.55 +/-0.05	1.125 +/-0.125	1.75 +/-0.10	6.25 min	3.50 +/-0.05	4.0 +/-0.1	4.0 +/-0.1	1.37 +/-0.10	0.255 +/-0.150	5.2 +/-0.3	0.06 +/-0.02

Notes: A0, B0, and K0 dimensions are determined with respect to the EIA/Jedec RS-481 rotational and lateral movement requirements (see sketches A, B, and C).



## SSOT-6 Reel Configuration: Figure 4.0

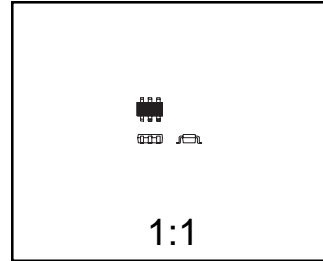
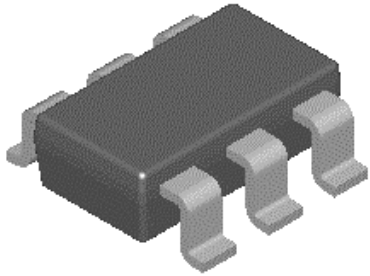


Dimensions are in inches and millimeters									
Tape Size	Reel Option	Dim A	Dim B	Dim C	Dim D	Dim N	Dim W1	Dim W2	Dim W3 (LSL-USL)
8mm	7" Dia	7.00 177.8	0.059 1.5	512 +0.020/-0.008 13 +0.5/-0.2	0.795 20.2	2.165 55	0.331 +0.059/-0.000 8.4 +1.5/0	0.567 14.4	0.311 - 0.429 7.9 - 10.9
8mm	13" Dia	13.00 330	0.059 1.5	512 +0.020/-0.008 13 +0.5/-0.2	0.795 20.2	4.00 100	0.331 +0.059/-0.000 8.4 +1.5/0	0.567 14.4	0.311 - 0.429 7.9 - 10.9

# SuperSOT™-6 Package Dimensions



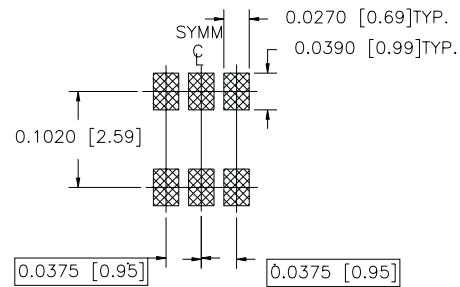
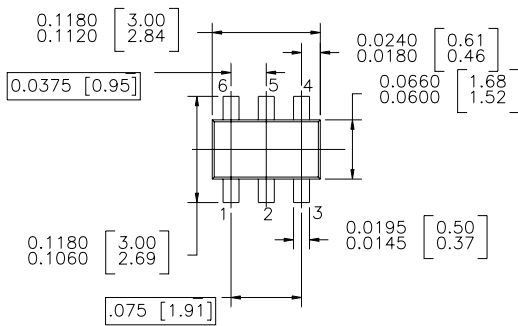
## SuperSOT™-6 (FS PKG Code 31, 33)



Scale 1:1 on letter size paper

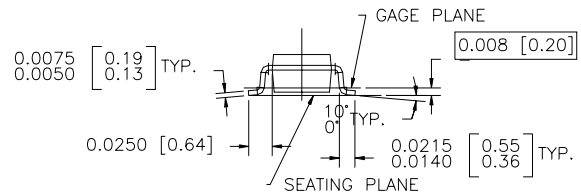
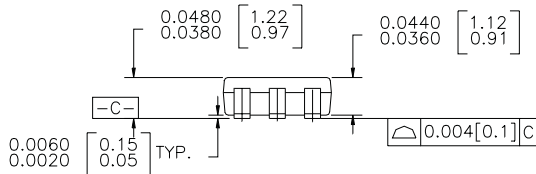
Dimensions shown below are in:  
inches [millimeters]

Part Weight per unit (gram): 0.0158



LAND PATTERN RECOMMENDATION

CONTROLLING DIMENSION IS INCH  
VALUES IN [ ] ARE MILLIMETERS



SUPER SOT 6 LEADS

NOTES : UNLESS OTHERWISE SPECIFIED

1.0 STANDARD LEAD FINISH : 150 MICROINCHES 93.81 MICROMETERS)  
MINIMUM TIN / LEAD (SOLDER) ON COPPER.

2.0 NO JEDEC REGISTRATION AS OF JULY 1996

## TRADEMARKS

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ACE <sub>x</sub> <sup>TM</sup>	FAST <sup>®</sup>	OPTOLOGIC <sup>TM</sup>	SMART START <sup>TM</sup>	VCX <sup>TM</sup>
Bottomless <sup>TM</sup>	FAST <sub>r</sub> <sup>TM</sup>	OPTOPLANAR <sup>TM</sup>	STAR*POWER <sup>TM</sup>	
CoolFET <sup>TM</sup>	FRFET <sup>TM</sup>	PACMAN <sup>TM</sup>	Stealth <sup>TM</sup>	
CROSSVOLT <sup>TM</sup>	GlobalOptoisolator <sup>TM</sup>	POP <sup>TM</sup>	SuperSOT <sup>TM</sup> -3	
DenseTrench <sup>TM</sup>	GTO <sup>TM</sup>	Power247 <sup>TM</sup>	SuperSOT <sup>TM</sup> -6	
DOMET <sup>TM</sup>	HiSeC <sup>TM</sup>	PowerTrench <sup>®</sup>	SuperSOT <sup>TM</sup> -8	
EcoSPARK <sup>TM</sup>	ISOPLANAR <sup>TM</sup>	QFET <sup>TM</sup>	SyncFET <sup>TM</sup>	
E <sup>2</sup> CMOS <sup>TM</sup>	LittleFET <sup>TM</sup>	QST <sup>TM</sup>	TinyLogic <sup>TM</sup>	
EnSigna <sup>TM</sup>	MicroFET <sup>TM</sup>	QT Optoelectronics <sup>TM</sup>	TruTranslation <sup>TM</sup>	
FACT <sup>TM</sup>	MicroPak <sup>TM</sup>	Quiet Series <sup>TM</sup>	UHC <sup>TM</sup>	
FACT Quiet Series <sup>TM</sup>	MICROWIRE <sup>TM</sup>	SILENT SWITCHER <sup>®</sup>	UltraFET <sup>®</sup>	

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

## PRODUCT STATUS DEFINITIONS

### Definition of Terms

Datasheet Identification	Product Status	Definition
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