SRAM

8K x 8 SRAM

FEATURES

- High speed: 8, 10, 12, 15, 20, 25 and 35ns
- High-performance, low-power, CMOS double-metal process
- Single +5V ±10% power supply
- Easy memory expansion with $\overline{CE}1$, CE2 and $\overline{OE}$ options
- All inputs and outputs are TTL compatible

OPTIONS MARKING

- Timing

8ns access (preliminary)	- 8
10ns access	-10
12ns access	-12
15ns access	-15
20ns access	-20
25ns access	-25
30ns access	-30
35ns access	-35

- Packages

Plastic DIP (300 mil)	None
Plastic SOJ (300 mil)	DJ

Available in ceramic packages tested to meet military specifications. Please refer to Micron's ***Military Data Book***.

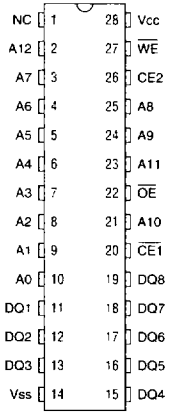
- 2V data retention — L

- Temperature

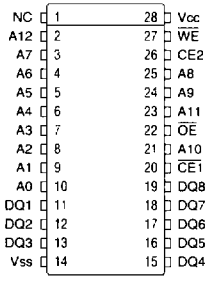
Industrial	(-40°C to +85°C)	IT
Automotive	(-40°C to +125°C)	AT
Extended	(-55°C to +125°C)	XT

PIN ASSIGNMENT (Top View)

28-Pin DIP (A-9)



28-Pin SOJ (E-8)



GENERAL DESCRIPTION

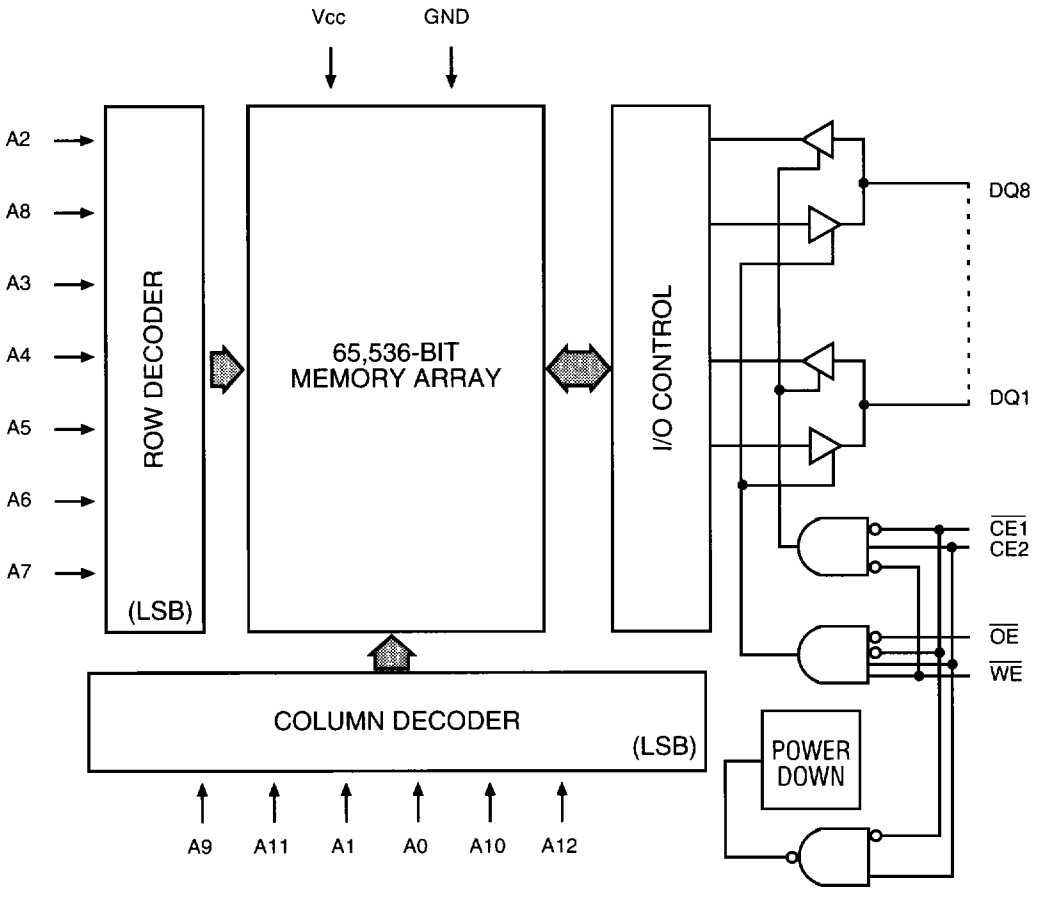
The Micron SRAM family employs high-speed, low-power CMOS designs using a four-transistor memory cell. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

For flexibility in high-speed memory applications, Micron offers two chip enables on the x8 organizations. This enhancement can place the outputs in High-Z for additional flexibility in system design.

Writing to these devices is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ goes to LOW. The device offers a reduced power standby mode when disabled. This allows system designers to achieve their low standby power requirements.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{CE1}$	CE2	$\overline{OE}$	$\overline{WE}$	DQ	POWER
STANDBY	H	X	X	X	HIGH-Z	STANDBY
STANDBY	X	L	X	X	HIGH-Z	STANDBY
READ	L	H	H	L	Q	ACTIVE
READ	L	H	H	H	HIGH-Z	ACTIVE
WRITE	L	H	L	X	D	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1.0V to +7.0V
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$; V_{CC} = 5V ±10%)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	V_{CC} +1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	I_{LI}	-5	5	µA	
Output Leakage Current	Output(s) Disabled $0V \le V_{OUT} \le V_{CC}$	I_{LO}	-5	5	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1

				MAX								
DESCRIPTION	CONDITIONS	SYMBOL	TYP	-8	-10	-12	-15	-20	-25	-35	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE} \le V_{IL}$; V_{CC} = MAX f = MAX = 1/ ^tRC Outputs Open	I_{CC}	65	160	150	140	120	110	100	90	mA	3, 14
Power Supply Current: Standby	$\overline{CE} \ge V_{IH}$; V_{CC} = MAX f = MAX = 1/ ^tRC Outputs Open	I_{SB1}	20	55	50	45	40	35	30	25	mA	14
	$\overline{CE} \ge V_{CC}$ -0.2V; V_{CC} = MAX $V_{IL} \le V_{SS}$ +0.2V $V_{IH} \ge V_{CC}$ -0.2V; f = 0	I_{SB2}	0.4	3	3	3	3	3	3	3	mA	14

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C, f = 1 MHz V_{CC} = 5V	C_I	5	pF	4
Output Capacitance		C_O	7	pF	4

FAST SRAM

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5, 13) ($0°C \le T_A \le 70°C$; V_{CC} = 5V ±10%)

DESCRIPTION		-8*		-10		-12		-15		-20		-25		-35			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle																	
READ cycle time	^tRC	8		10		12		15		20		25		35		ns	
Address access time	^tAA		8		10		12		15		20		25		35	ns	
Chip Enable access time	^tACE		7		9		10		12		15		20		30	ns	
Output hold from address change	^tOH	3		3		3		3		3		3		3		ns	
Chip Enable to output in Low-Z	^tLZCE	2		2		2		3		5		5		5		ns	
Chip disable to output in High-Z	^tHZCE		4		5		6		7		8		8		8	ns	6, 7
Chip Enable to power-up time	^tPU	0		0		0		0		0		0		0		ns	
Chip disable to power-down time	^tPD		8		10		12		15		20		25		35	ns	
Output Enable access time	^tAOE		4		5		6		7		8		8		15	ns	
Output Enable to output in Low-Z	^tLZOE	0		0		0		0		0		0		0		ns	
Output disable to output in High-Z	^tHZOE		4		5		5		6		7		8		8	ns	6
WRITE Cycle																	
WRITE cycle time	^tWC	8		10		12		15		20		25		35		ns	
Chip Enable to end of write	^tCW	8		9		10		12		15		20		25		ns	
Address valid to end of write	^tAW	8		9		11		12		15		20		25		ns	
Address setup time	^tAS	0		0		0		0		0		0		0		ns	
Address hold from end of write	^tAH	0		0		0		0		0		0		0		ns	
WRITE pulse width	$^tWP1$	7		8		9		12		15		18		20		ns	
WRITE pulse width	$^tWP2$	8		9		10		14		18		20		25		ns	
Data setup time	^tDS	5		6		7		8		10		10		12		ns	
Data hold time	^tDH	0		0		0		0		0		0		0		ns	
Write disable to output in Low-Z	^tLZWE	2		2		2		2		2		2		2		ns	
Write Enable to output in High-Z	^tHZWE		4		5		5		6		8		8		8	ns	6

*These specifications are preliminary.

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

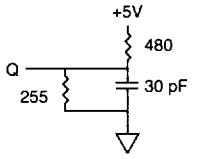


Fig. 1 OUTPUT LOAD EQUIVALENT

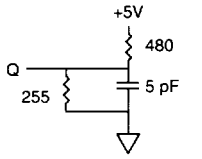


Fig. 2 OUTPUT LOAD EQUIVALENT

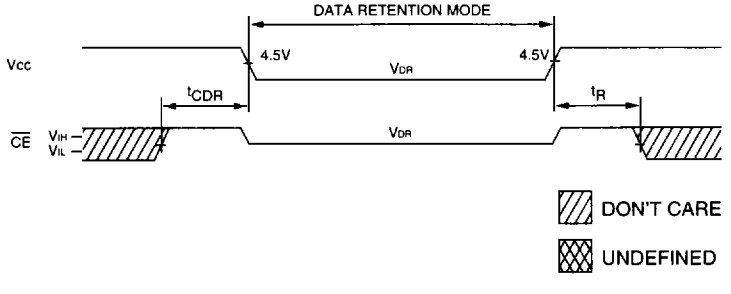
NOTES

1. All voltages referenced to Vss (GND).
2. -3V for pulse width < 20ns.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE, ^{t}HZWE and ^{t}HZOE are specified with CL = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables are held in their active state.
10. Address valid prior to or coincident with latest occurring chip enable.
11. ^{t}RC = Read Cycle Time.
12. Chip enable ($\overline{CE}$) and write enable ($\overline{WE}$) can initiate and terminate a WRITE cycle.
13. For automotive, industrial and extended temperature specifications, refer to page 1-173.
14. Typical values are measured at 5V, 25°C and 20ns cycle time.

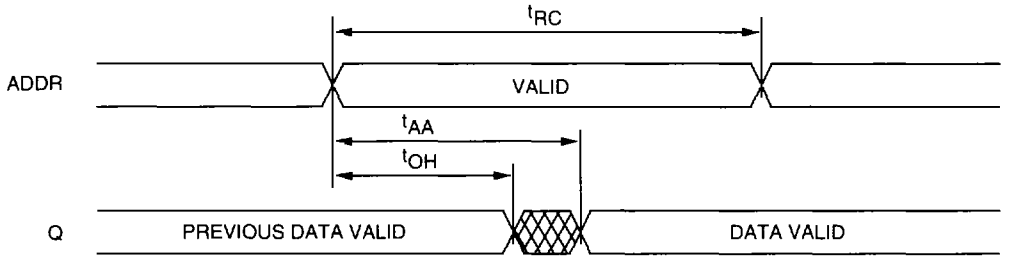
DATA RETENTION ELECTRICAL CHARACTERISTICS (L Version Only)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Vcc for Retention Data			VDR	2		—	V	
Data Retention Current	$\overline{CE}$ ≥ (Vcc -0.2V) VIN ≥ (Vcc -0.2V) or ≤ 0.2V	Vcc = 2V	ICCDR		95	250	µA	
		Vcc = 3V			125	400	µA	
Chip Deselect to Data Retention Time			^{t}CDR	0		—	ns	4
Operation Recovery Time			^{t}R	^{t}RC			ns	4, 11

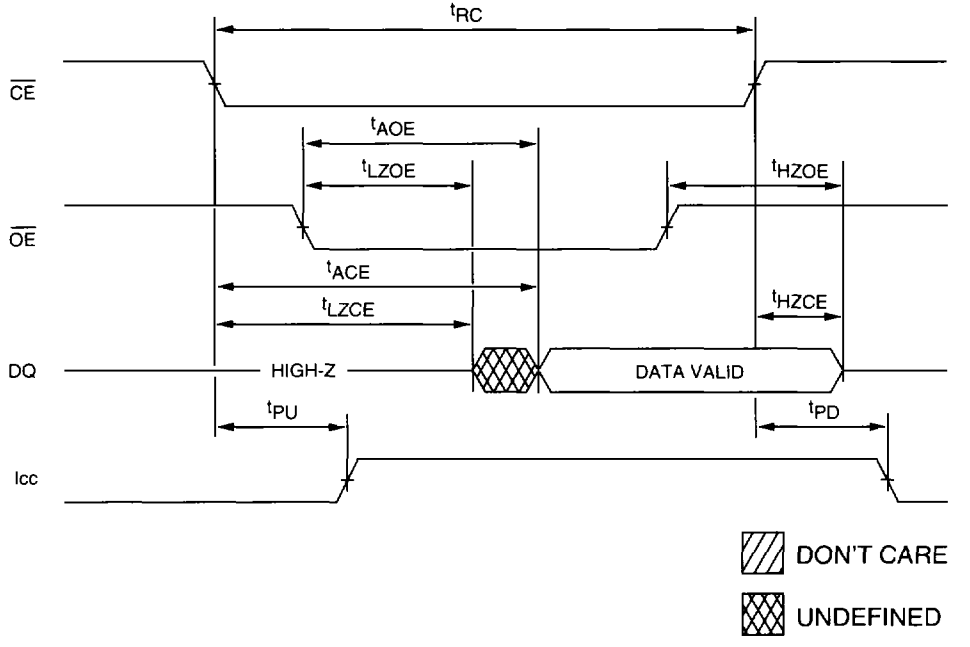
LOW Vcc DATA RETENTION WAVEFORM



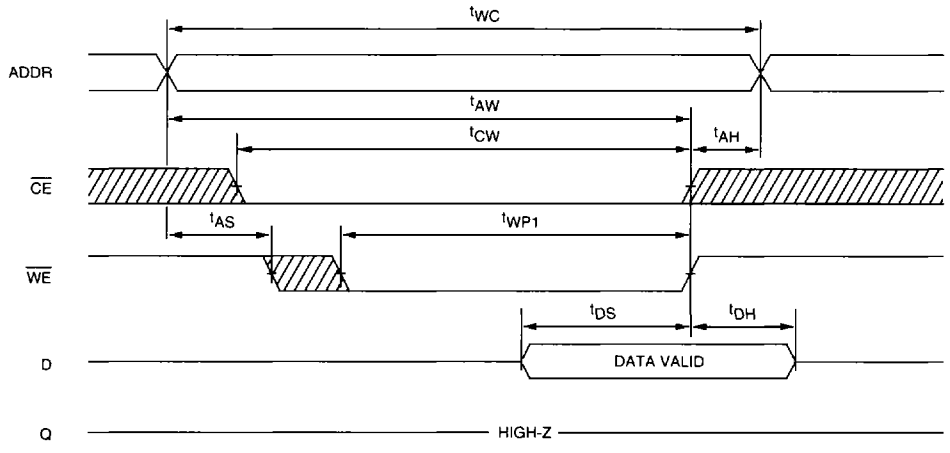
READ CYCLE NO. 1 [8, 9]



READ CYCLE NO. 2 [7, 8, 10]

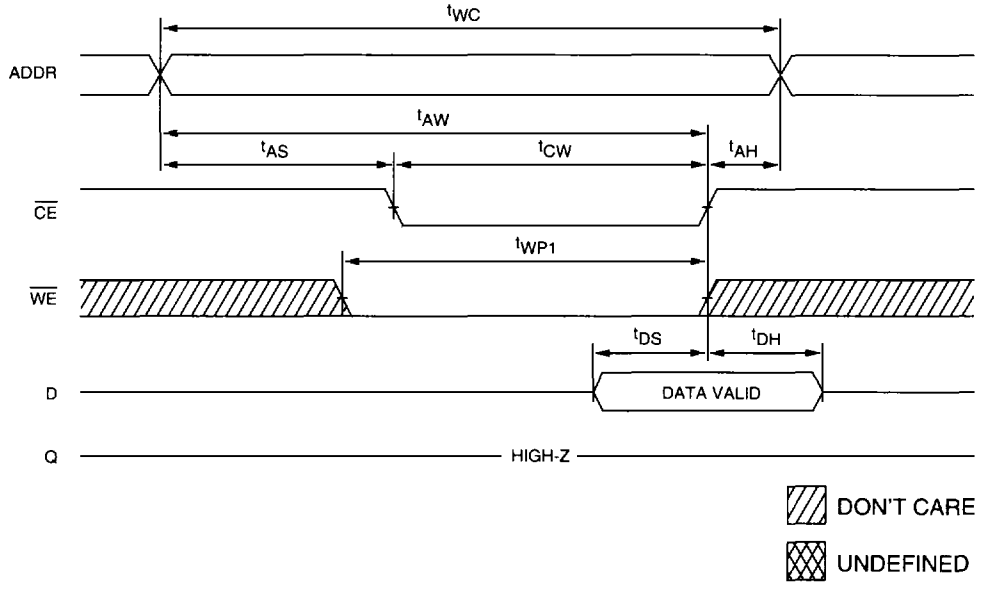


WRITE CYCLE NO. 1
(Write Enable Controlled) [12]



NOTE: Output enable ($\overline{OE}$) is inactive (HIGH).

WRITE CYCLE NO. 2
(Chip Enable Controlled)



WRITE CYCLE NO. 3

(Write Enable Controlled) [7, 12]