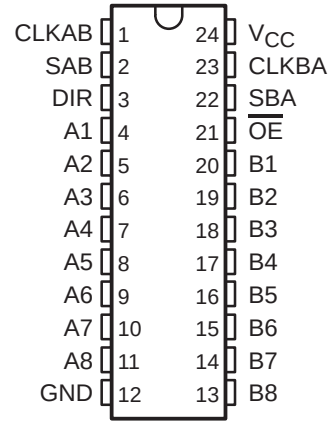
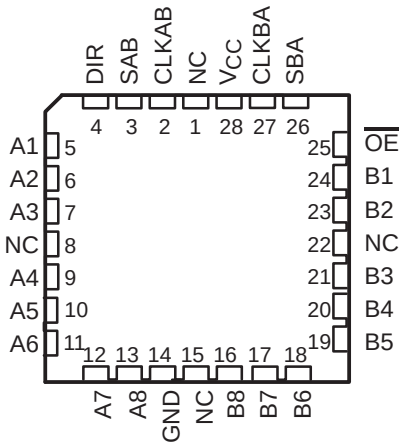
- **Independent Registers for A and B Buses**
- **Multiplexed Real-Time and Stored Data**
- **Choice of True or Inverting Data Paths**
- **Choice of 3-State or Open-Collector Outputs**
- **Package Options Include Plastic Small-Outline (DW) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (NT) and Ceramic (JT) 300-mil DIPs**

DEVICE	OUTPUT	LOGIC
SN54ALS646, SN74ALS646A, ′AS646	3 state	True
SN54ALS648, SN74ALS648A, SN74AS648	3 state	Inverting

SN54ALS646, SN54ALS648, SN54AS646 . . . JT PACKAGE
SN74ALS646A, SN74ALS648A, SN74AS646,
SN74AS648 . . . DW OR NT PACKAGE
(TOP VIEW)



SN54ALS646, SN54ALS648, SN54AS646 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

These devices consist of bus-transceiver circuits with 3-state or open-collector outputs, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. Data on the A or B bus is clocked into the registers on the low-to-high transition of the appropriate clock (CLKAB or CLKBA) input. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the octal bus transceivers and registers.

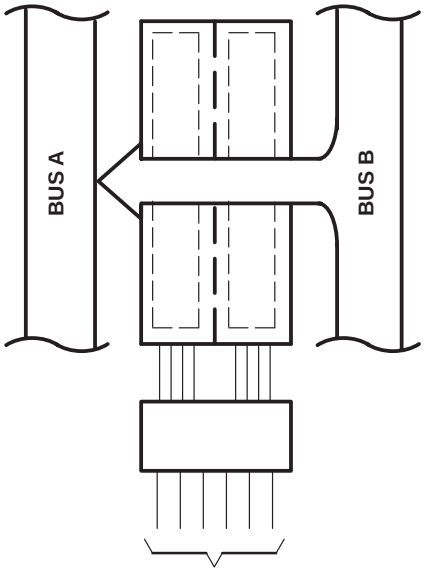
Output-enable ($\overline{OE}$) and direction-control (DIR) inputs control the transceiver functions. In the transceiver mode, data present at the high-impedance port may be stored in either or both registers.

The select-control (SAB and SBA) inputs can multiplex stored and real-time (transparent mode) data. The circuitry used for select control eliminates the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. DIR determines which bus receives data when $\overline{OE}$ is low. In the isolation mode ($\overline{OE}$ high), A data may be stored in one register and/or B data may be stored in the other register.

When an output function is disabled, the input function is still enabled and can be used to store and transmit data. Only one of the two buses, A or B, may be driven at a time.

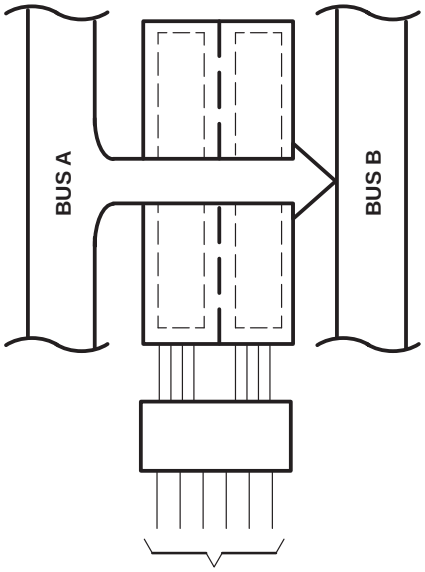
The -1 version of the SN74ALS646A is identical to the standard version, except that the recommended maximum I_{OL} in the -1 version is increased to 48 mA. There are no -1 versions of the SN54ALS646, SN54ALS648, or SN74ALS648A.

The SN54ALS646, SN54ALS648, and SN54AS646 are characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ALS646A, SN74ALS648A, SN74AS646, and SN74AS648 are characterized for operation from 0°C to 70°C.



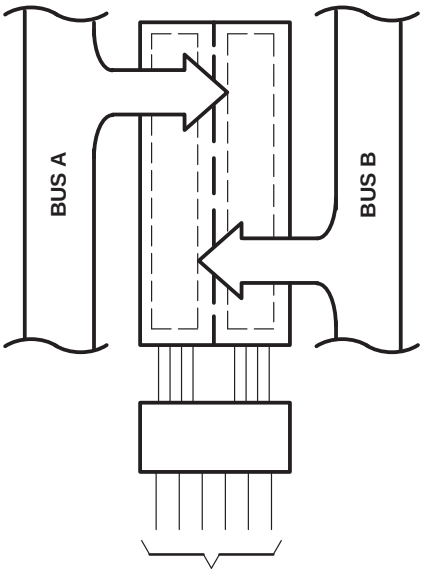
21 $\overline{OE}$	3 DIR	1 CLKAB	23 CLKBA	2 SAB	22 SBA
L	L	X	X	X	L

REAL-TIME TRANSFER BUS B TO BUS A



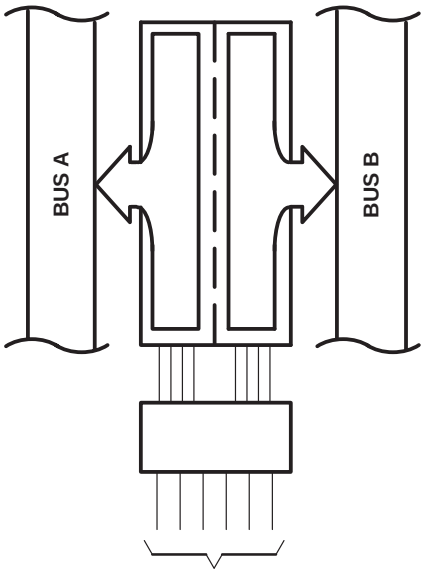
21 $\overline{OE}$	3 DIR	1 CLKAB	23 CLKBA	2 SAB	22 SBA
L	H	X	X	L	X

REAL-TIME TRANSFER BUS A TO BUS B



21 $\overline{OE}$	3 DIR	1 CLKAB	23 CLKBA	2 SAB	22 SBA
X	X	↑	X	X	X
X	X	X	↑	X	X
H	X	↑	↑	X	X

STORAGE FROM A, B, OR A AND B



21 $\overline{OE}$	3 DIR	1 CLKAB	23 CLKBA	2 SAB	22 SBA
L	L	X	H or L	X	H
L	H	H or L	X	H	X

TRANSFER STORED DATA TO A AND/OR B

Figure 1. Bus-Management Functions

Pin numbers shown are for the DW, JT, and NT packages.

Function Tables

SN54ALS646, SN54AS646, SN74ALS646A, SN74AS646

INPUTS						DATA I/O		OPERATION OR FUNCTION
$\overline{OE}$	DIR	CLKAB	CLKBA	SAB	SBA	A1–A8	B1–B8	
X	X	↑	X	X	X	Input	Unspecified†	Store A, B unspecified†
X	X	X	↑	X	X	Unspecified†	Input	Store B, A unspecified†
H	X	↑	↑	X	X	Input	Input	Store A and B data
H	X	H or L	H or L	X	X	Input disabled	Input disabled	Isolation, hold storage
L	L	X	X	X	L	Output	Input	Real-time B data to A bus
L	L	X	H or L	X	H	Output	Input	Stored B data to A bus
L	H	X	X	L	X	Input	Output	Real-time A data to B bus
L	H	H or L	X	H	X	Input	Output	Stored A data to B bus

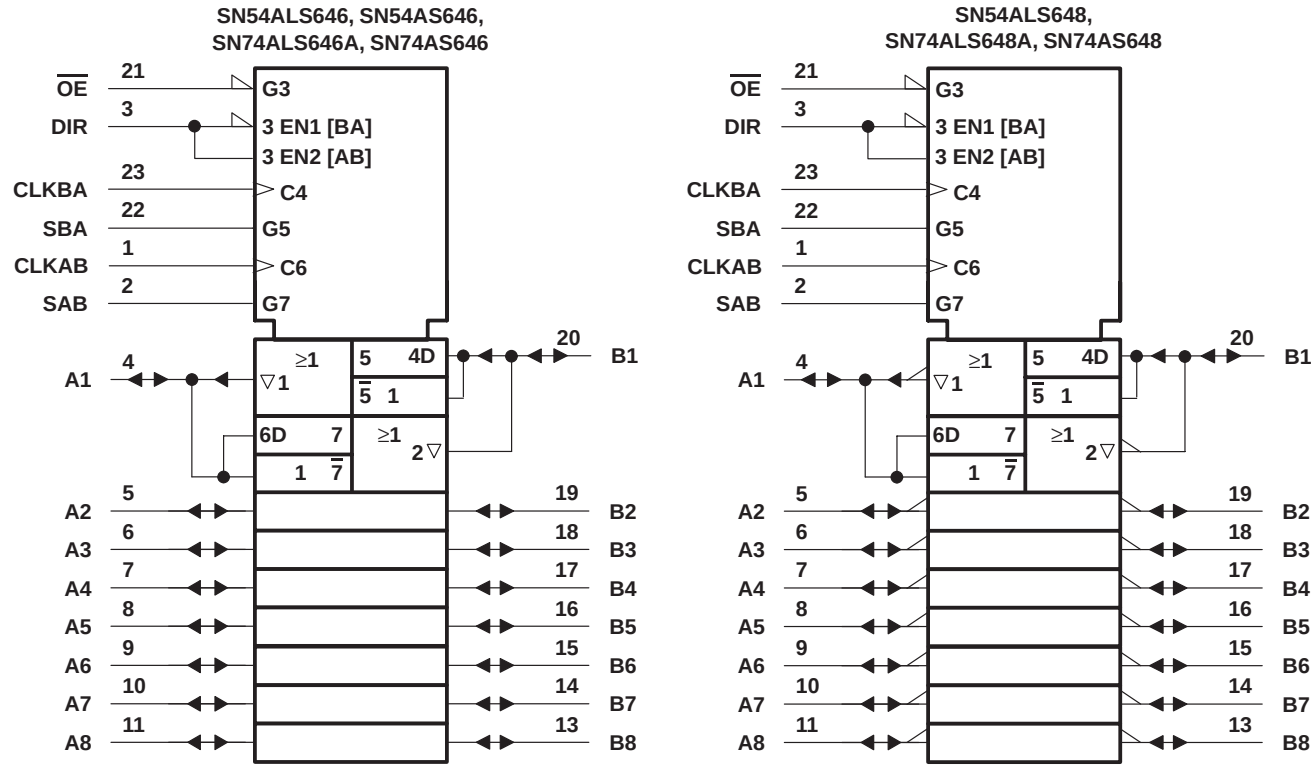
† The data output functions can be enabled or disabled by various signals at $\overline{OE}$ and DIR. Data input functions are always enabled; i.e., data at the bus terminals is stored on every low-to-high transition of the clock inputs.

SN54ALS648, SN74ALS648A, SN74AS648

INPUTS						DATA I/O		OPERATION OR FUNCTION
$\overline{OE}$	DIR	CLKAB	CLKBA	SAB	SBA	A1–A8	B1–B8	
X	X	↑	X	X	X	Input	Unspecified†	Store A, B unspecified†
X	X	X	↑	X	X	Unspecified†	Input	Store B, A unspecified†
H	X	↑	↑	X	X	Input	Input	Store A and B data
H	X	H or L	H or L	X	X	Input disabled	Input disabled	Isolation, hold storage
L	L	X	X	X	L	Output	Input	Real-time $\overline{B}$ data to A bus
L	L	X	H or L	X	H	Output	Input	Stored $\overline{B}$ data to A bus
L	H	X	X	L	X	Input	Output	Real-time $\overline{A}$ data to B bus
L	H	H or L	X	H	X	Input	Output	Stored $\overline{A}$ data to B bus

† The data output functions can be enabled or disabled by various signals at $\overline{OE}$ and DIR. Data input functions are always enabled; i.e., data at the bus terminals is stored on every low-to-high transition of the clock inputs.

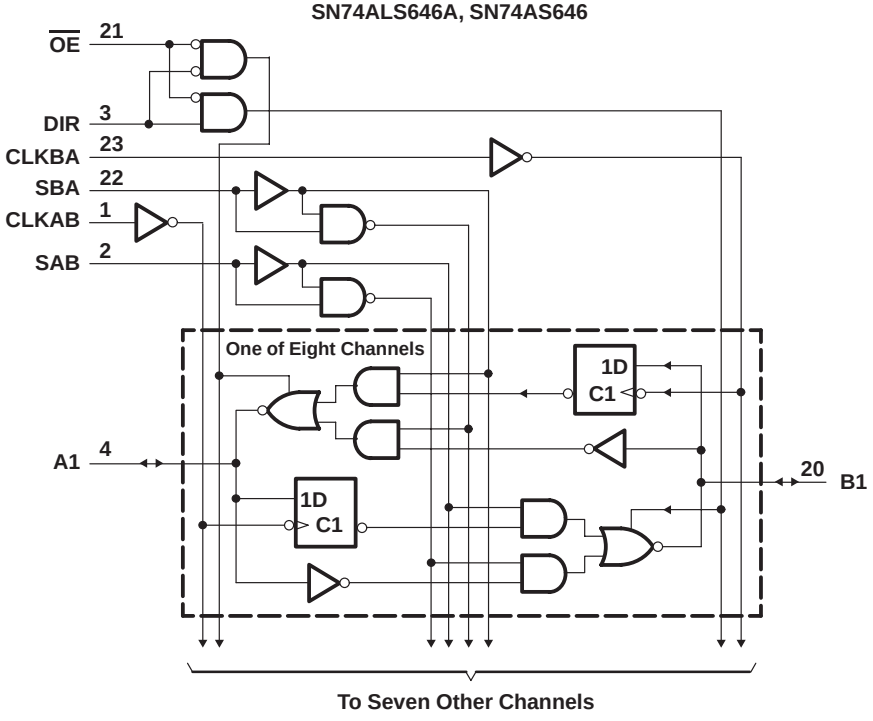
logic symbols†



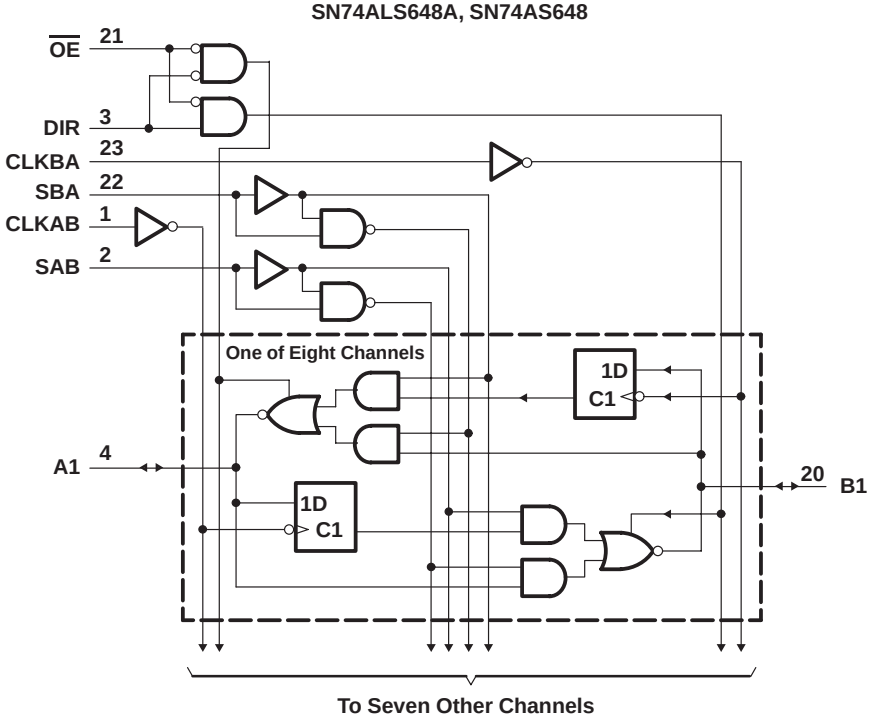
† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the DW, JT, and NT packages.

logic diagrams (positive logic)

**SN54ALS646, SN54AS646,
SN74ALS646A, SN74AS646**



**SN54ALS648,
SN74ALS648A, SN74AS648**



Pin numbers shown are for the DW, JT, and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} . . . . . 7 V
Input voltage, V_I: Control inputs . . . . . 7 V
I/O ports . . . . . 5.5 V
Operating free-air temperature range, T_A: SN54ALS646 . . . . . −55°C to 125°C
SN74ALS646A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		SN54ALS646			SN74ALS646A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			−12			−15	mA
I_{OL}	Low-level output current			12			24	mA
							48‡	
f_{clock}	Clock frequency	0		35	0		40	MHz
t_w	Pulse duration, CLKBA or CLKAB high or low	14.5			12.5			ns
t_{su}	Setup time, A before CLKAB↑ or B before CLKBA↑	15			10			ns
t_h	Hold time, A after CLKAB↑ or B after CLKBA↑	0			0			ns
T_A	Operating free-air temperature	−55		125	0		70	°C

‡ Applies only to the -1 version and only if V_{CC} is maintained between 4.75 V and 5.25

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS646			SN74ALS646A			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = –18 mA			–1.2			–1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = –0.4 mA	V_{CC}–2			V_{CC}–2			V
		V_{CC} = 4.5 V	I_{OH} = –3 mA	2.4	3.2		2.4	3.2		
			I_{OH} = –12 mA	2						
			I_{OH} = –15 mA				2			
V_{OL}		V_{CC} = 4.5 V	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
			I_{OL} = 24 mA					0.35	0.5	
			I_{OL} = 48 mA‡					0.35	0.5	
I_I	Control inputs	V_{CC} = 5.5 V	V_I = 7 V			0.1			0.1	mA
	A or B ports		V_I = 5.5 V			0.1			0.1	
I_{IH}	Control inputs	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	µA
	A or B ports§					20			20	
I_{IL}	Control inputs	V_{CC} = 5.5 V,	V_I = 0.4 V			–0.2			–0.2	mA
	A or B ports§					–0.2			–0.2	
I_O¶		V_{CC} = 5.5 V,	V_O = 2.25 V	–20		–112	–30		–112	mA
I_{CC}		V_{CC} = 5.5 V	Outputs high		47	76		47	76	mA
			Outputs low		55	88		55	88	
			Outputs disabled		55	88		55	88	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ Applies only to the -1 version and only if V_{CC} is maintained between 4.75 V and 5.25
§ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
¶ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX†				UNIT
			SN54ALS646		SN74ALS646A		
			MIN	MAX	MIN	MAX	
f_{max}			35		40		MHz
t_{PLH}	CLKBA or CLKAB	A or B	10	35	7	30	ns
t_{PHL}			5	20	5	17	
t_{PLH}	A or B	B or A	5	22	3	20	ns
t_{PHL}			3	15	3	12	
t_{PLH}	SBA or SAB‡ (stored data low)	A or B	10	40	7	35	ns
t_{PHL}			5	23	5	20	
t_{PLH}	SBA or SAB‡ (stored data high)	A or B	8	30	6	25	ns
t_{PHL}			5	24	5	20	
t_{PZH}	$\overline{OE}$	A or B	3	20	2	17	ns
t_{PZL}			5	22	4	20	
t_{PHZ}	$\overline{OE}$	A or B	1	12	1	10	ns
t_{PLZ}			1	20	2	16	
t_{PZH}	DIR	A or B	5	38	3	30	ns
t_{PZL}			5	30	4	25	
t_{PHZ}	DIR	A or B	1	12	1	10	ns
t_{PLZ}			2	21	2	16	

† For conditions shown MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ These parameters are measured with the internal output state of the storage register opposite that of the bus input.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} . . . . . 7 V
Input voltage, V_I: Control inputs . . . . . 7 V
I/O ports . . . . . 5.5 V
Operating free-air temperature range, T_A: SN54ALS648 . . . . . −55°C to 125°C
SN74ALS648A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		SN54ALS648			SN74ALS648A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			−12			−15	mA
I_{OL}	Low-level output current			12			24	mA
f_{clock}	Clock frequency	0		35	0		40	MHz
t_w	Pulse duration, CLKBA or CLKAB high or low	14.5			12.5			ns
t_{su}	Setup time, A before CLKAB↑ or B before CLKBA↑	15			10			ns
t_h	Hold time, A after CLKAB↑ or B after CLKBA↑	0			0			ns
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS648			SN74ALS648A			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = –18 mA			–1.2			–1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = –0.4 mA	V_{CC}–2			V_{CC}–2			V
		V_{CC} = 4.5 V	I_{OH} = –3 mA	2.4	3.2		2.4	3.2		
			I_{OH} = –12 mA	2						
			I_{OH} = –15 mA				2			
V_{OL}		V_{CC} = 4.5 V	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
			I_{OL} = 24 mA					0.35	0.5	
I_I	Control inputs	V_{CC} = 5.5 V	V_I = 7 V			0.1			0.1	mA
	A or B ports		V_I = 5.5 V			0.1			0.1	
I_{IH}	Control inputs	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	µA
	A or B ports‡					20			20	
I_{IL}	Control inputs	V_{CC} = 5.5 V,	V_I = 0.4 V			–0.2			–0.2	mA
	A or B ports‡					–0.2			–0.2	
I_O§		V_{CC} = 5.5 V,	V_O = 2.25 V	–20		–112	–30		–112	mA
I_{CC}		V_{CC} = 5.5 V	Outputs high		47	76		47	76	mA
			Outputs low		57	88		57	88	
			Outputs disabled		57	88		57	88	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX†				UNIT
			SN54ALS648		SN74ALS648A		
			MIN	MAX	MIN	MAX	
f_{max}			35		40		MHz
t_{PLH}	CLKBA or CLKAB	A or B	8	39	7	33	ns
t_{PHL}			5	23	5	20	
t_{PLH}	A or B	B or A	3	20	2	17	ns
t_{PHL}			2	12	2	10	
t_{PLH}	SBA or SAB‡ (stored data low)	A or B	5	44	5	39	ns
t_{PHL}			4	26	4	22	
t_{PLH}	SBA or SAB‡ (stored data high)	A or B	6	30	6	25	ns
t_{PHL}			6	25	6	21	
t_{PZH}	$\overline{OE}$	A or B	4	25	2	22	ns
t_{PZL}			4	25	4	22	
t_{PHZ}	$\overline{OE}$	A or B	1	12	1	10	ns
t_{PLZ}			2	21	2	15	
t_{PZH}	DIR	A or B	4	35	2	27	ns
t_{PZL}			3	25	3	19	
t_{PHZ}	DIR	A or B	1	17	1	14	ns
t_{PLZ}			2	22	2	15	

† For conditions shown MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ These parameters are measured with the internal output state of the storage register opposite that of the bus input.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} . . . . . 7 V
Input voltage, V_I: Control inputs . . . . . 7 V
I/O ports . . . . . 5.5 V
Operating free-air temperature range, T_A: SN54AS646 . . . . . –55°C to 125°C
SN74AS646 . . . . . 0°C to 70°C
Storage temperature range . . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54AS646			SN74AS646			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				–12			–15	mA
I_{OL}	Low-level output current				32			48	mA
f_{clock}*	Clock frequency		0		75	0		90	MHz
t_w*	Pulse duration	CLKBA or CLKAB high	6			5			ns
		CLKBA or CLKAB low	7			6			
t_{su}*	Setup time, A before CLKAB↑ or B before CLKBA↑		7			6			ns
t_h*	Hold time, A after CLKAB↑ or B before CLKBA		0			0			ns
T_A	Operating free-air temperature		–55		125	0		70	°C

* On products compliant to MIL-STD-883, Class B, this parameter is based on characterization data but is not production tested.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS646			SN74AS646			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = –18 mA			–1.2			–1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = –2 mA	V_{CC}–2			V_{CC}–2			V
		V_{CC} = 4.5 V	I_{OH} = –3 mA	2.4	3.2		2.4	3.2		
			I_{OH} = –12 mA	2						
			I_{OH} = –15 mA				2			
V_{OL}		V_{CC} = 4.5 V	I_{OL} = 32 mA		0.25	0.5				V
			I_{OL} = 48 mA					0.35	0.5	
I_I	Control inputs	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	A or B ports	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1			0.1	
I_{IH}	Control inputs	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	µA
	A or B ports‡					70			70	
I_{IL}	Control input	V_{CC} = 5.5 V,	V_I = 0.4 V			–0.5			–0.5	mA
	A or B ports‡					–0.75			–0.75	
I_O§		V_{CC} = 5.5 V,	V_O = 2.25 V	–30		–112	–30		–112	mA
I_{CC}		V_{CC} = 5.5 V	Outputs high		120	195		120	195	mA
			Outputs low		130	211		130	211	
			Outputs disabled		130	211		130	211	

† All typical values are at V_{CC} = 5 V, T_A = 25 °C.
‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX†				UNIT
			SN54AS646		SN74AS646		
			MIN	MAX	MIN	MAX	
f_{max}*			75		90		MHz
t_{PLH}	CLKBA or CLKAB	A or B	2	9.5	2	8.5	ns
t_{PHL}			2	10	2	9	
t_{PLH}	A or B	B or A	2	11.5	2	9	ns
t_{PHL}			1	8	1	7	
t_{PLH}	SBA or SAB‡	A or B	2	13.5	2	11	ns
t_{PHL}			2	11	2	9	
t_{PZH}	$\overline{OE}$	A or B	2	11	2	9	ns
t_{PZL}			3	15	3	14	
t_{PHZ}	$\overline{OE}$	A or B	2	11	2	9	ns
t_{PLZ}			2	11	2	9	
t_{PZH}	DIR	A or B	3	21	3	16	ns
t_{PZL}			3	24	3	18	
t_{PHZ}	DIR	A or B	2	12	2	10	ns
t_{PLZ}			2	12	2	10	

* On products compliant to MIL-STD-883, Class B, this parameter is based on characterization data but is not production tested.
† For conditions shown MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ These parameters are measured with the internal output state of the storage register opposite that of the bus input.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} . . . . . 7 V
Input voltage, V_I: Control inputs . . . . . 7 V
I/O ports . . . . . 5.5 V
Operating free-air temperature range, T_A: SN74AS648 . . . . . 0°C to 70°C
Storage temperature range . . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN74AS648			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current				–15	mA
I_{OL}	Low-level output current				48	mA
f_{clock}	Clock frequency		0		90	MHz
t_w	Pulse duration	CLKBA or CLKAB high	5			ns
		CLKBA or CLKAB low	6			
t_{su}	Setup time, A before CLKAB↑ or B before CLKBA↑		6			ns
t_h	Hold time, A after CLKAB↑ or B before CLKBA		0			ns
T_A	Operating free-air temperature		0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN74AS648			UNIT
				MIN	TYP‡	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = –18 mA			–1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = –2 mA	V_{CC}–2			V
		V_{CC} = 4.5 V	I_{OH} = –3 mA	2.4	3.2		
			I_{OH} = –15 mA	2			
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 48 mA		0.35	0.5	V
I_I	Control inputs	V_{CC} = 5.5 V	V_I = 7 V			0.1	mA
	A or B ports		V_I = 5.5 V			0.1	
I_{IH}	Control inputs	V_{CC} = 5.5 V,	V_I = 2.7 V			20	µA
	A or B ports§					70	
I_{IL}	Control input	V_{CC} = 5.5 V,	V_I = 0.4 V			–0.5	mA
	A or B ports§					–0.75	
I_O¶		V_{CC} = 5.5 V,	V_O = 2.25 V	–30		–112	mA
I_{CC}		V_{CC} = 5.5 V	Outputs high		110	185	mA
			Outputs low		120	195	
			Outputs disabled		120	195	

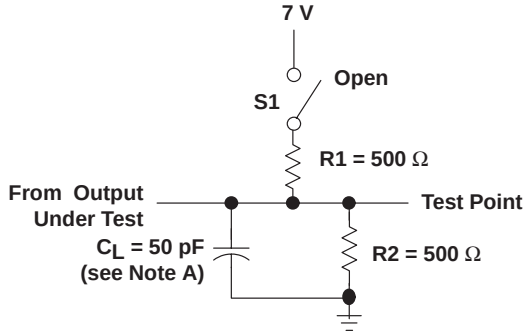
‡ All typical values are at V_{CC} = 5 V, T_A = 25 °C.
§ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
¶ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX†		UNIT
			SN74AS648		
			MIN	MAX	
f_{max}			90		MHz
t_{PLH}	CLKBA or CLKAB	A or B	2	8.5	ns
t_{PHL}			2	9	
t_{PLH}	A or B	B or A	2	8	ns
t_{PHL}			1	7	
t_{PLH}	SBA or SAB‡	A or B	2	11	ns
t_{PHL}			2	9	
t_{PZH}	$\overline{OE}$	A or B	2	9	ns
t_{PZL}			3	15	
t_{PHZ}	$\overline{OE}$	A or B	2	9	ns
t_{PLZ}			2	9	
t_{PZH}	DIR	A or B	3	16	ns
t_{PZL}			3	18	
t_{PHZ}	DIR	A or B	2	10	ns
t_{PLZ}			2	10	

† For conditions shown MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ These parameters are measured with the internal output state of the storage register opposite that of the bus input.

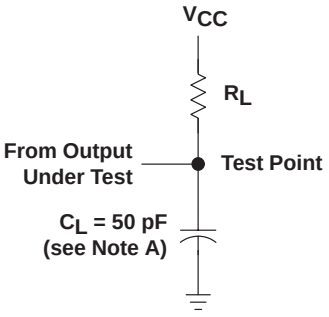
PARAMETER MEASUREMENT INFORMATION



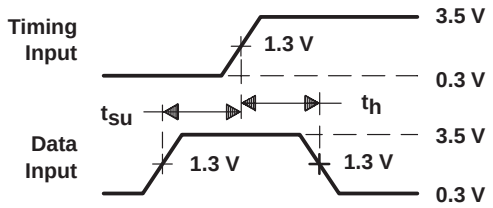
LOAD CIRCUIT
FOR 3-STATE OUTPUTS

SWITCH POSITION TABLE

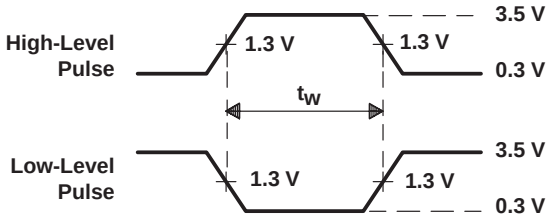
TEST	S1
t_{PLH}	Open
t_{PHL}	Open
t_{PZH}	Open
t_{PZL}	Closed
t_{PHZ}	Open
t_{PLZ}	Closed



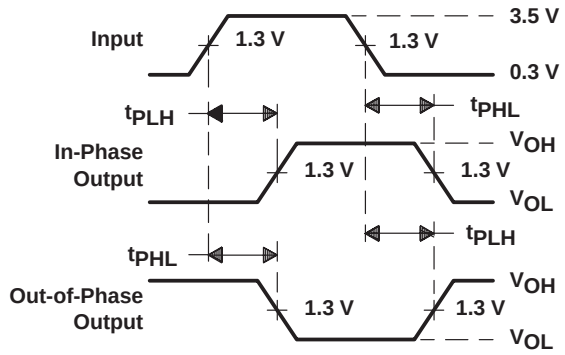
LOAD CIRCUIT
FOR OPEN-COLLECTOR OUTPUTS



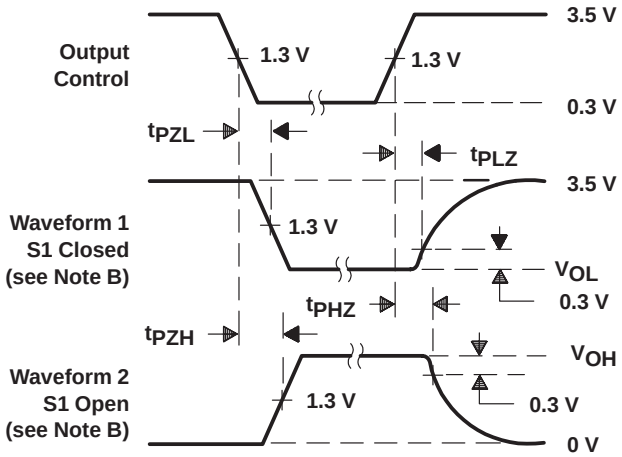
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 2 ns, t_f ≤ 2 ns.
D. The outputs are measured one at a time with one transition per measurement.

Figure 2. Load Circuits and Voltage Waveforms

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SN54ALS648, Octal Bus Transceivers & Registers With 3 -State Outputs

DEVICE STATUS: **ACTIVE**

PARAMETER NAME	SN54ALS648
Voltage Nodes (V)	5

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- Independent Registers for A and B Buses
- Multiplexed Real-Time and Stored Data
- Choice of True or Inverting Data Paths
- Choice of 3-State or Open-Collector Outputs
- Package Options Include Plastic Small-Outline (DW) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (NT) and Ceramic (JT) 300-mil DIPs

DESCRIPTION

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The -1 version of the SN74ALS646A is identical to the standard version, except that the recommended maximum I_{OL} in the -1 version is increased to 48 mA. There are no -1 versions of the SN54ALS646, SN54ALS648, or SN74ALS648A.

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- Designing With Logic (Rev. C) (SDYA009C - Updated: 06/01/1997)
- Evaluation of Nickel/Palladium/Gold-Finished Surface-Mount Integrated Circuits (SZZA026 - Updated: 06/20/2001)
- Input and Output Characteristics of Digital Integrated Circuits (SDYA010 - Updated: 10/01/1996)
- Live Insertion (SDYA012 - Updated: 10/01/1996)
- TI IBIS File Creation, Validation, and Distribution Processes (SZZA034 - Updated: 08/29/2002)
- Understanding and Interpreting Texas Instruments Standard-Logic Products Data Sh (Rev. A) (SZZA036A - Updated: 02/27/2003)

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- Enhanced Plastic Portfolio Brochure (SGZB004, 387 KB - Updated: 08/19/2002)
- Logic Reference Guide (SCYB004, 1032 KB - Updated: 10/23/2001)
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ORDERABLE DEVICE	STATUS	PACKAGE TYPE | PINS	TEMP (°C)	DSCC NUMBER	PRODUCT CONTENT	BUDGETARY PRICING QTY | $US	STD PACK QTY	IN STOCK	IN PROGRESS QTY | DATE	LEAD TIME	DISTRIBUTOR COMPANY | REGION	IN STOCK	PURCHASE
5962-9052301LA	ACTIVE	CDIP (JT) | 24	-55 TO 125		View Contents	1KU | 9.50	1	264*	>10k | 20 May	8 WKS	None Reported View Distributors		
SNJ54ALS648FK	OBSOLETE	(FK) | 24	-55 TO 125		View Contents	1KU |		0*		Call**	None Reported View Distributors		
SNJ54ALS648JT	ACTIVE	CDIP (JT) | 24	-55 TO 125	5962-9052301LA	View Contents	1KU | 9.50	1	10*	>10k | 20 May	8 WKS	None Reported View Distributors		
SNJ54ALS648W	OBSOLETE	CFP (W) | 24	-55 TO 125		View Contents	1KU |		0*		Call**	None Reported View Distributors		

Table Data Updated on: 4/17/2003

Product Folder: SN54ALS648, Octal Bus Transceivers & Registers With 3 -State Outputs

SN54ALS646, Octal Registered Bus Transceivers with 3-State Outputs

DEVICE STATUS: **ACTIVE**

PARAMETER NAME	SN54ALS646
Voltage Nodes (V)	5

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- Independent Registers for A and B Buses
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5962-89956013A	ACTIVE	LCCC (FK) | 28	-55 TO 125		View Contents	1KU | 15.06	1	25*	3536 | 20 May	8 WKS	None Reported View Distributors		
									3876 | 27 May				
5962-8995601LA	ACTIVE	CDIP (JT) | 24	-55 TO 125		View Contents	1KU | 9.50	1	199*	8338 | 20 May	8 WKS	None Reported View Distributors		
SNJ54ALS646FK	ACTIVE	LCCC (FK) | 28	-55 TO 125	5962-89956013A	View Contents	1KU | 15.06	1	0*	3668 | 20 May	8 WKS	None Reported View Distributors		
									4021 | 27 May				
SNJ54ALS646JT	ACTIVE	CDIP (JT) | 24	-55 TO 125	5962-8995601LA	View Contents	1KU | 9.50	1	237*	7967 | 20 May	8 WKS	None Reported View Distributors		
SNJ54ALS646W	OBSOLETE	CFP (W) | 24	-55 TO 125		View Contents	1KU |		0*		Call**	None Reported View Distributors		

Table Data Updated on: 4/17/2003

Product Folder: SN54ALS646, Octal Registered Bus Transceivers with 3-State Outputs

SN54AS646, Octal Bus Transceivers & Registers With 3 -State Outputs

DEVICE STATUS: **ACTIVE**

PARAMETER NAME	SN54AS646	SN74AS646
Voltage Nodes (V)	5	5
Vcc range (V)	4.5 to 5.5	4.5 to 5.5
Input Level	TTL	TTL
Output Level	TTL	TTL
No. of Outputs	8	8
Static Current		203

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- Advanced Schottky Load Management (SDYA016 - Updated: 02/01/1997)
- Designing With Logic (Rev. C) (SDYA009C - Updated: 06/01/1997)
- Evaluation of Nickel/Palladium/Gold-Finished Surface-Mount Integrated Circuits (SZZA026 - Updated: 06/20/2001)
- Input and Output Characteristics of Digital Integrated Circuits (SDYA010 - Updated: 10/01/1996)
- Live Insertion (SDYA012 - Updated: 10/01/1996)
- TI IBIS File Creation, Validation, and Distribution Processes (SZZA034 - Updated: 08/29/2002)
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ORDERABLE DEVICE	STATUS	PACKAGE TYPE | PINS	TEMP (°C)	DSCC NUMBER	PRODUCT CONTENT	BUDGETARY PRICING QTY | $US	STD PACK QTY
5962-87595013A	ACTIVE	LCCC (FK) | 28	-55 TO 125		View Contents	1KU | 15.06	1
5962-8759501KA	ACTIVE	CFP (W) | 24	-55 TO 125		View Contents	1KU | 11.58	1
5962-8759501LA	ACTIVE	CDIP (JT) | 24	-55 TO 125		View Contents	1KU | 9.50	1
SN54AS646JT	ACTIVE	CDIP (JT) | 24	-55 TO 125		View Contents	1KU | 8.11	1

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0*	3624 | 20 May	8 WKS
	>10k | 27 May	
0*	>10k | 20 May	8 WKS
288*	>10k | 20 May	8 WKS

REPORTED DISTRIBUTOR INVENTORY
As Of 09:00 AM GMT, 17 Apr 2003

DISTRIBUTOR COMPANY | REGION	IN STOCK	PURCHASE
None Reported View Distributors		
None Reported View Distributors		
None Reported View Distributors		

Product Folder: SN54AS646, Octal Bus Transceivers & Registers With 3 -State Outputs

SNJ54AS646FK	ACTIVE	LCCC (FK)	28	-55 TO 125	5962-87595013A	View Contents	1KU | 15.06	1	191*	>10k | 20 May	8 WKS	None Reported View Distributors	
									0*	3447 | 20 May	8 WKS	None Reported View Distributors	
SNJ54AS646JT	ACTIVE	CDIP (JT)	24	-55 TO 125	5962-8759501LA	View Contents	1KU | 9.50	1		>10k | 27 May			
SNJ54AS646W	ACTIVE	CFP (W)	24	-55 TO 125	5962-8759501KA	View Contents	1KU | 11.58	1	115*	>10k | 20 May	8 WKS	EBV Electronik | Europe	11
									0*	>10k | 20 May	8 WKS	None Reported View Distributors	

Table Data Updated on: 4/17/2003